

FX-427 Low Jitter Frequency Translator



Features

- Quartz-based PLL for Ultra-Low Jitter
- Frequency Translation up to 850 MHz
- Accepts 4 externally-muxed clock inputs
- LVCMOS/LVDS/LVPECL Inputs Compatible
- Differential LVPECL Outputs
- Lock Detect
- Output Disable
- 20.3 x 13.7 x 5.1 mm surface mount package
- Compliant to EC RoHS Directive



Description

The FX-427 is a precision quartz-based frequency translator used to translate 1 to 4 selected input clocks as low as 8 kHz to an integer multiple as high as 850 MHz. The FX-427's superior jitter performance is achieved through the filtering action of the on-board voltage-controlled SAW oscillator (VCISO) and integrated loop filter. Two low-jitter outputs are provided. Monitoring and control functionality are also standard features.

Applications

- Wireless Infrastructure
- 802.16 BTS
- 10 Gigabit FC
- 10GbE LAN / WAN
- OADM and IP Routers
- Test Equipment

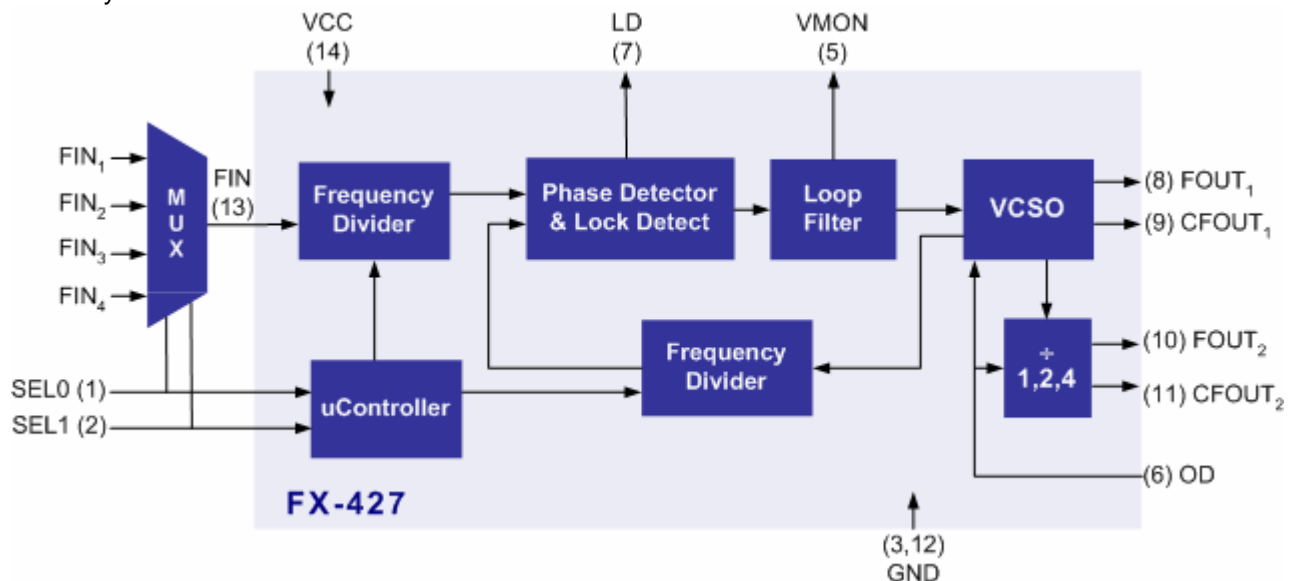


Figure 1. Functional Block Diagram

FX-427 Low Jitter Frequency Translator

Table 1. Electrical Performance						
Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Frequency						
Input Frequency	F_{IN}	0.008		200	MHz	1,2,3
Capture Range	APR	± 40			ppm	1,2,3
Output Frequency - Primary	F_{OUT1}	500		850	MHz	1,2,3
Output Frequency - Secondary	F_{OUT2}	125		850	MHz	1,2,3
Supply						
Voltage	V_{CC}	3.13	3.3	3.46	V	2,3
Current (No Load)	I_{CC}		140	180	mA	3
Input Signal						
CMOS	F_{IN}		CMOS			
LVDS	F_{IN}		LVDS			2,3
LVPECL	F_{IN}		LVPECL			
Differential Output (Options F and P)						
Common Mode Output Voltage	V_{OCM}	$V_{CC}-1.5$	$V_{CC}-1.3$	$V_{CC}-1.1$	V	3,5
DC Output High Voltage	V_{OH}	$V_{CC}-1.085$	$V_{CC}-0.950$	$V_{CC}-0.880$	V	3,5
DC Output Low Voltage	V_{OL}	$V_{CC}-1.830$	$V_{CC}-1.700$	$V_{CC}-1.620$	V	3,5
Peak-to-Peak Output Voltage	V_{P-P}		700		mV-pp	3,5
Rise Time	t_R		0.5		ns	4,5
Fall Time	t_F		0.5		ns	4,5
Symmetry	SYM	45	50	55	%	2,3
SSB Phase Noise, $F_{OUT} = 155.52/622.08$						
@ 10 Hz Offset	Φ_n		-64/-27		dBc/Hz	
@ 100 Hz Offset	Φ_n		-95/-55		dBc/Hz	
@ 1 kHz Offset	Φ_n		-123/-85		dBc/Hz	
@ 10 kHz Offset	Φ_n		-143/-110		dBc/Hz	5,6
@ 100 kHz Offset	Φ_n		-146/-130		dBc/Hz	
@ 1 MHz Offset	Φ_n		-146/-146		dBc/Hz	
@ 10 MHz Offset	Φ_n		-146/-146		dBc/Hz	
Jitter Generation						
155.52 MHz (12 kHz – 20 MHz BW)	Φ_J		0.30		ps RMS	5, 6
622.08 MHz (12 kHz – 20 MHz BW)	Φ_J		0.12		ps RMS	
Operating Temperature (Options C or F)						
	T_{OP}	0° to 70° or -40 to +85°			°C	1,3

1. See Standard Frequencies and Ordering Information.
2. Parameters are tested with production test circuit below (Fig 2).
3. Parameters are tested at ambient temperature with test limits guard banded for specified operating temperature.
4. Measured from 20% to 80% of a full output swing (Fig 3).
5. Not tested in production, guaranteed by design, verified at qualification.
6. The FX-427 phase noise and jitter performance can be optimized for specific applications. Please consult with Vectron's Application Engineers for more information.

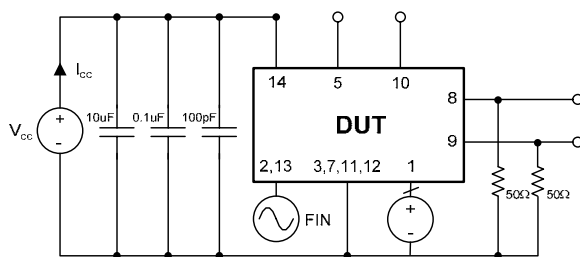


Figure 2. Test Circuit

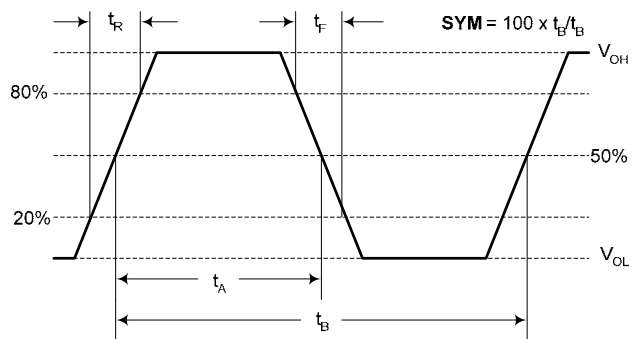


Figure 3. LVPECL Waveform

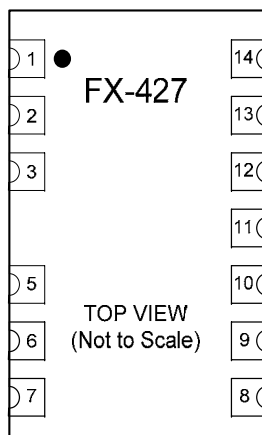


Figure 4. Pin Configuration

Table 2. Pin Out

Pin #	Symbol	I/O	Level	Function
1	SEL0	I	LVC MOS	Frequency Select - see table 3
2	SEL1	I	LVC MOS	Frequency Select – see table 3
3	GND	GND	Supply	Case and Electrical Ground
4				Not present
5	VMON	O	Analog (0 – V _{cc})	VCXO Control Voltage Monitor Under locked conditions VMON should be > 0.3V and <3.0V. The input frequency may be out of range if the voltage exceeds these levels.
6	OD	I	LVC MOS	Output Disable Disabled = Logic “1” Enabled = Logic “0” or no connect
7	LD	O	LVC MOS	Lock Detect Locked = Logic “1” Loss of Lock = Logic “0”
8	FOUT1	O	LCPECL	Frequency Output – Primary
9	CFOUT1	O	LVPECL	Complimentary Frequency Output - Primary
10	FOUT2	O	LVPECL	Divided-Down VCXO/VCXO Output, or Disabled
11	CFOUT2	O	LVPECL	Complimentary Divided-Down VCXO/VCXO Output, or Disabled
12	GND	GND	Supply	Case and Electrical Ground
13	FIN	I	LVC MOS or LVPECL	Input Frequency – AC Coupled
14	VCC	VCC	Supply	Power Supply Voltage (3.3 V ±5%)

Table 3. Control Logic (LVC MOS)

SELO		SEL1		CLOCK INPUT	
0	0	0	0	FIN ₁	
0	0	0	1	FIN ₂	
1	0	0	0	FIN ₃	
1	0	0	1	FIN ₄	

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Outline Diagram

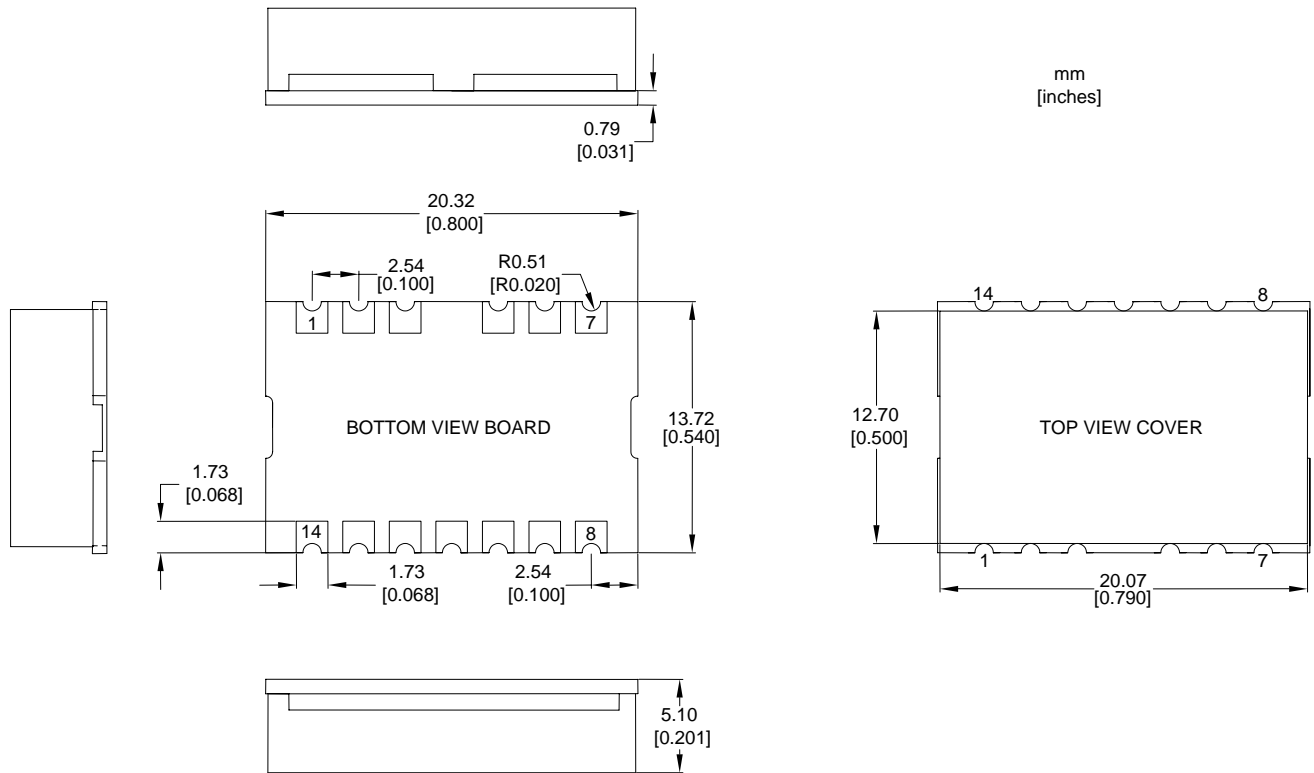


Figure 5.

Suggested Pad Layout

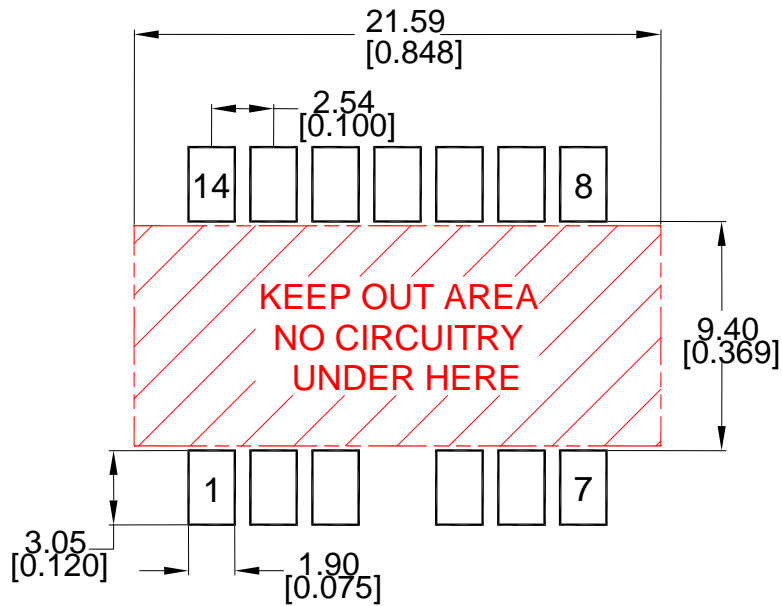


Figure 6.

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power Supply	V _{CC}	0 to 6	V
Storage Temperature	TS	-55 to 125	°C
Soldering Temp/Time	T _{LS}	260/40	°C/sec

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The FX-427 family is undergoing the following qualification tests:

Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016

Handling Precautions

Although ESD protection circuitry has been designed into the FX-427 proper precautions should be taken when handling and mounting. VI employs a human body model (HBM) and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation

ESD Ratings

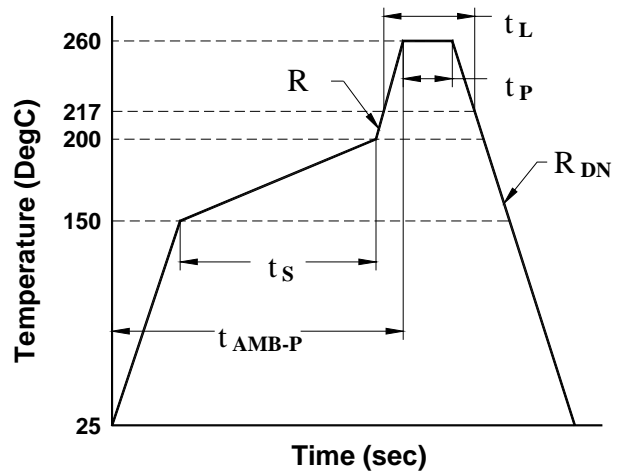
Model	Minimum	Conditions
Human Body Model	500 V	MIL-STD 883, Method 3015
Charged Device Model	500 V	JEDEC, JESD22-C101

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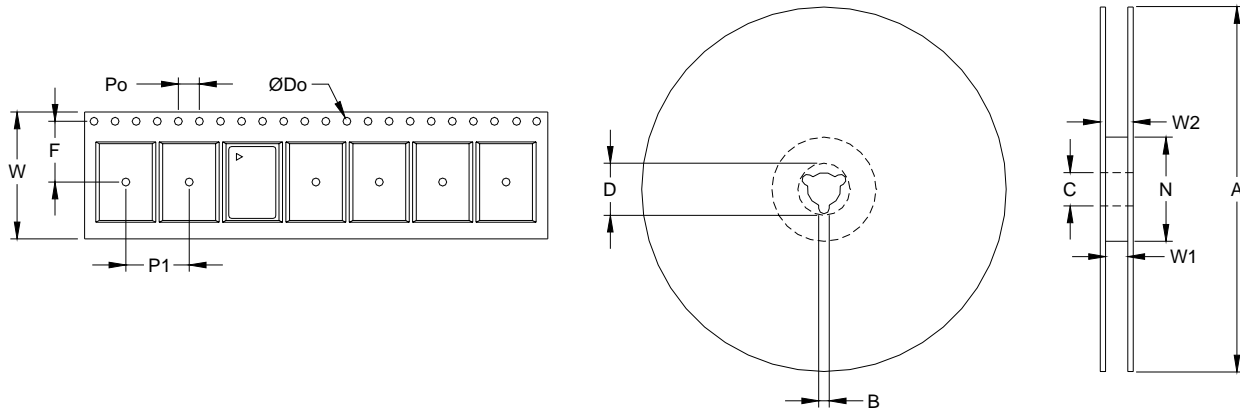
Reflow Profile (IPC/JEDEC J-STD-020C)

Parameter	Symbol	Value
PreHeat Time	t_s	60 sec Min, 180 sec Max
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	t_{AMB-P}	480 sec Max
Time At 260 °C	t_P	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 °C/sec Max

The FX-427 is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The temperatures refer to the top side of the package, measured on the package body surface. The FX-427 should not be subjected to a wash process that will immerse it in solvents. NO CLEAN is the recommended procedure. The FX-427 has been designed for pick and place reflow soldering. The FX-427 may be reflowed once and should not be reflowed in the inverted position.



Tape and Reel



Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	# Per Reel
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Min	Typ	Min	Min	Typ	Max	
FX-427	32	14.2	1.5	4	20	330	1.5	13	20.2	100	44.4	50.4	200

Vectron plans to offer both tape-n-reel and matrix trays as packaging options for the FX-427. The standard shipping container for volume production is a matrix tray. The trays are 100% recyclable and offer the added feature that they can be continuously fed into a pick-n-place machine.

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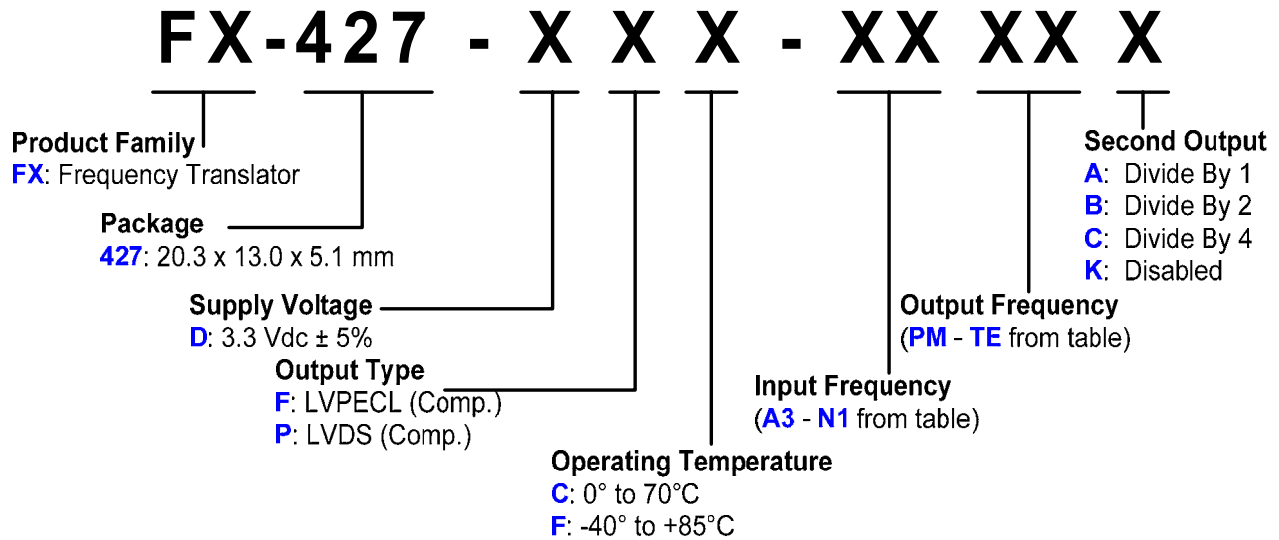
Standard Frequencies (MHz)*											
0.0080	A3	31.2500	H8	166.6286	M5	625.0000	P3	707.3527	TC	781.2500	T9
0.0160	A4	38.8800	H5	167.3316	N2	637.5000	PG	716.5732	T1	796.8750	TB
1.5440	B3	51.8400	J4	201.4160	N1	644.5313	P4	718.7500	T5	805.6641	TA
2.0480	B4	61.4400	J5	300.0000	PT	657.4219	PB	719.7344	T3	809.0635	TE
10.0000	C4	77.7600	K2	311.0400	P1	666.5143	P5	748.0709	T6		
12.3520	D1	125.0000	L4	491.5200	PM	669.3266	R3	750.0000	T7		
19.4400	D6	155.5200	M2	531.2500	P8	672.1627	R5	777.6000	T4		
20.0000	E2	156.2500	M3	569.1964	P9	690.5692	R4	779.5686	T8		
30.7200	H1	161.1328	M4	622.0800	P2	693.4830	R6	780.8810	TD		

Note 1: Other frequencies available upon request.

Note 2: Not all combinations are possible.

Note 3: For multiple input frequencies, replace the Input Frequency Code with "SS" and denote the input frequencies following the part number.

Ordering Information



EXAMPLE: **FX-427-DFF-A3P2C**

FX-427, 3.3V, LVPECL output, -40° to +85°C, $F_{IN1} = 8 \text{ kHz}$, $F_{OUT1} = 622.08 \text{ MHz}$, $F_{OUT2} = 155.52 \text{ MHz}$.

EXAMPLE: **FX-427-DFC-SSP2B, S = 2.048 MHz, 19.44 MHz, 77.76 MHz**

FX-427, 3.3V, LVPECL output, 0° to 70°C, $F_{IN1} = 2.048 \text{ MHz}$, $F_{IN2} = 19.44 \text{ MHz}$, $F_{IN3} = 77.76 \text{ MHz}$, $F_{OUT1} = 622.08 \text{ MHz}$, $F_{OUT2} = 311.04 \text{ MHz}$

For Additional Information, Please Contact:



USA: Vectron International • 267 Lowell Rd. Hudson, NH 03051 •
Tel: 1-88-VECTRON-1 • Fax: 1-888-FAX-VECTRON

EUROPE: Landstrasse, D-74924, Neckarbischofsheim, Germany •
Tel: 49 (0) 7268 8010 • Fax: 49 (0) 7268 801281

ASIA: 1F-2F, No 8 Workshop, No. 308 Fenju Road, WaiGaoQiao Free Trade Zone, Pudong, Shanghai, China 200131
Tel: 86 21 5048 0777 • Fax: 86 21 5048 1881

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