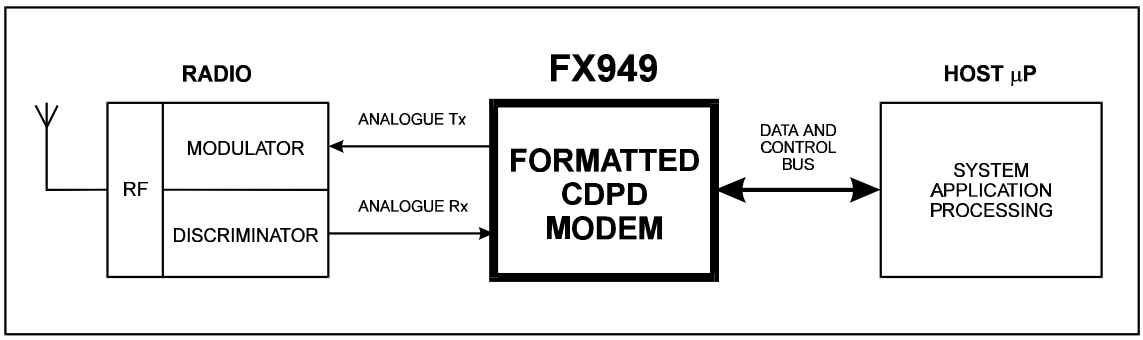
CML Semiconductor Products

CDPD Wireless Modem Data Pump FX949

D/949/5 March 1996
Advance Information

1.0 Features

- **MES Full Duplex Operation**
- **Forward Channel Decoding**
- **Reverse Channel Encoding**
- **Error Detection and Syndrome Output**
- **19.2kb/s GMSK Modulation**
- **Sleep Timer Included**
- **3.3V and 5V Applications**
- **PCMCIA Package Option**



1.1 Brief Description

The FX949 is a low power CMOS integrated circuit which performs all of the real-time signal and data format-management functions required for full-duplex operation of a CDPD Mobile End Station.

The FX949 interfaces directly with the analogue modulation and demodulation circuits of the radio and the host radio/application processor bus.

It accepts application data from the processor, constructs a correct Reverse Channel packet containing this data and converts the packet to GMSK analogue signals for transmission. In receive, Forward Channel GMSK signals from the discriminator are demodulated, the packet disassembled, error checked, and the recovered application data passed to the processor.

The FX949 is the cost, size, and power efficient alternative to DSP design solutions in high performance OEM products for the Cellular Digital Packet Data wireless services.

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1.2 Block Diagram

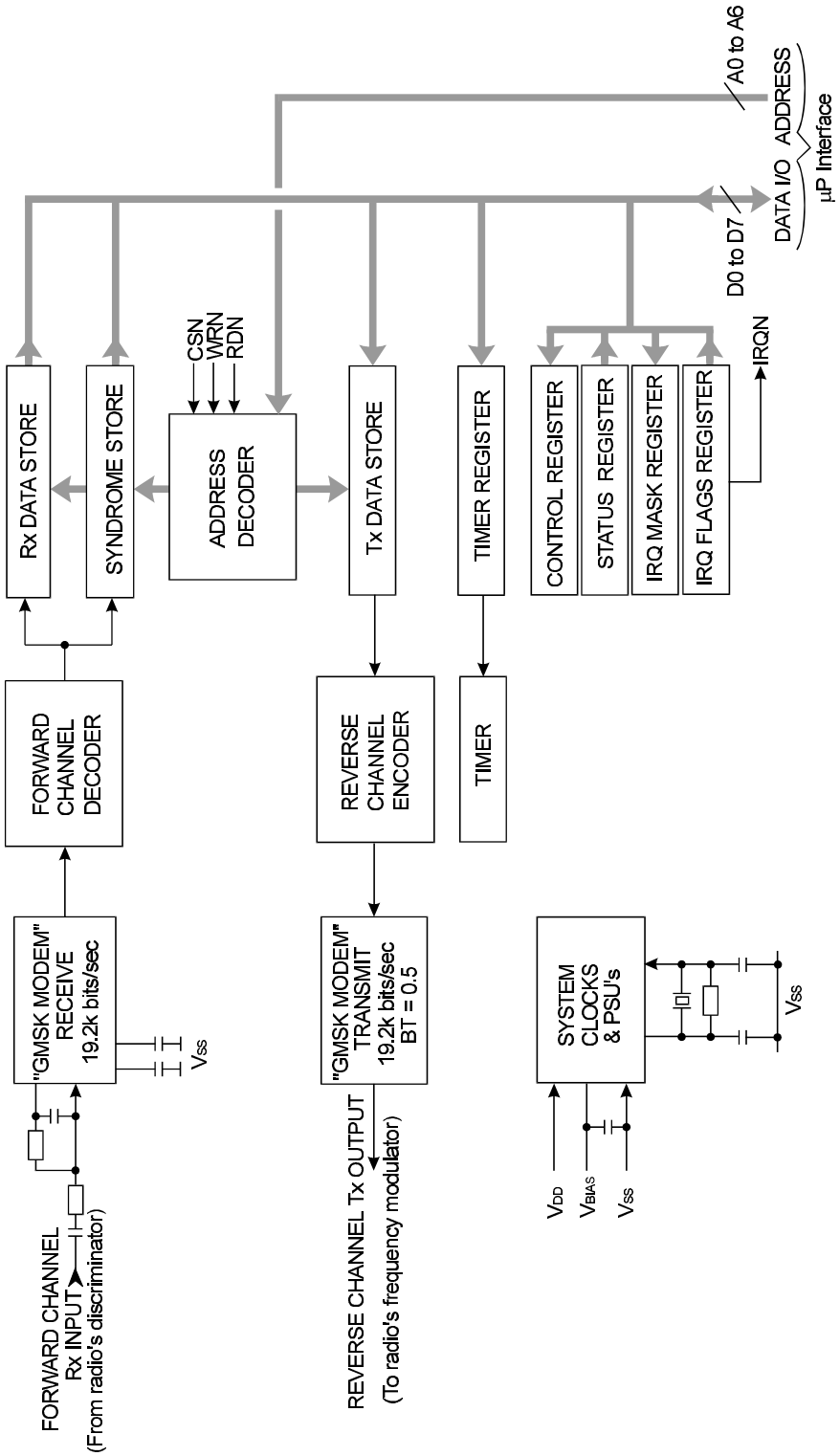


Figure 1 Block Diagram

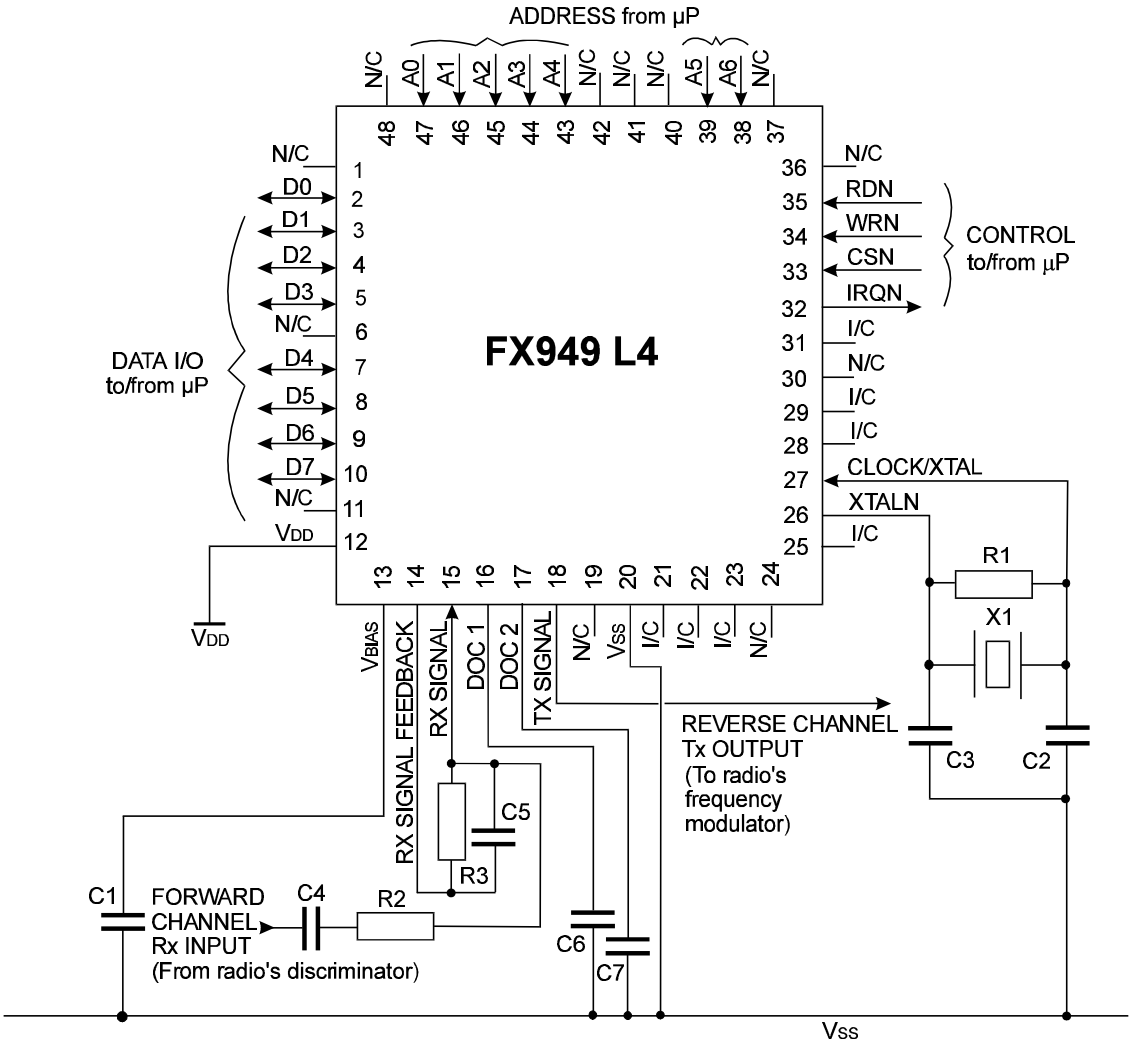
1.3 Signal List

Package L4	Package L6	Signal		Description
Pin No.	**Pin No.**	**Name**	**Type**	
2	8	D0	BI	)
3	9	D1	BI	)
4	10	D2	BI	)
5	11	D3	BI	) 8-bit bidirectional tristate µP interface
7	12	D4	BI	) data lines.
8	13	D5	BI	)
9	14	D6	BI	)
10	15	D7	BI	)
12	17	V_{DD}	Power	The positive supply rail. Levels and voltages are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor.
13	18	V_{BIAS}	O/P	A bias line for the internal circuitry, held at ½ V_{DD}. This pin must be decoupled by a capacitor mounted close to the device pins (see Figures 2 and 3).
14	19	RX SIGNAL FEEDBACK	O/P	The output of the Rx input amplifier and the input to the Rx filter.
15	20	RX SIGNAL	I/P	The inverting input to the Rx input amplifier.
16	21	DOC 1	O/P	) Connections to the Rx level measurement
17	22	DOC 2	O/P	) circuitry. A capacitor should be connected) from each pin to V_{SS}.
18	23	TX SIGNAL	O/P	The inverted Tx signal output from the modem.
20	24	V_{SS}	Power	The negative supply rail (ground).
26	31	XTALN	O/P	The inverted output of the on-chip oscillator.
27	32	CLOCK/XTAL	I/P	The input to the on-chip oscillator, for external Xtal circuit or clock.
32	36	IRQN	O/P	A 'wire-ORable' output for connection to the controlling µP's Interrupt Request input. This output has a low impedance pull down to V_{SS} when active and is high impedance when inactive.

Package L4	Package L6	Signal		Description
Pin No.	**Pin No.**	**Name**	**Type**	
33	37	CSN	I/P	Chip Select. An active low logic level input to the modem, used to enable a data read or write operation.
34	38	WRN	I/P	Write. An active low logic level input used to control the writing of data into the modem from the controlling µP.
35	39	RDN	I/P	Read. An active low logic level input used to control the reading of data from the modem into the controlling µP.
38	41	A6	I/P	)
39	42	A5	I/P	)
43	1	A4	I/P	)
44	2	A3	I/P	) 7 logic level modem register address select
45	3	A2	I/P	) inputs.
46	4	A1	I/P	)
47	5	A0	I/P	)
1, 6, 11, 19, 24, 30, 36, 37, 40, 41, 42, 48	6, 7, 16, 28, 30, 40, 43, 44			))) No internal connection: leave open circuit.)))
21, 22, 23, 25, 28, 29, 31	25, 26, 27, 29, 33, 34, 35			)) Internally connected: leave open circuit.))

Notes: I/P = Input
O/P = Output
BI = Bidirectional

1.4 External Components



Typical Values:

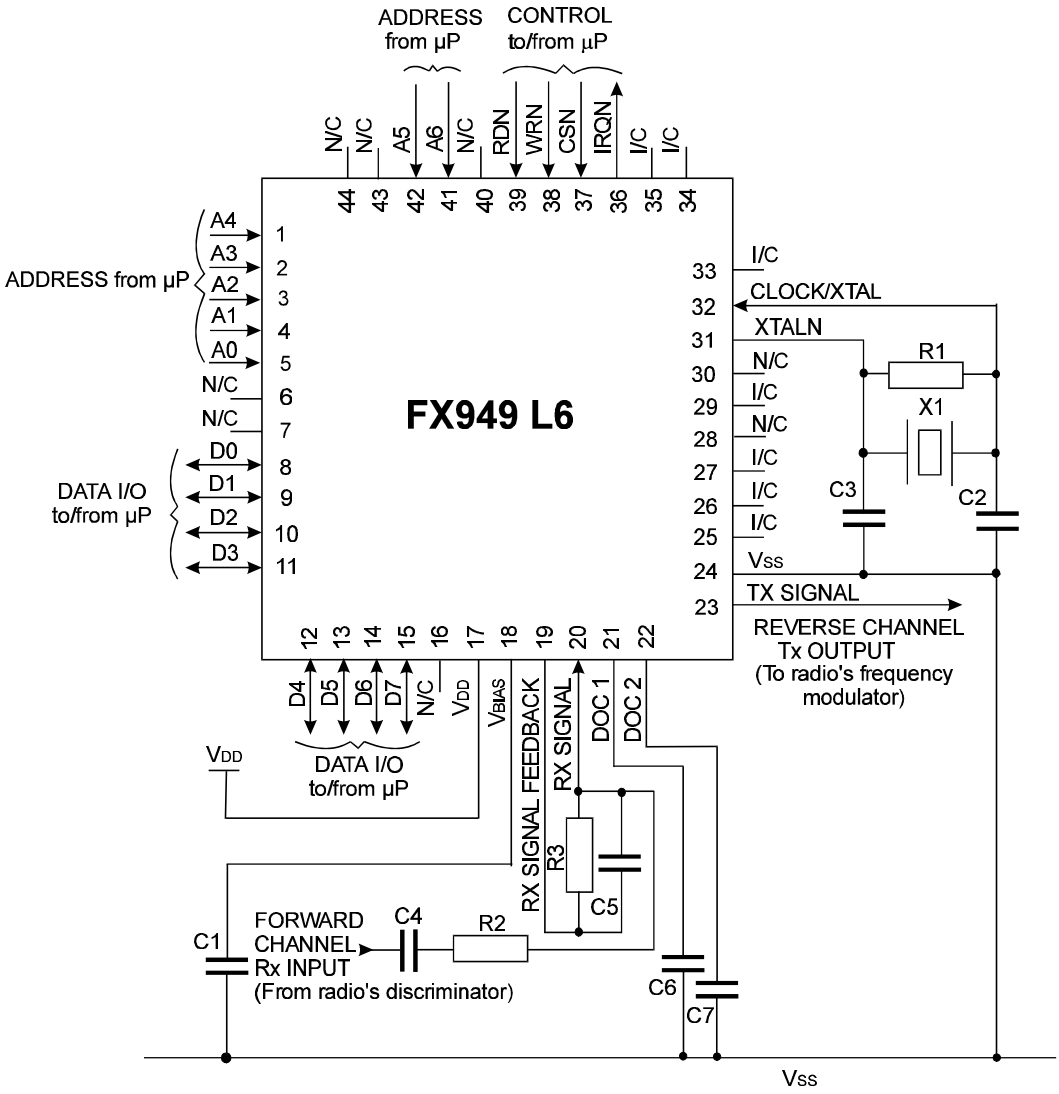
R1	1MΩ	+/− 5%	C1	1µF		X1 4.9152 MHz
R2	Note1	+/− 10%	C2	18pF		(ref. Section 1.7.1)
R3	100KΩ	+/− 10%	C3	18pF		
			C4	Note 1	+/− 20%	
			C5	100pF		
			C6	6.8nF		
			C7	6.8nF		

Notes:

1. R2, R3, C4 and C5 form the gain components for the Rx INPUT.
   R2 and C4 should be chosen as required by the signal input level, using the following formula:
   Gain = - R3/R2

2. Connections labelled 'N/C': No internal connection, do not use.
   Connections labelled 'I/C': Internally connected, leave open circuit.

Figure 2 Recommended External Components (L4)



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			C5	100pF	
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			C7	6.8nF	

Notes:

1. R2, R3, C4 and C5 form the gain components for the Rx INPUT. R2 and C4 should be chosen as required by the signal input level, using the following formula:

   Gain = - R3/R2

2. Connections labelled 'N/C': No internal connection, do not use.
   Connections labelled 'I/C': Internally connected, leave open circuit.

Figure 3 Recommended External Components (L6)

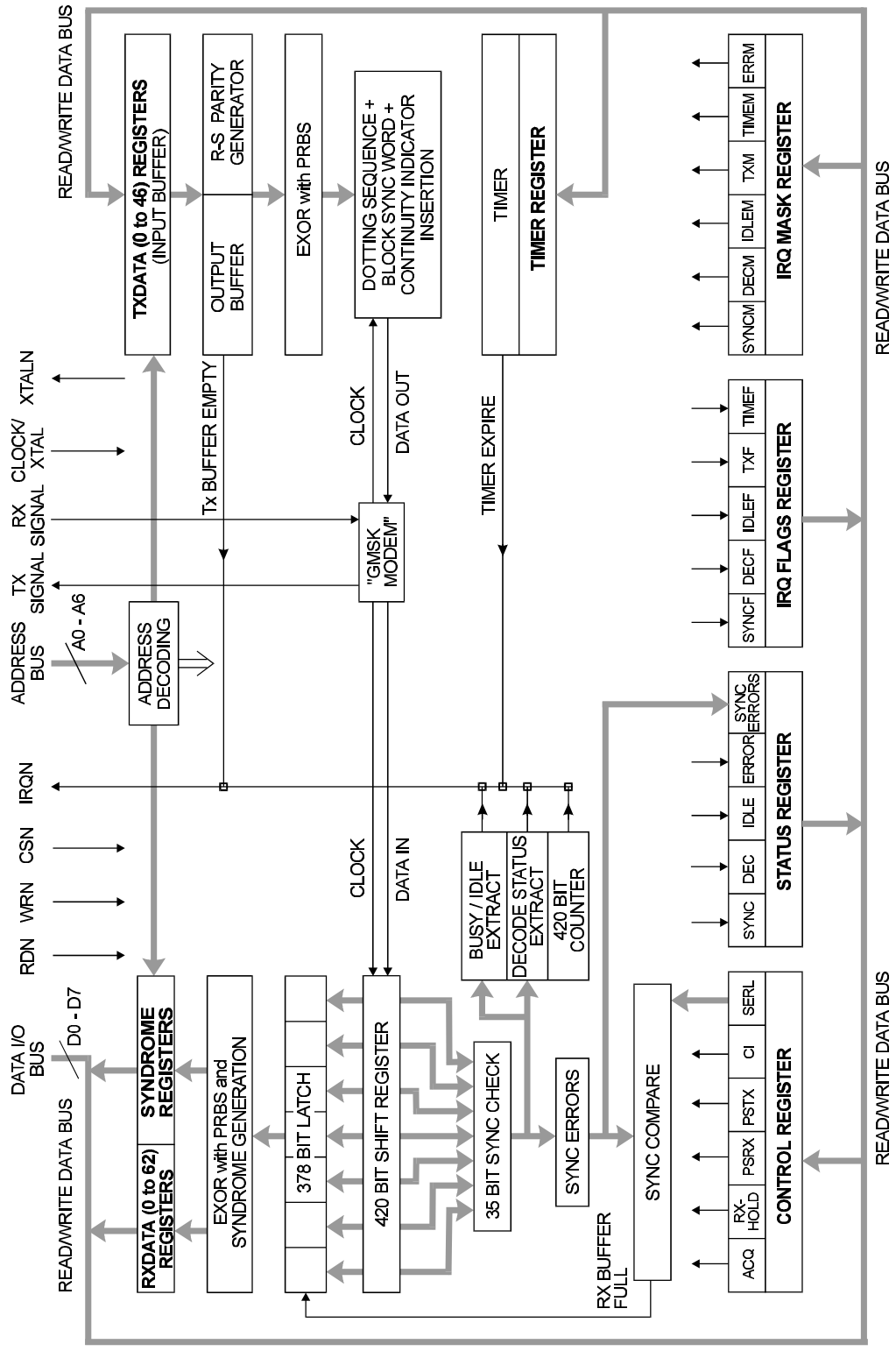


Figure 4 Internal Block Diagram

1.5 General Description

This device performs most of the Medium Access Control (MAC) layer functions of the CDPD specification as well as generation of the baseband signals in the physical layer, all of which are specifically for the Mobile End Station (M-ES). For details of the system requirements and telegram formats, the user is referred to "Cellular Digital Packet Data System Specification", Volumes 1 to 5, currently available from:

CDPD Forum Inc.
PO Box 809320
Chicago, IL 60686
United States of America

1.5.1 Software Description

From the programmer's viewpoint, the FX949 interface consists of a number of registers, addressable from a 7-bit bus with data supplied on a standard 8-bit µP bus, as shown in Figure 4.

Read Only Registers

A0 - A6 HEX ADDRESS	RDN	WRN	CSN	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$00	0	1	0	RX DATA 0	0	0	<---------- DATA SYMBOL 0 ---------->					
$01	0	1	0	RX DATA 1	0	0	<---------- DATA SYMBOL 1 ---------->					
$02	0	1	0	RX DATA 2	0	0	<---------- DATA SYMBOL 2 ---------->					
|				|			|					
|				|			|					
|				|			|					
|				|			|					
$3C	0	1	0	RX DATA 60	0	0	<---------- DATA SYMBOL 60 ---------->					
$3D	0	1	0	RX DATA 61	0	0	<---------- DATA SYMBOL 61 ---------->					
$3E	0	1	0	RX DATA 62	0	0	<---------- DATA SYMBOL 62 ---------->					
$3F	0	1	0	RX SYN 1	0	0	<-- SYNDROME SYMBOL 1 = [r (x) / (x + α^1)] -->					
$40	0	1	0	RX SYN 2	0	0	<-- SYNDROME SYMBOL 2 = [r (x) / (x + α^2)] -->					
$41	0	1	0	RX SYN 3	0	0	<-- SYNDROME SYMBOL 3 = [r (x) / (x + α^3)] -->					
$42	0	1	0	RX SYN 4	0	0	<-- SYNDROME SYMBOL 4 = [r (x) / (x + α^4)] -->					
$43	0	1	0	RX SYN 5	0	0	<-- SYNDROME SYMBOL 5 = [r (x) / (x + α^5)] -->					
$44	0	1	0	RX SYN 6	0	0	<-- SYNDROME SYMBOL 6 = [r (x) / (x + α^6)] -->					
$45	0	1	0	RX SYN 7	0	0	<-- SYNDROME SYMBOL 7 = [r (x) / (x + α^7)] -->					
$46	0	1	0	RX SYN 8	0	0	<-- SYNDROME SYMBOL 8 = [r (x) / (x + α^8)] -->					
$47	0	1	0	RX SYN 9	0	0	<-- SYNDROME SYMBOL 9 = [r (x) / (x + α^9)] -->					
$48	0	1	0	RX SYN 10	0	0	<-- SYNDROME SYMBOL 10 = [r (x) / (x + α^{10})] -->					

$49	0	1	0	RX SYN 11	0	0	<-- SYNDROME SYMBOL 11 = [r (x) / (x + α^{11})] -->					
$4A	0	1	0	RX SYN 12	0	0	<-- SYNDROME SYMBOL 12 = [r (x) / (x + α^{12})] -->					
$4B	0	1	0	RX SYN 13	0	0	<-- SYNDROME SYMBOL 13 = [r (x) / (x + α^{13})] -->					
$4C	0	1	0	RX SYN 14	0	0	<-- SYNDROME SYMBOL 14 = [r (x) / (x + α^{14})] -->					
$4D	0	1	0	RX SYN 15	0	0	<-- SYNDROME SYMBOL 15 = [r (x) / (x + α^{15})] -->					
$4E	0	1	0	RX SYN 16	0	0	<-- SYNDROME SYMBOL 16 = [r (x) / (x + α^{16})] -->					
$4F	0	1	0	STATUS	SYNC	DEC	IDLE	ERROR	0	<---- SYNC ERRORS--->		
$50	0	1	0	IRQ FLAGS	SYNCF	DECF	IDLEF	TXF	TIMEF	0	0	0

Read Only Register Description

RXDATA0 to RXDATA62 Registers (Hex address $00 to $3E)

These are read only registers and all 63 registers are each updated with 6-bit symbols every time a valid SYNC occurs. This is indicated by an interrupt (see SYNC, SYNC ERRORS, and SYNC ERROR LIMIT).

SYNDROME SYMBOL 1 to 16 (Hex address $3F to $4E)

These 16, 6-bit symbols contain the syndrome calculated from the received data (RXDATA 0 to 62). The syndrome is recalculated every time a valid SYNC occurs. An all zero pattern in the 16 syndrome symbols indicates zero errors in the data.

STATUS Register (Hex address $4F)

This is a read only register that contains the status of the various functions on the device as described below:

SYNC (Bit 7)
: This bit is set to "1" when a forward channel synchronisation word has been received successfully. (See SYNC ERRORS and SYNC ERROR LIMIT). This bit is reset to "0" when the sync word has not been detected for more than 420 bits (i.e. sync lost).

DEC (Bit 6)
: This bit indicates the decode status of the Mobile Data Base Station (MDBS) on the forward channel. This bit is set to "1" when the station fails to decode data successfully, and is reset to "0" when the station is successful in decoding data. This bit will only change and be valid if SYNC (Bit 7) is set to "1".

IDLE (Bit 5)
: This bit indicates the active status of the Mobile Data Base Station (MDBS) on the forward channel. This bit is set to "0" when the station is in an IDLE state, and reset to "1" when the station is in a BUSY state. This bit will only change and be valid if SYNC (Bit 7) is set to "1".

  The IDLE bit is derived from a majority decision on the five consecutive busy/idle bits, as in the CDPD specification.

  The first block of data received in the forward channel will not output any data until the sync word has been found. Once this has been found, the most recent (last) idle bit will be output in the STATUS register, and the IDLEF bit will be set to "1" in the IRQ FLAGS register.

  The next seven idle bits are output as they come in and, so long as the sync word remains correct, successive idle bits are output as they come in.

ERROR (Bit 4)
: This bit indicates if there are errors in RXDATA. This bit is set to "0" if all syndrome symbols (1 - 16) are "0", i.e. no errors in the data. This bit is set to "1" if any syndrome symbol is not "0", i.e. errors are present in the data. This bit is updated every time a valid SYNC occurs.

SYNC ERRORS (Bits 2, 1 and 0)
: This 3-bit number indicates the number of errors received in the synchronisation word. It is updated whenever the synchronisation word is in error less than or equal to the number specified by the SYNC ERROR LIMIT bits of the CONTROL register. It also implies the synchronisation word has been received successfully and sets the SYNC bit to "1" (See SYNC above).

IRQ FLAGS Register (Hex address $50)
This is a read only register that contains flags to indicate the source of an interrupt, as described below:

SYNCF (Bit 7) — This bit is set to "1" when the device has decoded the sync word on the forward channel. It also is set to "1" if, after detecting sync, it fails to detect it 420 bits later, indicating sync has been lost. The state of sync can be read from the STATUS register. This bit is reset to "0" after a "read" of the IRQ FLAGS register. When this bit is set to "1" an interrupt may be generated, depending on the state of the IRQ MASK register.

DECF (Bit 6) — This bit is set to "1" when the decode status of the Mobile Data Base Station (MDBS) in the forward channel changes state. The decode state can be read from the STATUS register. This bit is reset to "0" after a "read" of the IRQ FLAGS register. When this bit is set to "1" an interrupt may be generated depending on the state of the IRQ MASK register.

IDLEF (Bit 5) — This bit is set to "1" when the idle status of the Mobile Data Base Station (MDBS) in the forward channel changes state. The idle state can be read from the STATUS register. This bit is reset to "0" after a "read" of the IRQ FLAGS register. When this bit is set to "1" an interrupt may be generated depending on the state of the IRQ MASK register.

TXF (Bit 4) — This bit is used in transmission of data from the 47 symbol "write only" buffer on the reverse channel. This bit is set to "1" when the buffer is empty and new data can be loaded in. It is reset to "0" after a "read" of the IRQ FLAGS register. When this bit is set to "1" an interrupt may be generated depending on the state of the IRQ MASK register.

TIMEF (Bit 3) — This bit is set to "1" when the timer expires and it is reset after a "read" of the IRQ FLAGS register. When this bit is set to "1" an interrupt may be generated depending on the state of the IRQ MASK register.

Write Only Registers

A0 - A6 HEX ADDRESS	RDN	WRN	CSN	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$00	1	0	0	TX DATA 0	X	X	<---------- DATA SYMBOL 0 ---------->					
$01	1	0	0	TX DATA 1	X	X	<---------- DATA SYMBOL 1 ---------->					
$02	1	0	0	TX DATA 2	X	X	<---------- DATA SYMBOL 2 ---------->					
|				|			|					
|				|			|					
|				|			|					
|				|			|					
$2C	1	0	0	TX DATA 44	X	X	<---------- DATA SYMBOL 44 ---------->					
$2D	1	0	0	TX DATA 45	X	X	<---------- DATA SYMBOL 45 ---------->					
$2E	1	0	0	TX DATA 46	X	X	<---------- DATA SYMBOL 46 ---------->					
$2F	1	0	0	TIMER	<---------- 0 TO 255 SECONDS ---------->							
$30	1	0	0	CONTROL	ACQ	RX-HOLD	PSRX	PSTX	CI	<--SYNC ERROR LIMIT---> (SERL)		
$31	1	0	0	IRQ MASK	SYNCM	DECM	IDLEM	TXM	TIMEM	ERRM	0	0

Write Only Register Description

TXDATA0 to TXDATA46 Registers (Hex address $00 to $2E)

These 47 registers can be loaded with 6-bit symbols when the TXF bit in the IRQ FLAGS register is "1". On loading the 47th symbol, the device will generate the 16 symbol parity code and begin the transmit sequence. These registers are buffered, therefore after the TXF bit has gone to "1" there are 47 x 6 bit periods minus the time to generate the 16 parity symbols in which to load all registers, i.e. approximately 14 msec. The controlling µP has to re-load the buffer with new data within this time otherwise the old data will be sent again.

TIMER Register (Hex address $2F)

This register sets a timer to expire from 1 to 255 seconds ("0" disables and powersaves it). The time starts from when the register is first set and expires when the programmed time has passed. On expiry, the TIMEF bit is set in the IRQ FLAGS register and an interrupt may occur. The timer is 1-shot and does not restart until it is programmed again. After power up the TIMEF bit should be reset to "0" in order to initialise the timer.

CONTROL Register (Hex address $30)

This register is used to control the functions of the device as described below:

ACQ (Bit 7)	This bit controls the way in which the receiver locks onto the phase and amplitude of the incoming signal. When a carrier has been detected, this bit should be set high for at least 16 signal-bit periods, during which time the receiver measures the signal level (Fast Peak Detect) and sets its phase locked loop (PLL) bandwidth wide enough to lock to the received signal in less than 8 zero crossings. When the ACQ bit is returned low, level measurement enters the slower but more accurate Averaging Peak Detect mode; the PLL enters its medium bandwidth for about 30 signal-bit periods, after which time it will continue in its narrow bandwidth mode.
RXHOLD (Bit 6)	When this bit is set to "1" the receiver "bit synchronisation" PLL will lock. It can be used during times when the signal fades, so that when the signal returns the receiver is still very close to good "bit synchronisation". When this bit is set to "0", the device uses its normal PLL acquisition sequence for "bit synchronisation". When ACQ is high, the RXHOLD bit has no effect.
PSRX (Bit 5)	When this bit is "1" the receiver is powersaved. When this bit is "0" the receiver is enabled. After power up, this bit should be programmed to "1" in order to initialise the receiver.
PSTX (Bit 4)	When this bit is "1" the transmitter is powersaved. When this bit is "0" the transmitter is enabled. Transmission starts as soon as the PSTX bit goes to "0". Before that time, the CI bit and the TXDATA symbols should be set up for the first transmission. Transmission is terminated as soon as the PSTX bit goes to "1". After power up, this bit should be programmed to "1" in order to initialise the transmitter.
CI (Bit 3)	This bit sets the continuity indicator for transmission. It should be set to "1" when there are more blocks to follow and set to "0" when the last block begins. The first 47 symbol block transmitted after this bit has gone from "0" to "1" is preceded by the "dotting sequence" and the reverse synchronisation.

SYNC ERROR LIMIT (SERL) (Bits 2, 1 and 0)

This 3-bit number specifies the maximum number of bits that can be in error in the synchronisation word. When the synchronisation word is recognised with less than or equal to this number of errors the SYNCF bit is set to "1" and the actual number of errors is loaded into SYNC ERRORS. The RXDATA is then loaded into the registers for "Data Symbols 0 to 62", the Rx syndrome is updated, and an interrupt may be generated, depending on the state of the IRQ MASK register. If 5, 6 or 7 errors are programmed to be accepted in the SYNC ERROR LIMIT, falsing of the forward channel sync word may occur.

IRQ MASK Register (Hex address $31)

These bits prevent interrupts from occurring as detailed below:

SYNCM (Bit 7)

When this bit is set to "1" the SYNC interrupt will be gated out to the IRQN pin. When this bit is set to "0" the SYNC interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.

DECM (Bit 6)

When this bit is set to "1" the DEC interrupt will be gated out to the IRQN pin. When this bit is set to "0" the DEC interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.

IDLEM (Bit 5)

When this bit is set to "1" the IDLE interrupt will be gated out to the IRQN pin. When this bit is set to "0" the IDLE interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.

TXM (Bit 4)

When this bit is set to "1" the Tx interrupt will be gated out to the IRQN pin. When this bit is set to "0" the Tx interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.

TIMERM (Bit 3)

When this bit is set to "1" the TIMER interrupt will be gated out to the IRQN pin. After this bit is set to "0" the TIMER interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.

ERRM (Bit 2)

For systems that are required to work error free and where Reed-Solomon error correction is not implemented, this bit provides the means not to interrupt the controlling µP if errors are detected. When this bit is set to "1" all the interrupts will work as specified. When this bit is set to "0", the SYNC, DEC and IDLE interrupts will be inhibited even if the on chip Reed-Solomon error detector indicates there are errors in the data, thus not wasting the controlling µP's time with interrupts for incorrect data.

1.6 Application Notes

Further information on Reed-Solomon codes may be found in "Error Control Coding" by S. Lin and D.J. Costello, published by Prentice Hall in 1983. The ISBN number is 0-13-283796-X.

The operation of the FX949 can be split into 3 sections: the Transmitter (reverse channel), the Receiver (forward channel) and the Timer. The operational sequence of each is described below, with reference to the internal block diagram, shown in Figure 4. Data and framing transmission structures are shown in Figure 5 for the reverse channel and in Figure 6 for the forward channel.

1.6.1 General

(1) After power up, enable or disable the interrupts by using the IRQ MASK register, depending on whether the IRQN signal or direct polling of the IRQ FLAGS register is being used.

(2) After power up, program PSRX (Bit 5 of the CONTROL register) to "1" to initialise the Rx circuitry, i.e:

reset the interrupts
reset SYNCF, DECF, IDLEF in the IRQ FLAGS register
reset SYNC, DEC, IDLE, ERROR, SYNC ERRORS in the STATUS register

All other Rx registers are not affected and will be in a random state after power up.

(3) After power up, program PSTX (Bit 4 of the CONTROL register) to "1" to initialise the Tx circuitry, i.e:

set TXF in the IRQ register to "1" to indicate that the Tx buffer is empty
set the interrupt IRQN, if enabled, to request Tx data from the controlling µP

1.6.2 Transmitter (reverse channel)

(1) After power up, a Tx interrupt is generated, if enabled, and TXF (Bit 4 of the IRQ FLAGS register) is set, indicating the output buffer is empty.

(2) The transmitter can now be enabled.

(3) CI (Bit 3 of the CONTROL register) should be set to "1" when there are more Tx blocks to follow and set to "0" for the last block. If there is only one block to be sent, i.e. the first block is the last block, then the CI bit should be pulsed from "0" to "1" to "0" to ensure that the dotting pattern and block sync are sent and that CI is set to "0" to indicate the presence of the last block, except just after powersave when the dotting sequence and block sync are added automatically.

(4) All 47 symbols (0 to 46) are loaded into the TXDATA registers from the controlling µP, finishing the load with the 47th symbol. This set of TXDATA registers is double buffered, therefore any previous data can be sent again by re-loading only symbol 46, i.e. loading symbol 46 indicates that data is ready to be sent.

(5) The loading of symbol 46 (as above [4]) triggers the generation of a Reed-Solomon 16 symbol parity code, based on symbols 0 to 46 in the input buffer.

(6) The transmitter will wait for the output buffer to become empty (if it is the first transmission it may already be empty). When this condition is met, data is transferred to the output buffer. At this point the data and C1 bit for that block have been defined and will not change whilst setting up for the next block to be sent.

(7) The data is EXORed with the pseudorandom sequence (PRBS) as it is transmitted. Once this is done, the output buffer will be empty and the TXF flag with interrupt will be generated, looping the control sequence back to the first step.

(8) The input buffer can be re-loaded while the transmitter is transmitting.

(9) The CI (continuity indicator) bit is automatically inserted every 9 symbols, during transmission.

(10) The 38 bit "dotting sequence" and 22 bit block synchronisation word are added if it is the first transmission after Tx powersave or if the CI bit has just previously gone from "0" to "1" indicating the start of a new transmission block.

(11) The signal generated has a data rate of 19.2k bits/sec and is filtered by a Gaussian filter with a BT of 0.5 in the transmit section of the GMSK modem.

1.6.3 Receiver (forward channel)

(1) The SYNC ERROR LIMIT (SERL) (Bits 2, 1 and 0 of the CONTROL register) is set from "0" to "7" as required by the application.

(2) The receiver is enabled using PSRX (Bit 5 of the CONTROL register).

(3) The receiver is now able to receive 19.2k bits/sec data via the receive section of the GMSK modem, comprising input filter, slicer and bit synchroniser.

(4) A continuous stream of data is fed into the receiver input shift register.

(5) When the controlling µP receives a carrier detect, it can pulse ACQ (Bit 7 of the CONTROL register) in order to quickly acquire bit synchronisation. If carrier detect is not available or, due to powersave requirements, the controlling device remains unpowered, then slower bit synchronisation will be acquired in approximately 32 bits.

(6) The receiver input shift register is continually monitored for the 35-bit synchronisation word interleaved with the data. It correlates the number of errors in the synchronisation word with the maximum number allowed (previously programmed into the SYNC ERROR LIMIT bits of the CONTROL register). When it achieves this limit or less, valid data is assumed to be present.

(7) The data is EXORed with the pseudorandom sequence (PRBS) and a 16-symbol syndrome is generated. The data and syndrome are then loaded into the Rx output registers, ready for reading by the controlling µP.

(8) DEC (Bit 6) and IDLE (Bit 5) of the STATUS register are set according to the data received.

(9) SYNCF (Bit 7 of the IRQ FLAGS register) is set and an IRQ is generated. SYNC (Bit 7 of the STATUS register) is set to "1". This indicates that a new block of data has successfully been received and is available for reading by the controlling µP.

(10) With the first block sync received, the device now checks the DEC and IDLE positions in the next block of data and outputs them with interrupts as they are counted in.

(11) On-chip circuitry predicts when the next block sync will arrive. If it arrives before that time, the circuit is reset and the sequence loops back to step (6). If the time expires, the SYNCF and IRQ signals will be generated and SYNC (Bit 7 of the STATUS register) will be set to "0", indicating that block sync has been lost and DEC, IDLE and RXDATA are no longer valid.

1.6.4 Timer

(1) The IRQ FLAGS register is read, to reset TIMEF (Bit 3).

(2) The TIMER register is programmed with the time required, from 1 to 255 seconds, starting the time-out.

(3) IRQ and TIMEF are set when time expires.

(4) This timer can be used to implement the "sleep mode", as described in the CDPD specification.

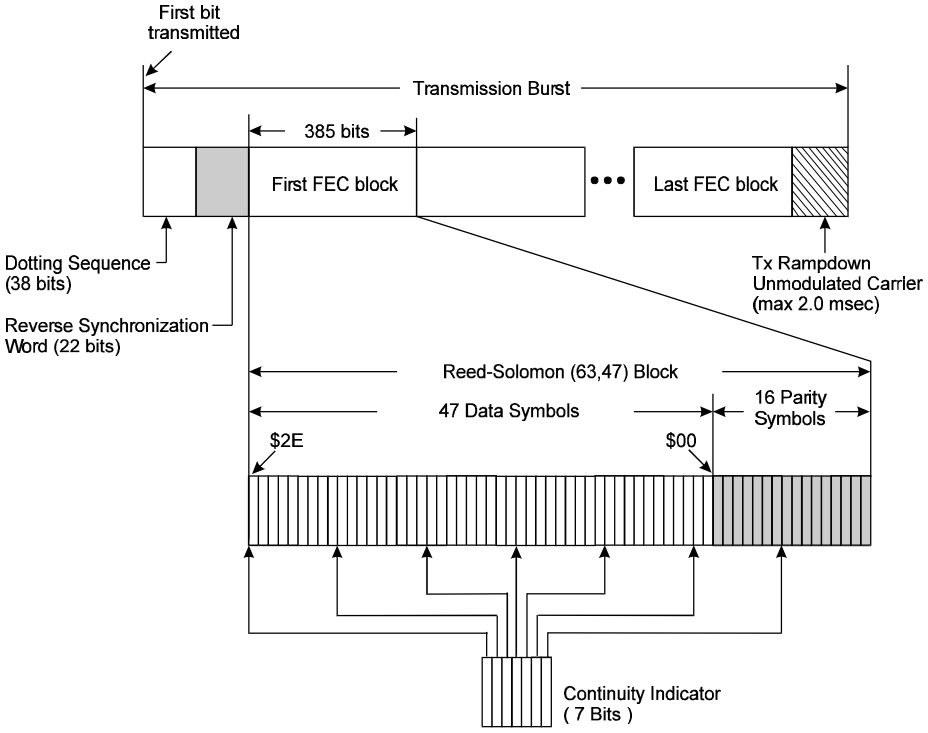


Figure 5 Reverse Channel Transmission Structure

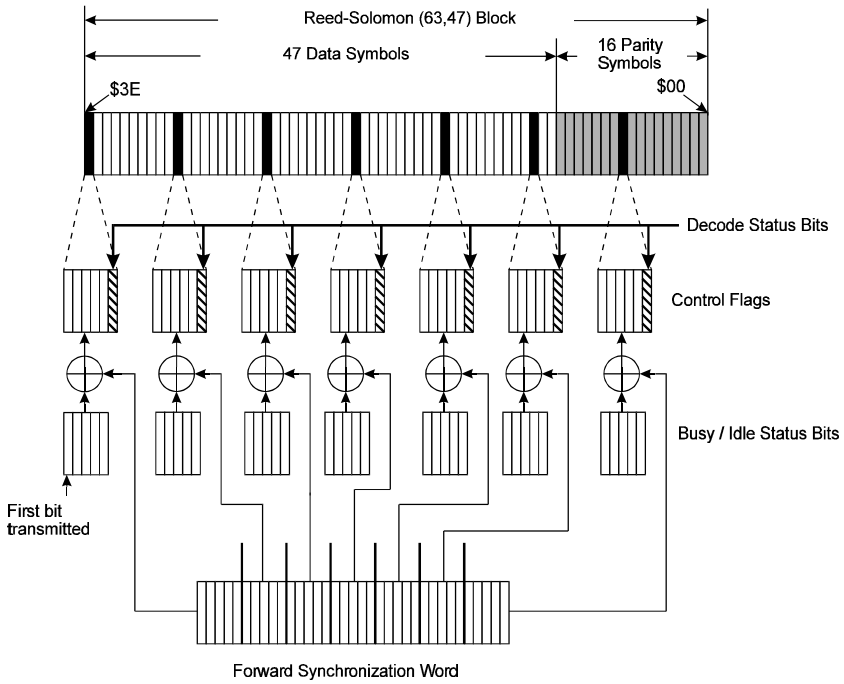


Figure 6 Forward Channel Transmission Structure

1.7 Performance Specification

1.7.1 Electrical Performance

Absolute Maximum Ratings
Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin (wrt V_{SS})	-0.3	V_{DD} + 0.3	V
Current into or out of V_{DD} and V_{SS} pins	-30	+30	mA
Current into or out of any other pin	-20	+20	mA
Storage Temperature	-40	+85	°C
Operating Temperature	-40	+85	°C
L4 Package			
Total Allowable Power Dissipation at Tamb = 25°C		550	mW
... Derating		9	mW/°C
L6 Package			
Total Allowable Power Dissipation at Tamb = 25°C		800	mW
... Derating		13	mW/°C

Operating Limits
Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Operating Temperature		-40	+85	°C
Xtal Frequency		4.9149	4.9155	MHz

Operating Characteristics
For the following conditions unless otherwise specified:

Xtal Frequency = 4.9152MHz, Bit Rate = 19.2k bits/sec,
V_{DD} = 3.3V to 5.0V, Tamb = -40°C to +85°C.

		Notes	Min.	Typ.	Max.	Units
DC Parameters						
I_{DD} (powersaved)	(V_{DD} = 5.0V)	1, 10		1.3	2.0	mA
I_{DD} (all enabled)	(V_{DD} = 5.0V)	1, 10		5.0	7.0	mA
I_{DD} (powersaved)	(V_{DD} = 3.0V)	1, 10		0.5	1.0	mA
I_{DD} (all enabled)	(V_{DD} = 3.0V)	1, 10		2.0	3.0	mA
AC Parameters						
Tx Output						
Tx O/P Impedance (Tx enabled)		2		1.0	2.5	kΩ
Tx O/P Impedance (powersaved)		2	300	500		kΩ
Output Signal Level		7	0.9	1.0	1.1	Vpk-pk
Power up to Tx O/P Stable		8		3	5	bits
Rx Input						
Rx I/P Impedance (at 100Hz)			10			MΩ
Rx I/P Amp Voltage Gain (I/P = 1mVrms at 100Hz)				500		V/V
Input Signal Level		9	0.7	1.0	1.3	Vpk-pk
Xtal/Clock Input						
'High' Pulse Width		3	40			ns
'Low' Pulse Width		3	40			ns
Input Impedance (at 100Hz)			10			MΩ
Gain (I/P = 1mV rms at 100Hz)			20			dB
µP Interface						
Input Logic "1" Level		4, 5	70%			V_{DD}
Input Logic "0" Level		4, 5			30%	V_{DD}
Input Leakage Current (Vin = 0 to V_{DD})		4, 5	-5.0		+5.0	µA
Input Capacitance		4, 5		10.0		pF
Output Logic "1" Level (I_{OH} = 120µA)		5	90%			V_{DD}
Output Logic "0" Level (I_{OL} = 360µA)		5, 6			10%	V_{DD}
'Off' State Leakage Current (Vout = V_{DD})		6			10	µA

Notes:
1. Not including any current drawn from the modem pins by external circuitry.
2. Small signal impedance, at V_{DD} = 5.0V and Tamb = 25°C.
3. Timing for an external input to the CLOCK/XTAL pin.
4. WRN, RDN, CSN, A0 - A6 pins.
5. D0 - D7 pins.
6. IRQN pin.
7. For 1111000011110000.. bit sequence, at V_{DD} = 5.0V and Tamb = 25°C. (output level is proportional to V_{DD}).
8. Measured between setting PSTX to "'0" and TXSIGNAL becoming stable.
9. For optimum performance, measured at RX SIGNAL FEEDBACK pin, for a '...11110000...' bit sequence, at V_{DD} = 5.0V and Tamb = 25°C.
10. At Tamb = 25°C only.

1.7.1 **Electrical Performance** (continued)

Timing Diagrams

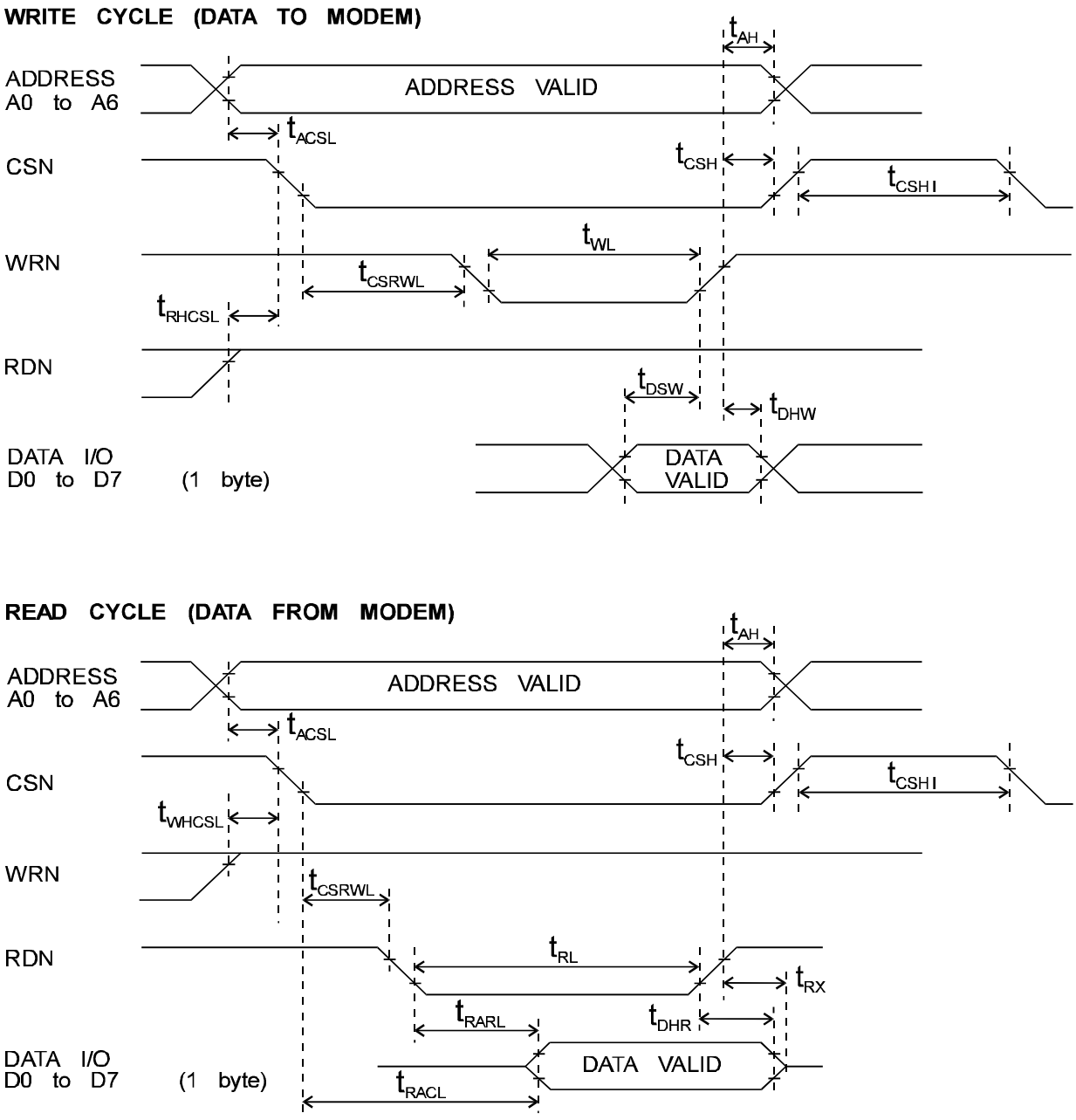


Figure 7 µP Interface Timings

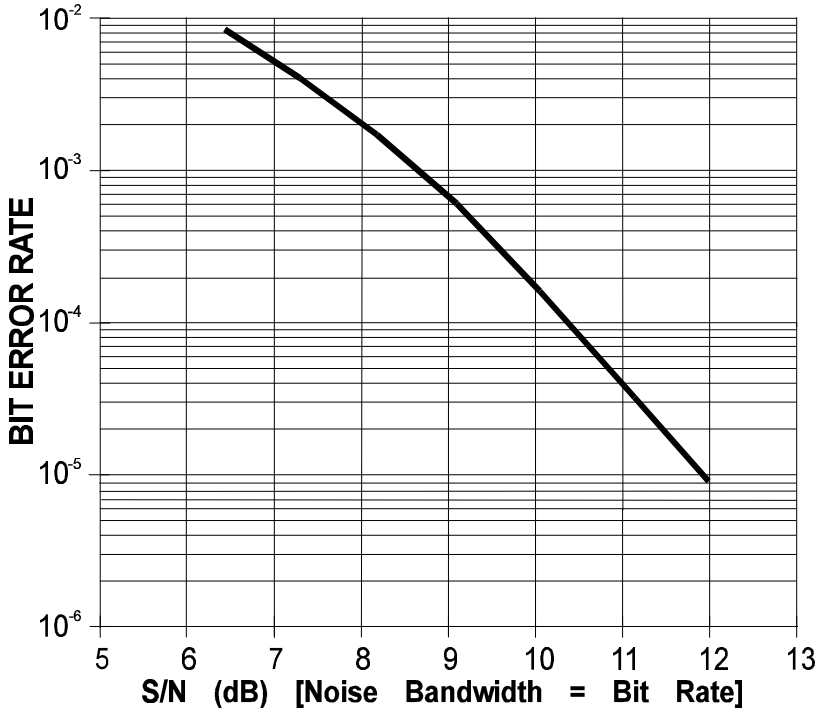
For the following conditions unless otherwise specified:

Xtal Frequency = 4.9152MHz, V_{DD} = 3.3V to 5.0V, Tamb = -40°C to +85°C.

		Notes	Min.	Typ.	Max.	Units
µP Interface Timings (ref. Fig. 7)						
t_{ACSL}	Address valid to CSN low time		0			ns
t_{AH}	Address hold time		10			ns
t_{CSH}	CSN hold time		0			ns
t_{CSHI}	CSN high time		6			clock cycles
t_{CSRWL}	CSN to WRN or RDN low time		0			ns
t_{DHR}	Read data hold time		0			ns
t_{DHW}	Write data hold time		0			ns
t_{DSW}	Write data setup time		90			ns
t_{RHCSL}	RDN high to CSN low time (write)		0			ns
t_{RACL}	Read access time from CSN low	11			175	ns
t_{RARL}	Read access time from RDN low	11			145	ns
t_{RL}	RDN low time		200			ns
t_{RX}	RDN high to D0 - D7 3-state time				50	ns
t_{WHCSL}	WRN high to CSN low time (read)		0			ns
t_{WL}	WRN low time		200			ns

Notes: 11. With 30pF max. to V_{SS} on D0 - D7 pins.

1.7.1 **Electrical Performance** (continued)

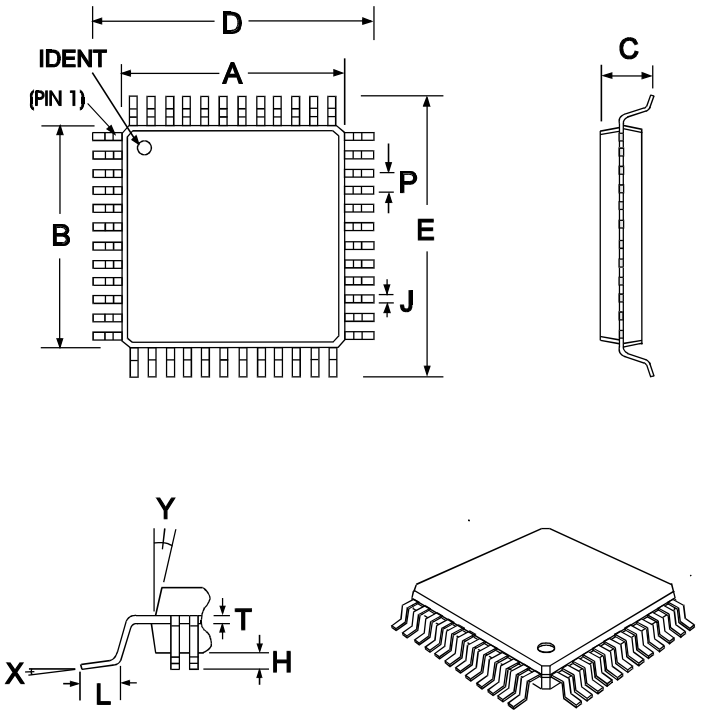


Note: This graph does not include the improvement in error rate that is achievable if error correction is included in the user's application software.

Figure 8 Typical Raw Bit Error Rate

for Xtal frequency = 4.9152MHz, V_{DD} = 5.0V, Tamb = 25°C

1.7.2 Packaging



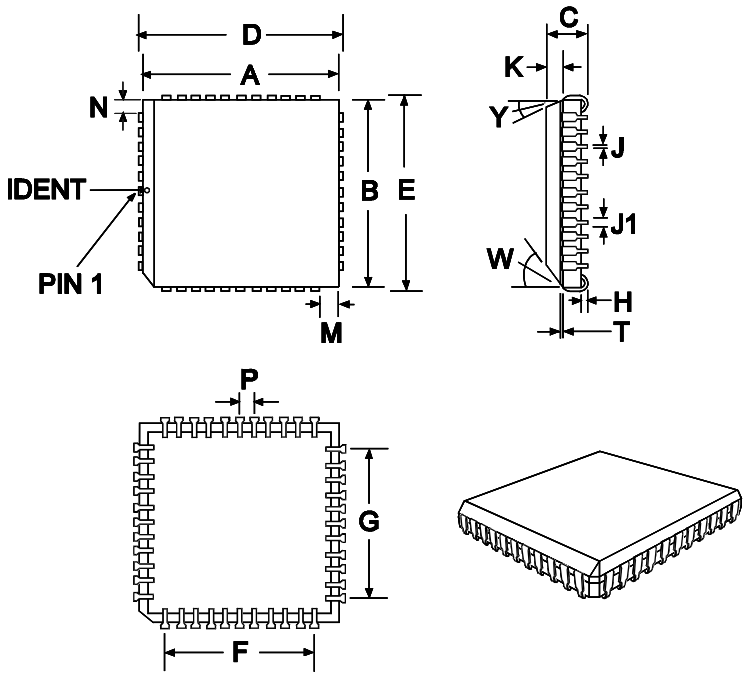
DIM.	MIN.	TYP.	MAX.
A	0.272 (6.90)		0.280 (7.10)
B	0.272 (6.90)		0.280 (7.10)
C			0.063 (1.60)
D	0.344 (8.75)		0.364 (9.25)
E	0.344 (8.75)		0.364 (9.25)
H	0.002 (0.05)		0.006 (0.15)
J	0.004 (0.11)		0.011 (0.27)
L	0.014 (0.35)		0.026 (0.66)
P		0.020 (0.50)	
T		0.005 (0.13)	
X	0°		7°
Y	11°		13°

NOTE : All dimensions in inches (mm.)

Angles in degrees

Lead coplanarity to be
0 to 0.003 (0.08) Max

Figure 9 TQFP Mechanical Outline: *Order as part no. FX949L4*



DIM.	MIN.	TYP.	MAX.
A	0.650 (16.51)		0.656 (16.66)
B	0.650 (16.51)		0.656 (16.66)
C			0.180 (4.57)
D	0.685 (17.40)		0.695 (17.65)
E	0.685 (17.40)		0.695 (17.65)
F		0.500 (12.7)	
G		0.500 (12.7)	
H	0.020 (0.51)		
J	0.013 (0.33)		0.021 (0.53)
J1		0.029 (0.74)	
K		0.070 (1.78)	
M		0.062 (1.57)	
N		0.062 (1.57)	
P		0.050 (1.27)	
T		0.010 (0.25)	
W		0.30 (7.62) x 45°	
Y		7°	

NOTE : All dimensions in inches (mm.)

Angles in degrees

Figure 10 PLCC Mechanical Outline: *Order as part no. FX949L6*

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