2W Stereo Audio Amplifier

Features

- **Depop Circuitry Integrated**
- **Output Power at 1% THD+N, VDD=5V**
  --1.8W/CH (typical) into a 4Ω Load
  --1.2W/CH (typical) into a 8Ω Load
- **Maximum Output Power Clamping Circuitry Integrated**
- **Bridge-Tied Load (BTL)**
- **Stereo Input MUX**
- **Mute and Shutdown Control Available**
- **Surface-Mount Power Package**
  24-Pin TSSOP-P & 24-Pin QFN Available

Applications

- **Stereo Power Amplifiers for Notebooks or Desktop Computers**
- **Multimedia Monitors**
- **Stereo Power Amplifiers for Portable Audio Systems**

General Description

The G1432 is a stereo audio power amplifier in 24pin TSSOP thermal pad package or 24pin QFN package. It can drive 1.8W continuous RMS power into 4Ω load per channel in Bridge-Tied Load (BTL) mode at 5V supply voltage. Its THD is smaller than 1% under the above operation condition. The G1432 can mute the output when Mute is activated. For the low current consumption applications, the SHDN mode is supported to disable the G1432 when it is idle. The current consumption can be further reduced to below 5μA.

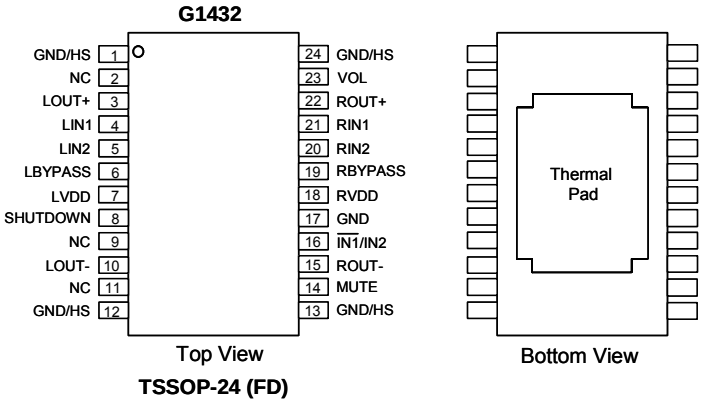
The G1432 also supports two input paths, that means two different gain loops can be set in the same PCB and choosing either one by setting $\overline{IN1}$/IN2 pin. It enhances the hardware designing flexibility. The G1432 also supports an extra function -- the maximum output power clamping function to protect the speakers from burned-out.

Ordering Information

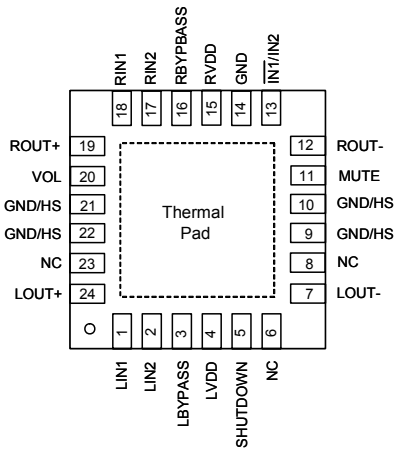
ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Pb free)
G1432F3U	G1432	-40°C to +85°C	TSSOP-24 (FD)
G1432Q5U	G1432	-40°C to +85°C	QFN4X4-24

Note: F3:TSSOP-24 (FD) Q5:QFN4X4-24
U: Tape & Reel

Pin Configuration



TSSOP-24 (FD)



G1432 QFN4X4-24

Note: Recommend connecting the Thermal Pad to the GND for excellent power dissipation.

Absolute Maximum Ratings

Supply Voltage, V_{DD} 6V
Input Voltage, V_I . . . . . -0.3V to V_{DD}+0.3V
Operating Ambient Temperature Range
T_A . . . . . -40°C to +85°C
Maximum Junction Temperature,
T_J . . . . . 150°C
Storage Temperature Range,
T_{STG} . . . . . .-65°C to+150°C
Reflow Temperature (soldering, 10sec) . . . . . 260°C

Power Dissipation [1]
TSSOP-24 (FD)
$T_A \le 25°C$ 2.7W
$T_A \le 70°C$ 1.7W
$T_A \le 85°C$ 1.4W
Electrostatic Discharge, V_{ESD}
Human body mode . . . . . .-3000 to 3000V[2]

Note:
[1]: Recommended PCB Layout.
[2]: Human body model : C = 100pF, R = 1500Ω, 3 positive pulses plus 3 negative pulses

Electrical Characteristics

DC Electrical Characteristics, T_A=+25°C

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNIT
Supply Current in Mute Mode	$I_{DD(MUTE)}$	V_{DD} =3.3V	Stereo BTL	---	7	13	mA
		V_{DD} = 5V	Stereo BTL	---	8	16	
DC Differential Output Voltage	$V_{O(DIFF)}$	V_{DD} = 5V,Gain = 2		---	5	50	mV
I_{DD} in Shutdown	I_{SD}	V_{DD} = 5V		---	2	5	µA

(AC Operation Characteristics, V_{DD} = 5.0V, T_A=+25°C, R_L = 4Ω, unless otherwise noted)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Output power (each channel) see Note	$P_{(OUT)}$	THD = 1%, BTL, R_L = 4Ω	---	1.8	---	W
		THD = 1%, BTL, R_L = 8Ω	---	1.2	---	
		THD = 10%, BTL, R_L = 4Ω	---	2	---	
		THD = 10%, BTL, R_L = 8Ω	---	1.4	---	
Total harmonic distortion plus noise	THD+N	P_O = 1.6W, BTL, R_L = 4Ω	---	500	---	m%
		P_O = 1W, BTL, R_L = 8Ω	---	150	---	
		V_I = 1V, RL = 10KΩ, G = 1	---	10	---	
Maximum output power bandwidth	B_{OM}	G = 1, THD =1%	---	20	---	kHz
Phase margin		R_L = 4Ω, Open Load	---	60	---	°
Power supply ripple rejection	PSRR	f = 120Hz	---	75	---	dB
Mute attenuation			---	85	---	dB
Channel-to-channel output separation		f = 1kHz	---	82	---	dB
$\overline{IN1}$/IN2 input separation			---	80	---	dB
Input impedance	ZI		---	2	---	MΩ
Signal-to-noise ratio		P_O = 500mW, BTL	---	90	---	dB
Output noise voltage	V_n	Output noise voltage	---	55	---	µV (rms)

Note :Output power is measured at the output terminals of the IC at 1kHz.

(AC Operation Characteristics, V_{DD} = 3.3V, T_A=+25°C, R_L = 4Ω, unless otherwise noted)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Output power (each channel) see Note	$P_{(OUT)}$	THD = 1%, BTL, R_L = 4Ω	---	0.8	---	W
		THD = 1%, BTL, R_L = 8Ω	---	0.5	---	
		THD = 10%, BTL, R_L = 4Ω	---	1	---	
		THD = 10%, BTL, R_L = 8Ω	---	0.6	---	
Total harmonic distortion plus noise	THD+N	P_O = 0.7W, BTL, R_L = 4Ω	---	270	---	m%
		P_O = 0.45W, BTL, R_L = 8Ω	---	100	---	
		V_I = 1V, RL = 10KΩ, G = 1	---	10	---	
Maximum output power bandwidth	B_{OM}	G = 1, THD 1%	---	20	---	kHz
Phase margin		R_L = 4Ω, Open Load	---	60	---	°
Power supply ripple rejection	PSRR	f = 120Hz	---	75	---	dB
Mute attenuation			---	85	---	dB
Channel-to-channel output separation		f = 1kHz	---	80	---	dB
$\overline{IN1}$/IN2 input separation			---	80	---	dB
Input impedance	ZI		---	2	---	MΩ
Signal-to-noise ratio		P_O = 500mW, BTL	---	90	---	dB
Output noise voltage	V_n	Output noise voltage	---	55	---	μV (rms)

Note : Output power is measured at the output terminals of the IC at 1kHz.

Typical Characteristics

Table of Graphs

			FIGURE
THD +N Total Harmonic Distortion Plus Noise		vs Output Power	1,3,6,9,10,13,16
		vs Frequency	2,4,5,7,8,11,12,14,15
V_n	Output Noise Voltage	vs Frequency	16,17
	Supply Ripple Rejection Ratio	vs Frequency	18,19
	Crosstalk	vs Frequency	20,21
	Closed loop Response	vs Frequency	22,23
I_{DD}	Supply Current	vs Supply Voltage	24
P_O	Output Power	vs Supply Voltage	25
		vs Load Resistance	26
P_D	Power Dissipation	vs Output Power	27,28

Total Harmonic Distortion Plus Noise vs Output Power

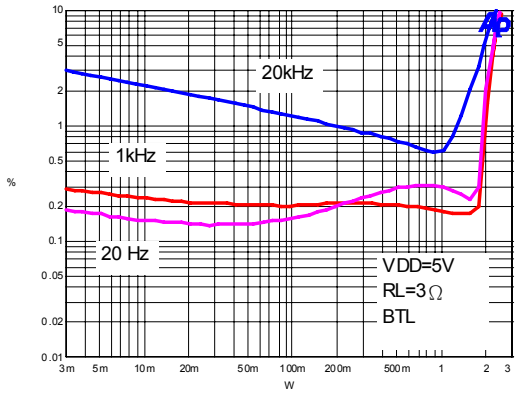


Figure 1

Total Harmonic Distortion Plus Noise vs Output Frequency

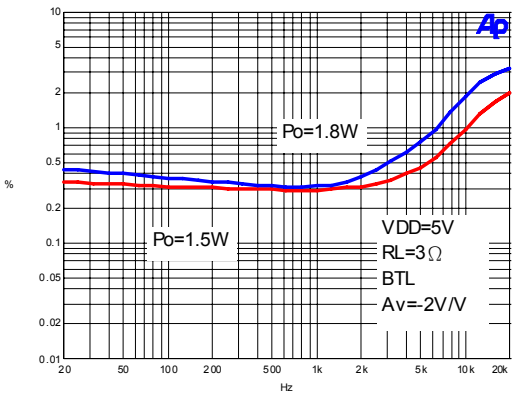


Figure 2

Total Harmonic Distortion Plus Noise vs Output Power

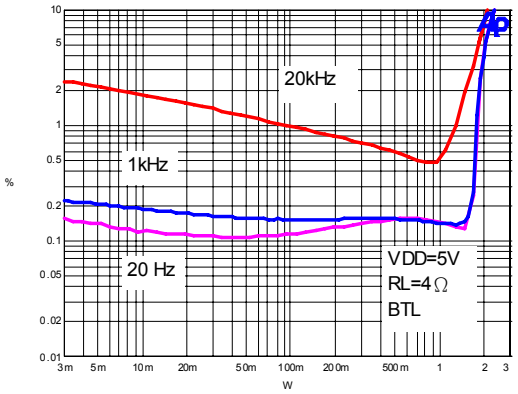


Figure 3

Total Harmonic Distortion Plus Noise vs Output Frequency

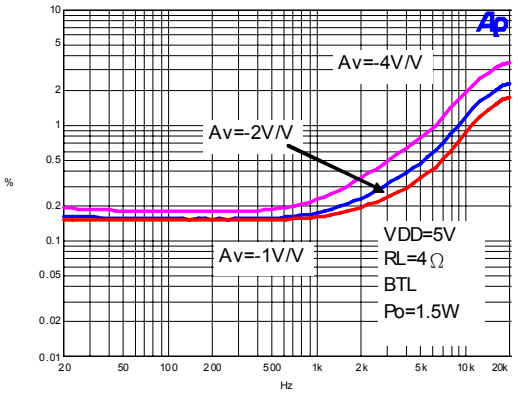


Figure 4

Total Harmonic Distortion Plus Noise vs Output Frequency

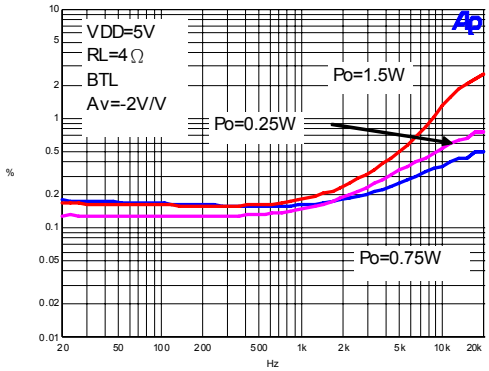


Figure 5

Total Harmonic Distortion Plus Noise vs Output Power

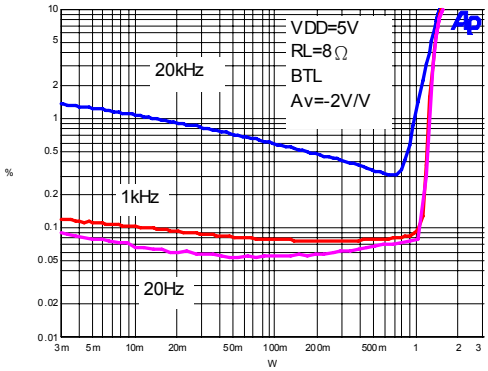


Figure 6

Total Harmonic Distortion Plus Noise vs Output Frequency

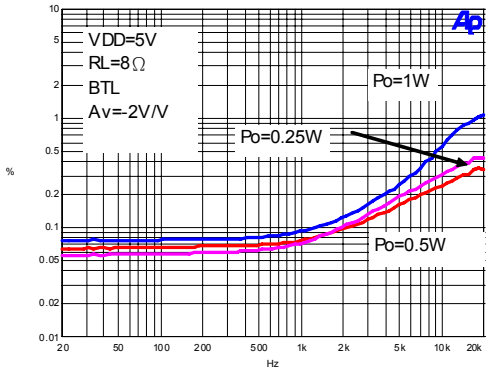


Figure 7

Total Harmonic Distortion Plus Noise vs Output Frequency

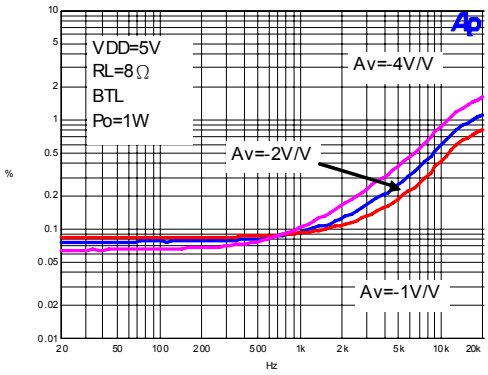


Figure 8

Total Harmonic Distortion Plus Noise vs Output Power

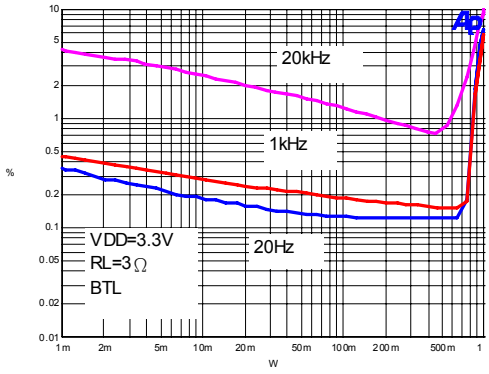


Figure 9

Total Harmonic Distortion Plus Noise vs Output Power

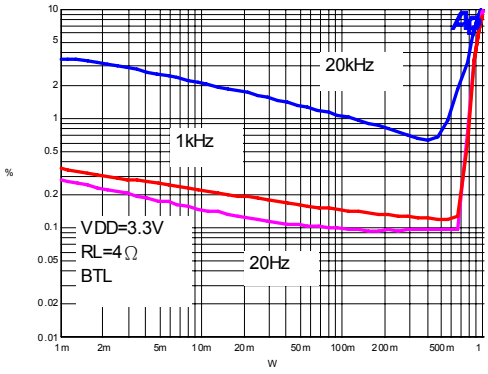


Figure 10

Total Harmonic Distortion Plus Noise vs Output Frequency

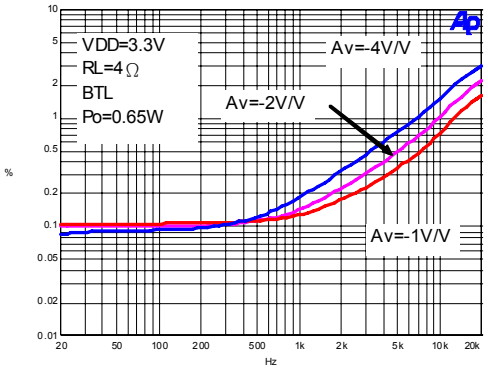


Figure 11

Total Harmonic Distortion Plus Noise vs Output Frequency

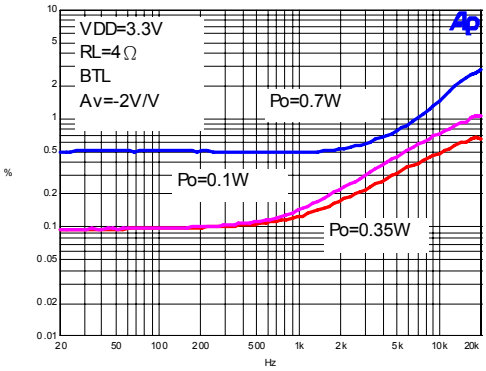


Figure 12

Total Harmonic Distortion Plus Noise vs Output Power

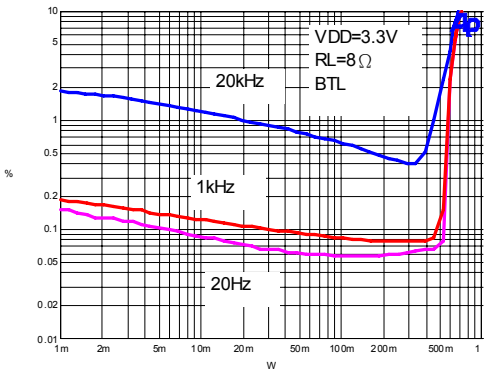


Figure 13

Total Harmonic Distortion Plus Noise vs Output Frequency

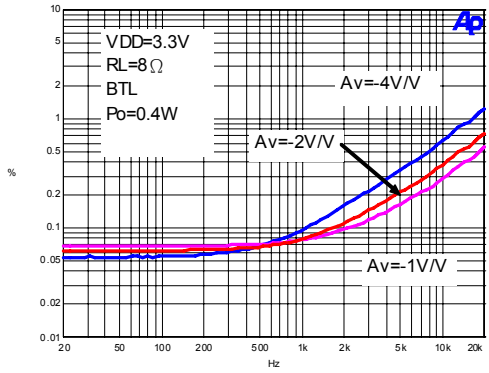


Figure 14

Total Harmonic Distortion Plus Noise vs Output Frequency

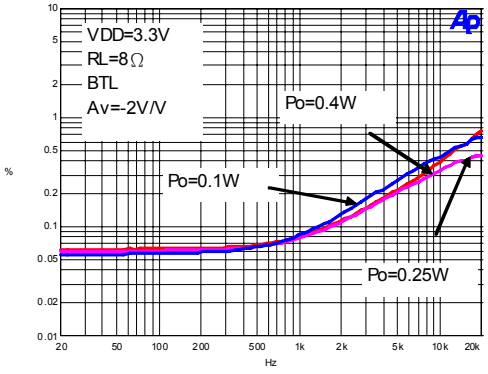


Figure 15

Output Noise Voltage vs Frequency

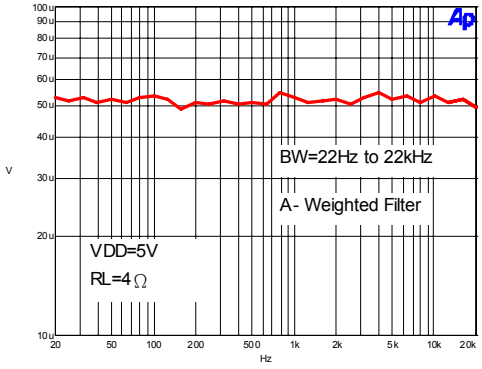


Figure 16

Output Noise Voltage vs Frequency

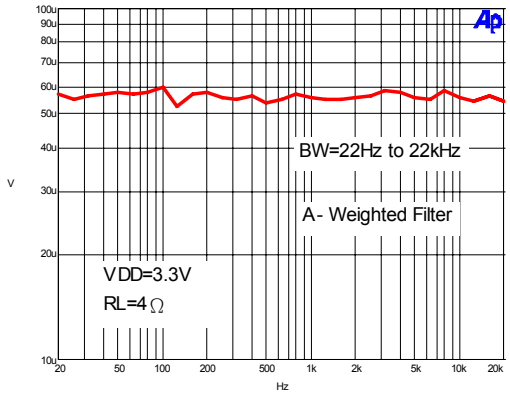


Figure 17

Supply Ripple Rejection Ratio vs Frequency

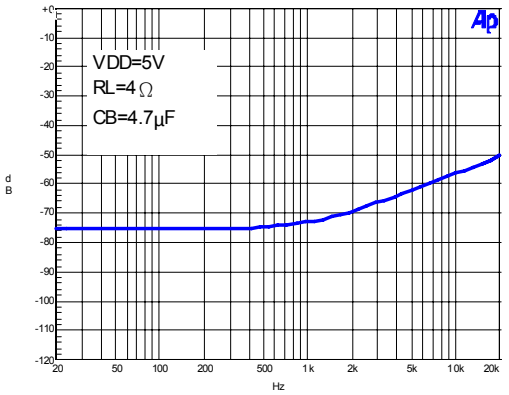


Figure 18

Supply Ripple Rejection Ratio vs Frequency

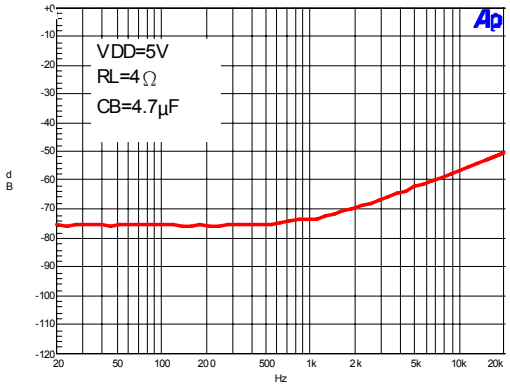


Figure 19

Crosstalk vs Frequency

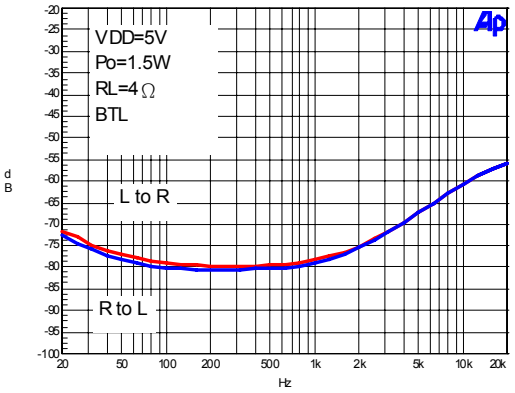


Figure 20

Crosstalk vs Frequency

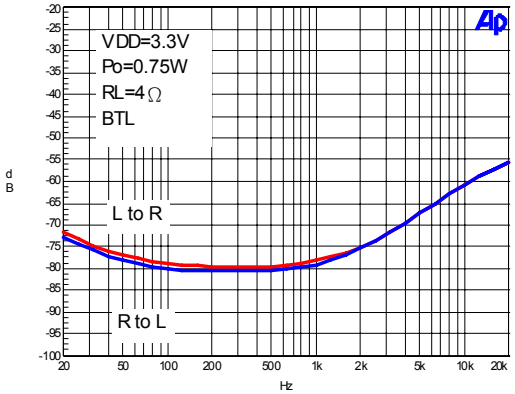


Figure 21

Closed Loop Response

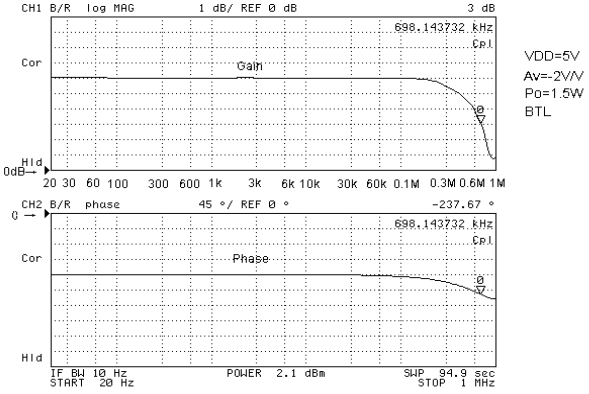


Figure 22

Closed Loop Response

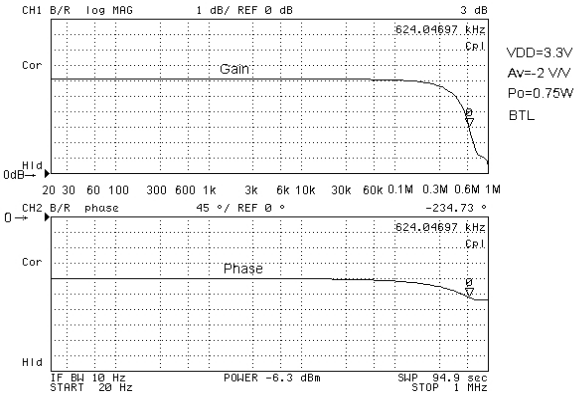


Figure 23

Supply Current vs Supply Voltage

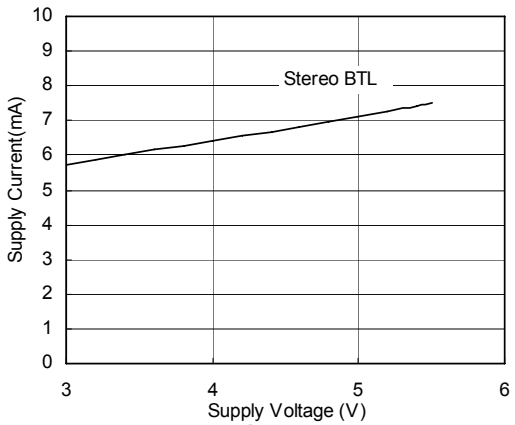


Figure 24

Output Power vs Supply Voltage

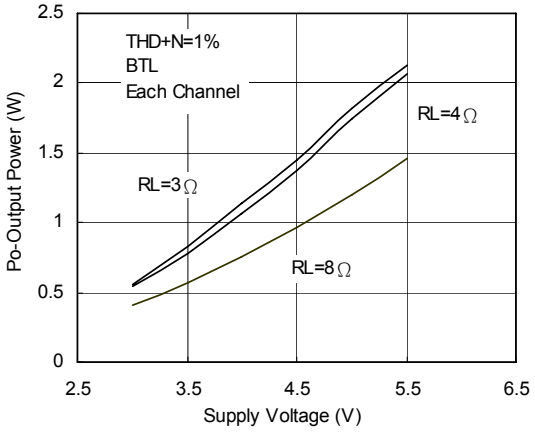


Figure 25

Output Power vs Load Resistance

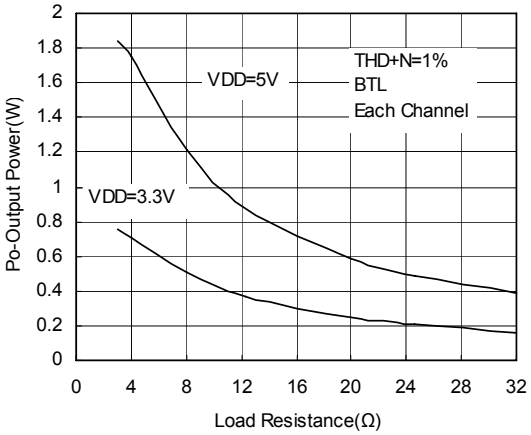


Figure 26

Power Dissipation vs Output Power

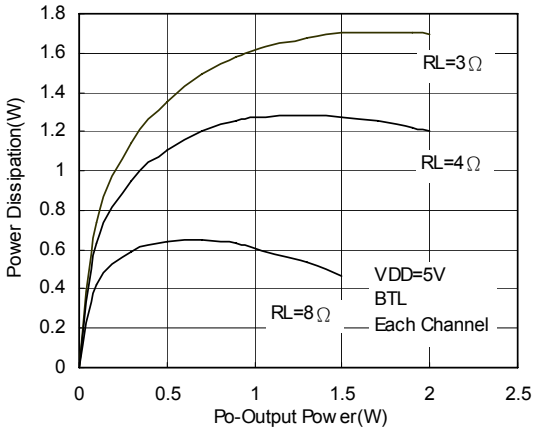


Figure 27

Power Dissipation vs Output Power

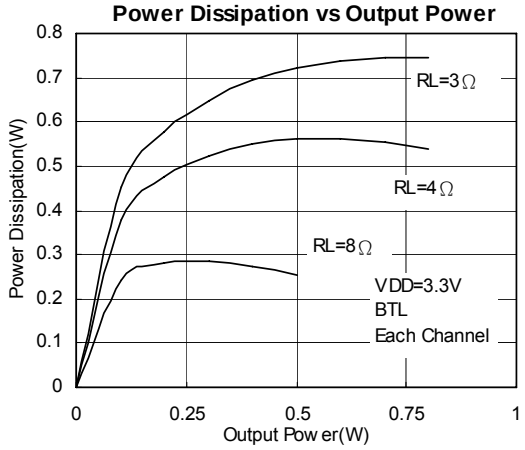


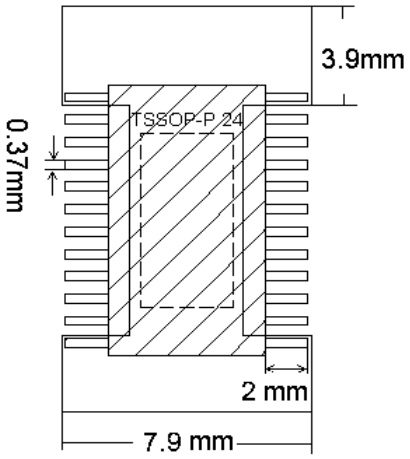
Figure 28

Pin Description

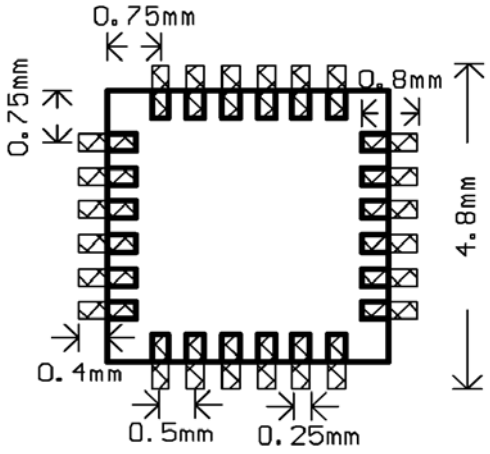
PIN		NAME	I/O	FUNCTION
TSSOP	QFN			
1,12,13,24	9,10,21,22	GND/HS		Ground connection for circuitry, directly connected to thermal pad.
2,9,11	6,8,23	NC	NC	Embedded test mode pin, please keep it floating.
3	24	LOUT+	O	Left channel + output in BTL mode
4	1	LIN1	I	Left channel IN1 input, selected when $\overline{IN1}$/IN2 pin is held low.
5	2	LIN2	I	Left channel IN2 input, selected when $\overline{IN1}$/IN2 pin is held high.
6	3	LBYPASS		Connect to voltage divider for left channel internal mid-supply bias.
7	4	LVDD	I	Supply voltage input for left channel and for primary bias circuits.
8	5	SHUTDOWN	I	Shutdown mode control signal input, places entire IC in shutdown mode when held high, I_{DD} < 5μA.
10	7	LOUT-	O	Left channel - output in BTL mode.
14	11	MUTE	I	Mode control signal input, hold low for activation, hold high for mute.
15	12	ROUT-	O	Right channel - output in BTL mode
16	13	$\overline{IN1}$/IN2	I	MUX control input, hold high to select in2 inputs (5,20)/(2/17), hold low to select in1 inputs (4,21)/(1,18).
17	14	GND		Ground connection for circuitry.
18	15	RVDD	I	Supply voltage input for right channel.
19	16	RBYPASS		Connect to voltage divider for right channel internal mid-supply bias.
20	17	RIN2	I	Right channel in2 input, selected when $\overline{IN1}$/IN2 pin is held high.
21	18	RIN1	I	Right channel lin1 input, selected when $\overline{IN1}$/IN2 pin is held low.
22	19	ROUT+	O	Right channel + output in BTL mode
23	20	VOL	I	The output power can be clamped by setting a low bound voltage to this pin. The high bound voltage will be generated internally. The output voltage will be clamped between high/low bound voltages. Then the output power is limited. It is weakly pull-low internally, let this pin floating or tied to GND can deactivate this function.
Thermal Pad	Thermal Pad			Recommend connecting the Thermal Pad to the GND for excellent power dissipation.

Recommended Minimum Footprint

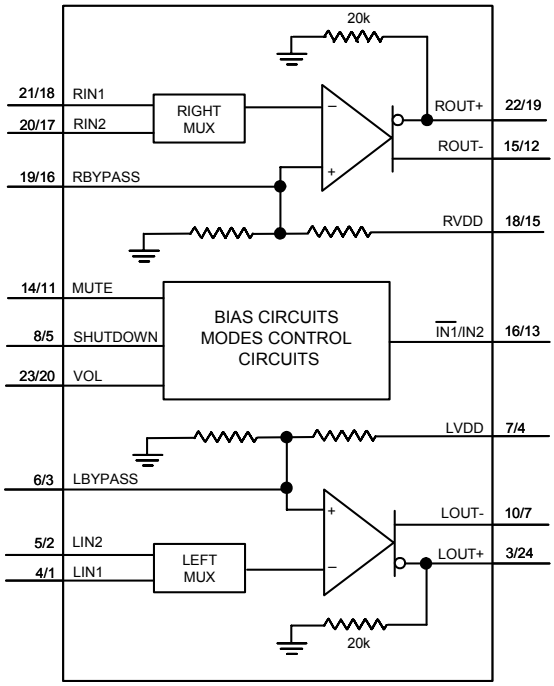
TSSOP-24 (FD)



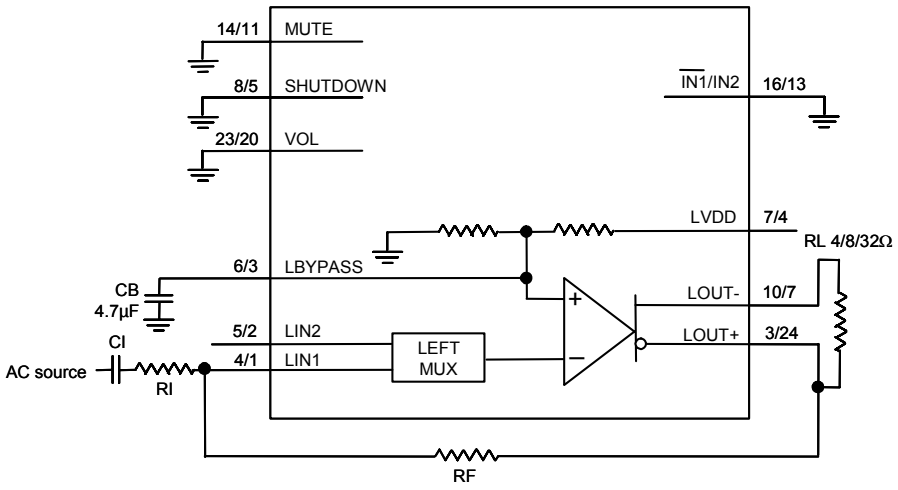
QFN4X4-24



Block Diagram
(TSSOP/QFN Pin No.)



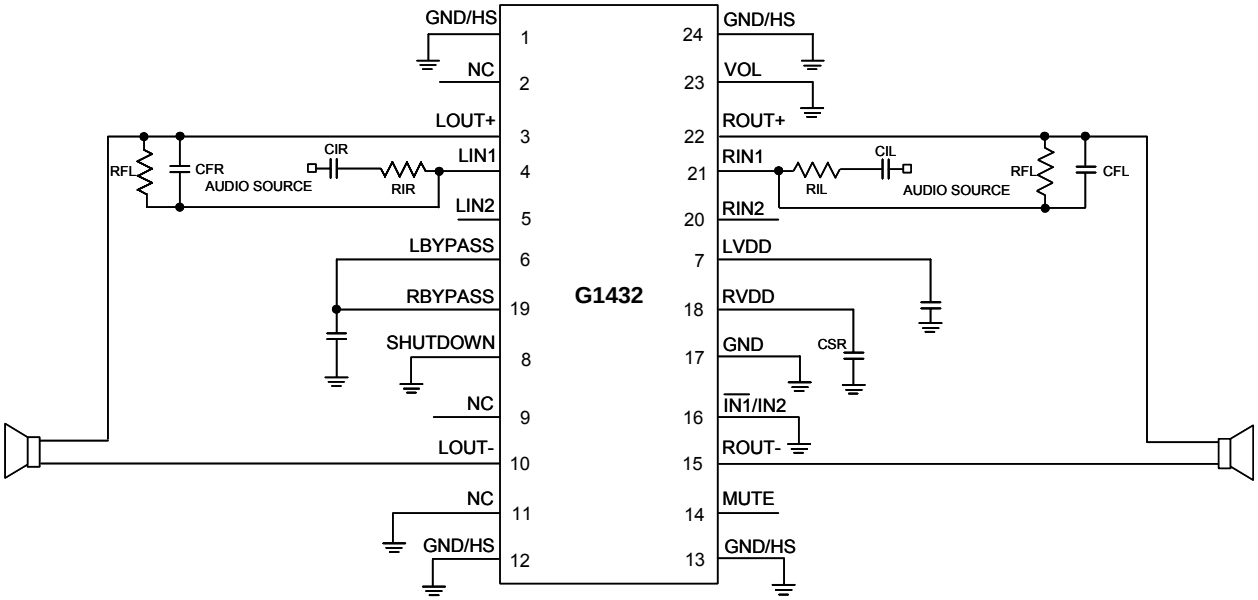
Parameter Measurement Information



BTL Mode Test Circuit

Application Circuits

(TSSOP-24)



Logical Truth Table

OUTPUT						
Mute	$\overline{IN1}$ /IN2	Shutdown	Input	L/R Out+	L/R Out-	Mode
X	X	High	X	----	----	Shutdown (Mute)
Low	Low	Low	L/R IN1	Output	Output	BTL
Low	High	Low	L/R IN2	Output	Output	BTL
High	Low	Low	L/R IN1	Output	----	Mute
High	High	Low	L/R IN2	Output	----	Mute

Application Information

(TSSOP-24/QFN4X4-24 Pin No.)

Input MUX Operation

There are two input signal paths – IN1 & IN2. With the prompt setting, the G1432 allows the setting of different gains for different input sources. If setting the $\overline{IN1}$ /IN2 pin low, the IN1 input source is selected. When setting the $\overline{IN1}$ /IN2 pin high, the IN2 input source is chosen.

Bridged-Tied Load Mode Operation

The G1432 has two linear amplifiers to drive both ends of the speaker load in Bridged-Tied Load (BTL) mode operation. Figure A shows the BTL configuration. The differential driving to the speaker load means that when one side is slewing up, the other side is slewing down, and vice versa. This configuration in effect will double the voltage swing on the load as compared to a ground reference load. In BTL mode, the peak-to-peak voltage V_O(PP) on the load will be two times than a ground reference configuration. The voltage on the load is doubled, this will also yield 4 times output power on the load at the same power supply rail and loading. Another benefit of using differential driving configuration is that BTL operation cancels the dc offsets, which eliminates the dc coupling capacitor that is needed to cancelled dc offsets in the ground reference configuration. Low-frequency performance is then limited only by the input network and speaker responses. Cost and PCB space can be minimized by eliminating the dc coupling capacitors.

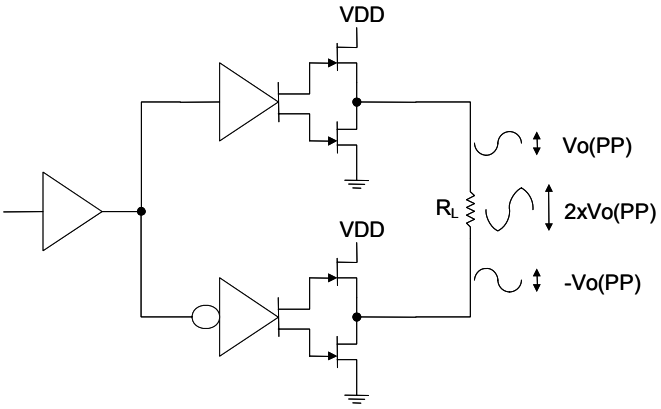


Figure A

MUTE and SHUTDOWN Mode Operations

The G1432 implements the mute and shutdown mode operations to reduce supply current, $I_{DD,}$ to the absolute minimum level during nonuse periods for battery-power conservation. When the shutdown pin (pin 8/5) is pulled high, all linear amplifiers will be deactivated to mute the amplifier outputs. And the G1432 enters an extra low current consumption state, I_{DD} is smaller than 5μA. If pulling the mute pin (pin 14/11) high, it will force the activated linear amplifier to supply the VDD/2 dc voltage on the output & shutdown the second linear amplifiers to mute the AC performance. In the mute mode operation, the current consumption will be a smaller than BTL modes. Shutdown and Mute pins should never be left unconnected, this floating condition will cause the amplifier operations unpredictable.

Maximum Power Clampping Function

The G1432 supports the maximum output power clamping function to avoid damaging the speaker when the amplifier output a power beyond the speaker tolerance. The Vol pin (pin 23/20) is weakly pull-low internally. If inputting a non-zero voltage (low boundary voltage) to the Vol pin, the G1432 will generate a high boundary voltage which the difference between the VDD/2 and the high boundary voltage is the same as the difference between the VDD/2 and the low boundary voltage. (i.e. V_{OH} – VDD/2 = VDD/2 – V_{OL}) Then the outputs of linear amplifiers will be effectively limited between the high/low boundary voltage, the maximum output power is clamped. By setting the voltage of Vol, the maximum output power can be well controlled. When the maximum power clamping function is not used, the Vol pin should be floated or tied to GND.

Optimizing DEPOP Operation

Circuitry has been implemented in the G1432 to minimize the amount of popping heard at power-up and when coming out of shutdown mode. Popping occurs whenever a voltage step is applied to the speaker and making the differential voltage generated at the two ends of the speaker. To avoid the popping heard, the bypass capacitor should be chosen promptly, $1/(C_B x 100k\Omega) \leqq 1/(C_I*(R_I+R_F))$. Where 100kΩ is the output impedance of the mid-rail generator, C_B is the mid-rail bypass capacitor, C_I is the input coupling capacitor, R_I is the input impedance, R_F is the gain setting impedance which is on the feedback path. C_B is the most important capacitor. Besides it is used to reduce the popping, C_B can also determine the rate at which the amplifier starts up during startup or recovery from shutdown mode.

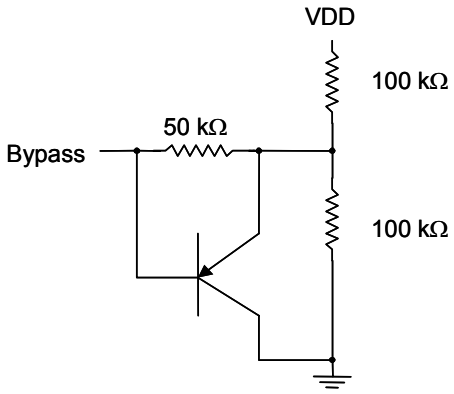
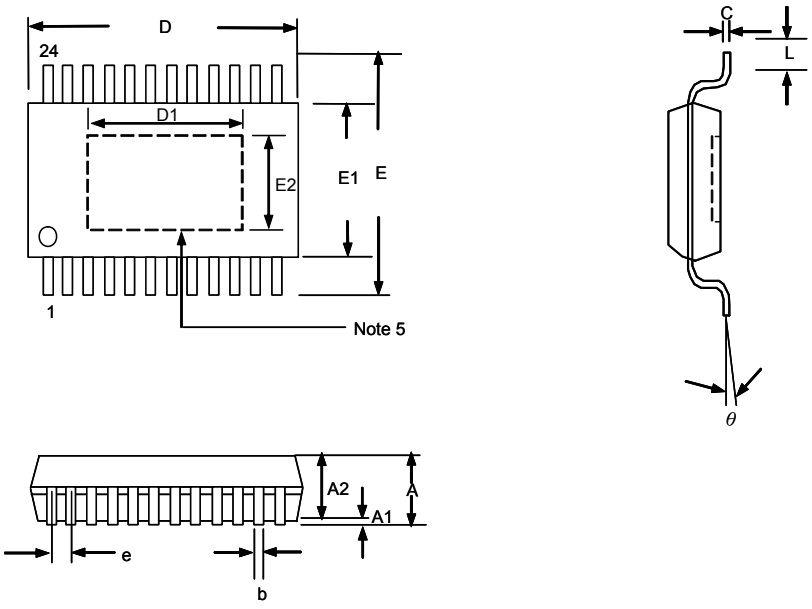


Figure B

De-popping circuitry of the G1432 is shown on Figure B. The PNP transistor limits the voltage drop across the 50kΩ by slewing the internal node slowly when power is applied. At start-up, the voltage at BYPASS capacitor is 0. The PNP is ON to pull the mid-point of the bias circuit down. So the capacitor sees a lower effective voltage, and thus the charging is slower. This appears as a linear ramp (while the PNP transistor is conducting), followed by the expected exponential ramp of an R-C circuit.

Package Information

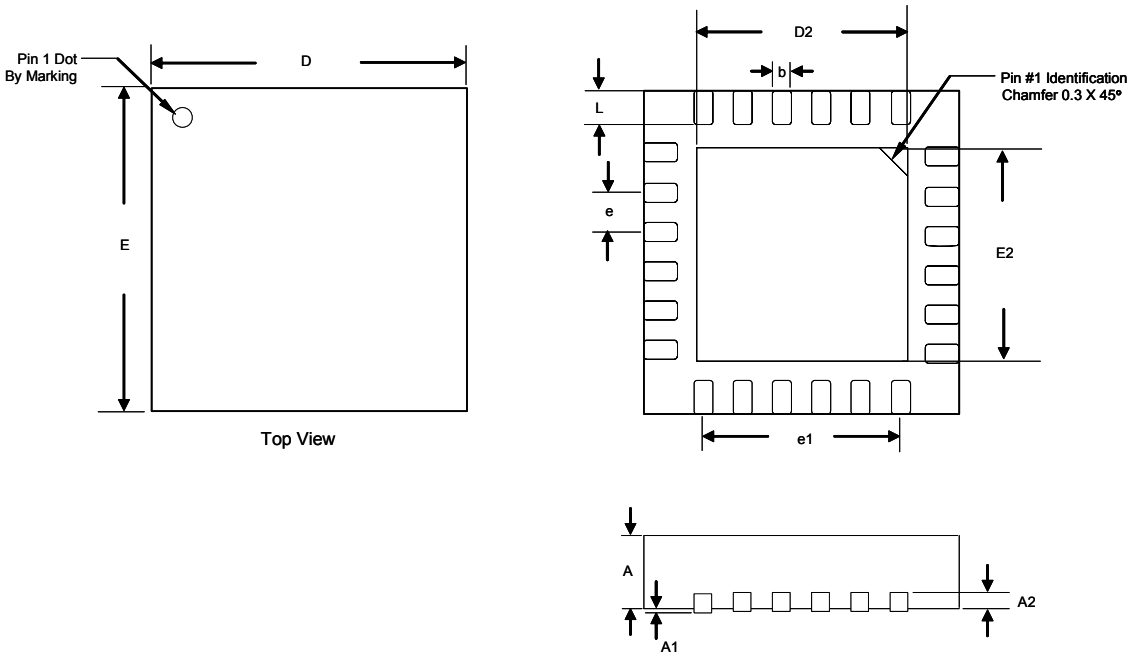


TSSOP-24 (FD) Package

NOTE:

1. Package body sizes exclude mold flash protrusions or gate burrs
2. Tolerance ±0.1mm unless otherwise specified
3. Coplanarity : 0.1mm
4. Controlling dimension is millimeter. Converted inch dimensions are not necessarily exact.
5. Die pad exposure size is according to lead frame design.
6. Follow JEDEC MO-153

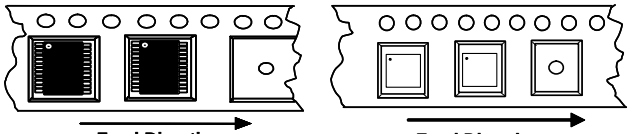
SYMBOLS	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-----	-----	1.20	-----	-----	0.047
A1	0.00	-----	0.15	0.000	-----	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	-----	0.30	0.007	-----	0.012
C	0.20	-----	-----	0.008	-----	-----
D	7.7	7.8	7.9	0.303	0.307	0.311
D1	4.4	-----	4.9	0.173	-----	0.193
E	6.40 BSC			0.252 BSC		
E1	4.30	4.40	4.50	0.169	0.173	0.177
E2	2.7	-----	3.2	0.106	-----	0.126
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
θ	0°	-----	8°	0°	-----	8°



QFN4X4-24 Package

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.700	-----	1.000	0.028	-----	0.039
A1	0.000	-----	0.050	0.000	-----	0.002
A2	0.178	0.203	0.228	0.007	0.008	0.009
b	0.225	0.250	0.275	0.009	0.010	0.011
D	3.950	4.000	4.050	0.156	0.157	0.159
D2	2.650	2.700	2.750	0.104	0.106	0.108
E	3.950	4.000	4.050	0.156	0.157	0.159
E2	2.650	2.700	2.750	0.104	0.106	0.108
e	0.500 BSC			0.020 BSC		
e1	2.500 REF			0.098 REF		
L	0.350	0.400	0.450	0.014	0.016	0.018

Taping Specification



Typical TSSOP Package Orientation **Typical QFN Package Orientation**

PACKAGE	Q'TY/REEL
TSSOP-24 (FD)	2,500 ea
QFN4X4-24	3,000 ea