

100-Pin TQFP
Commercial Temp
Industrial Temp

18Mb Pipelined and Flow Through Synchronous NBT SRAM

250 MHz–133 MHz
2.5 V or 3.3 V V_{DD}
2.5 V or 3.3 V I/O

Features

- User-configurable Pipeline and Flow Through mode
- NBT (No Bus Turn Around) functionality allows zero wait read-write-read bus utilization
- Fully pin-compatible with both pipelined and flow through NtRAM™, NoBL™ and ZBT™ SRAMs
- IEEE 1149.1 JTAG-compatible Boundary Scan
- 2.5 V or 3.3 V +10%/–10% core power supply
- $\overline{\text{LBO}}$ pin for Linear or Interleave Burst mode
- Pin-compatible with 2M, 4M, and 8M devices
- Byte write operation (9-bit Bytes)
- 3 chip enable signals for easy depth expansion
- ZZ pin for automatic power-down
- JEDEC-standard 100-lead TQFP and 165-bump FP-BGA packages

Functional Description

The GS8161Z18(T/D)/GS8161Z32(D)/GS8161Z36(T/D) is an 18Mbit Synchronous Static SRAM. GSI's NBT SRAMs, like ZBT, NtRAM, NoBL or other pipelined read/double late write or flow through read/single late write SRAMs, allow utilization of all available bus bandwidth by eliminating the need to insert deselect cycles when the device is switched from read to write cycles.

Because it is a synchronous device, address, data inputs, and read/write control inputs are captured on the rising edge of the input clock. Burst order control ($\overline{\text{LBO}}$) must be tied to a power rail for proper operation. Asynchronous inputs include the Sleep mode enable, ZZ and Output Enable. Output Enable can be used to override the synchronous control of the output drivers and turn the RAM's output drivers off at any time. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation required by asynchronous SRAMs and simplifies input signal timing.

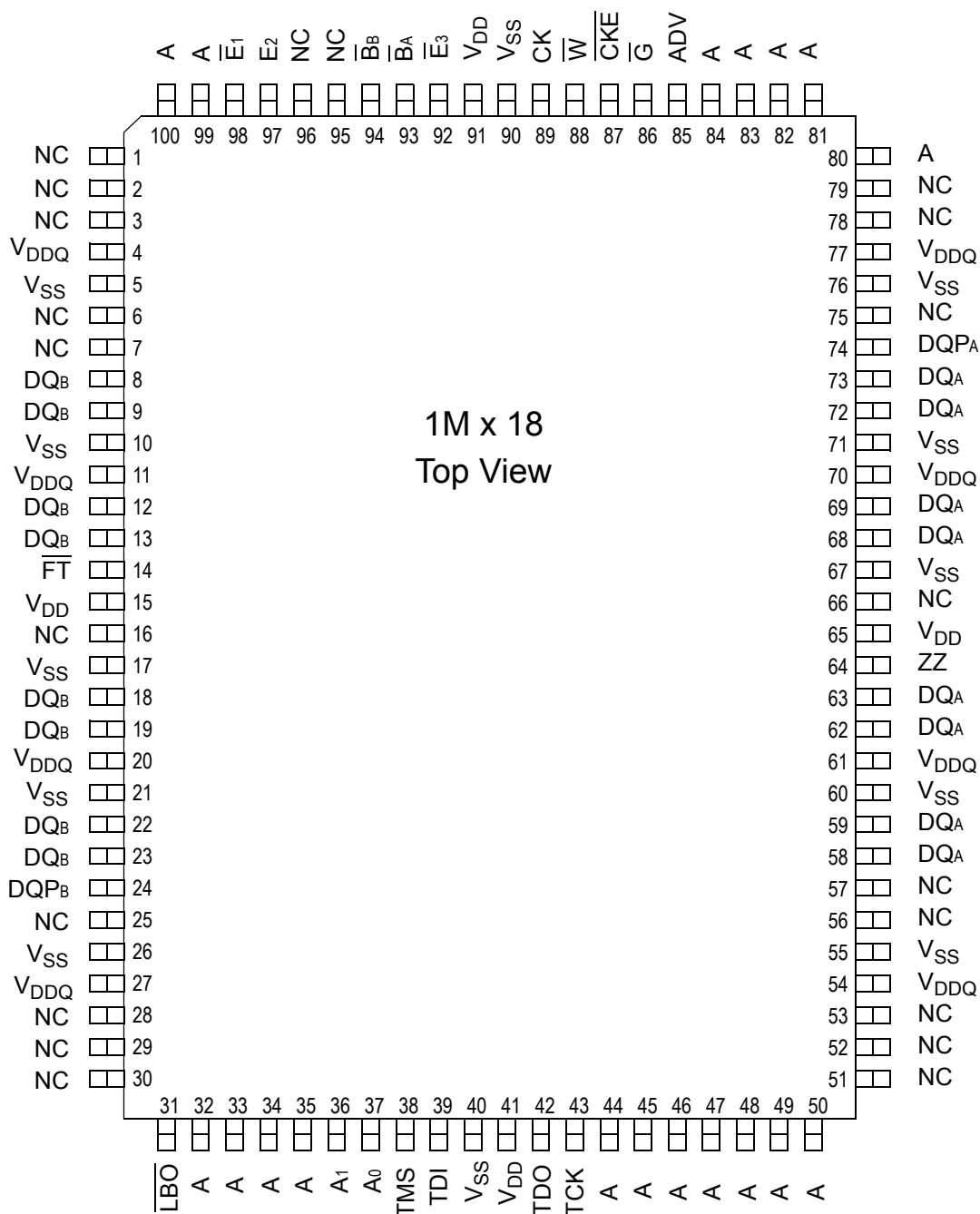
The GS8161Z18(T/D)/GS8161Z32(D)/GS8161Z36(T/D) may be configured by the user to operate in Pipeline or Flow Through mode. Operating as a pipelined synchronous device, in addition to the rising-edge-triggered registers that capture input signals, the device incorporates a rising-edge-triggered output register. For read cycles, pipelined SRAM output data is temporarily stored by the edge triggered output register during the access cycle and then released to the output drivers at the next rising edge of clock.

The GS8161Z18(T/D)/GS8161Z32(D)/GS8161Z36(T/D) is implemented with GSI's high performance CMOS technology and is available in JEDEC-standard 100-pin TQFP and 165-bump FP-BGA packages.

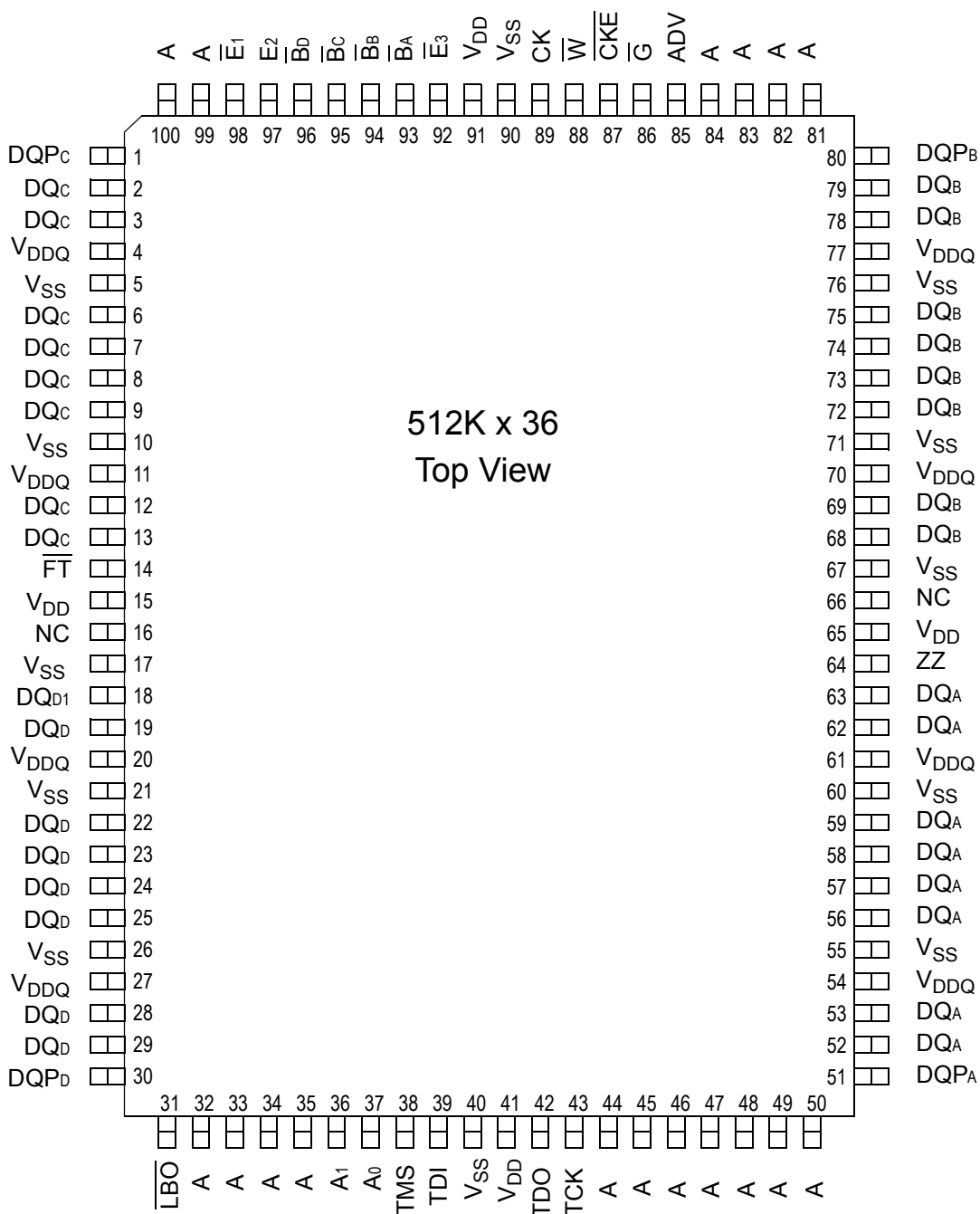
Parameter Synopsis

		-250	-225	-200	-166	-150	-133	Unit
Pipeline 3-1-1-1	t_{KQ}	2.5	2.7	3.0	3.4	3.8	4.0	ns
	t_{Cycle}	4.0	4.4	5.0	6.0	6.7	7.5	ns
3.3 V	Curr (x18)	280	255	230	200	185	165	mA
	Curr (x32/x36)	330	300	270	230	215	190	mA
2.5 V	Curr (x18)	275	250	230	195	180	165	mA
	Curr (x32/x36)	320	295	265	225	210	185	mA
Flow Through 2-1-1-1	t_{KQ}	5.5	6.0	6.5	7.0	7.5	8.5	ns
	t_{Cycle}	5.5	6.0	6.5	7.0	7.5	8.5	ns
3.3 V	Curr (x18)	175	165	160	150	145	135	mA
	Curr (x32/x36)	200	190	180	170	165	150	mA
2.5 V	Curr (x18)	175	165	160	150	145	135	mA
	Curr (x32/x36)	200	190	180	170	165	150	mA

GS8161Z18T Pinout (Package T)



GS8161Z36T Pinout (Package T)



100-Pin TQFP Pin Descriptions

Symbol	Type	Description
A ₀ , A ₁	In	Burst Address Inputs; Preload the burst counter
A	In	Address Inputs
CK	In	Clock Input Signal
$\overline{B_A}$	In	Byte Write signal for data inputs DQ _{A1} –DQ _{A9} ; active low
$\overline{B_B}$	In	Byte Write signal for data inputs DQ _{B1} –DQ _{B9} ; active low
$\overline{B_C}$	In	Byte Write signal for data inputs DQ _{C1} –DQ _{C9} ; active low
$\overline{B_D}$	In	Byte Write signal for data inputs DQ _{D1} –DQ _{D9} ; active low
$\overline{W}$	In	Write Enable; active low
$\overline{E_1}$	In	Chip Enable; active low
E ₂	In	Chip Enable—Active High. For self decoded depth expansion
$\overline{E_3}$	In	Chip Enable—Active Low. For self decoded depth expansion
$\overline{G}$	In	Output Enable; active low
ADV	In	Advance/Load; Burst address counter control pin
$\overline{CKE}$	In	Clock Input Buffer Enable; active low
NC	—	No Connect
DQ _A	I/O	Byte A Data Input and Output pins
DQ _B	I/O	Byte B Data Input and Output pins
DQ _C	I/O	Byte C Data Input and Output pins
DQ _D	I/O	Byte D Data Input and Output pins
TMS	I	Scan Test Mode Select
TDI	I	Scan Test Data In
TDO	O	Scan Test Data Out
TCK	I	Scan Test Clock
ZZ	In	Power down control; active high
$\overline{FT}$	In	Pipeline/Flow Through Mode Control; active low
$\overline{LBO}$	In	Linear Burst Order; active low.
V _{DD}	In	Core power supply
V _{SS}	In	Ground
V _{DDQ}	In	Output driver power supply

165 Bump BGA—x18 Commom I/O—Top View (Package D)

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	A	$\overline{E1}$	$\overline{BB}$	NC	$\overline{E3}$	$\overline{CKE}$	ADV	A	A	A	A
B	NC	A	E2	NC	$\overline{BA}$	CK	$\overline{W}$	$\overline{G}$	A	A	NC	B
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQPA	C
D	NC	DQB	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQA	D
E	NC	DQB	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQA	E
F	NC	DQB	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQA	F
G	NC	DQB	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQA	G
H	$\overline{FT}$	MCH	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ	H
J	DQB	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQA	NC	J
K	DQB	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQA	NC	K
L	DQB	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQA	NC	L
M	DQB	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQA	NC	M
N	DQPB	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	NC	N
P	NC	NC	A	A	TDI	A1	TDO	A	A	A	NC	P
R	$\overline{LBO}$	NC	A	A	TMS	A0	TCK	A	A	A	A	R

11 x 15 Bump BGA—13 mm x 15 mm Body—1.0 mm Bump Pitch

165 Bump BGA—x32 Common I/O—Top View (Package D)

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	A	$\overline{E1}$	$\overline{BC}$	$\overline{BB}$	$\overline{E3}$	$\overline{CKE}$	ADV	A	A	NC	A
B	NC	A	E2	$\overline{BD}$	$\overline{BA}$	CK	$\overline{W}$	$\overline{G}$	A	A	NC	B
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	C
D	DQC	DQC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQB	DQB	D
E	DQC	DQC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQB	DQB	E
F	DQC	DQC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQB	DQB	F
G	DQC	DQC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQB	DQB	G
H	$\overline{FT}$	MCH	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ	H
J	DQD	DQD	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQA	DQA	J
K	DQD	DQD	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQA	DQA	K
L	DQD	DQD	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQA	DQA	L
M	DQD	DQD	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQA	DQA	M
N	NC	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	NC	N
P	NC	NC	A	A	TDI	A1	TDO	A	A	A	NC	P
R	$\overline{LBO}$	NC	A	A	TMS	A0	TCK	A	A	A	A	R

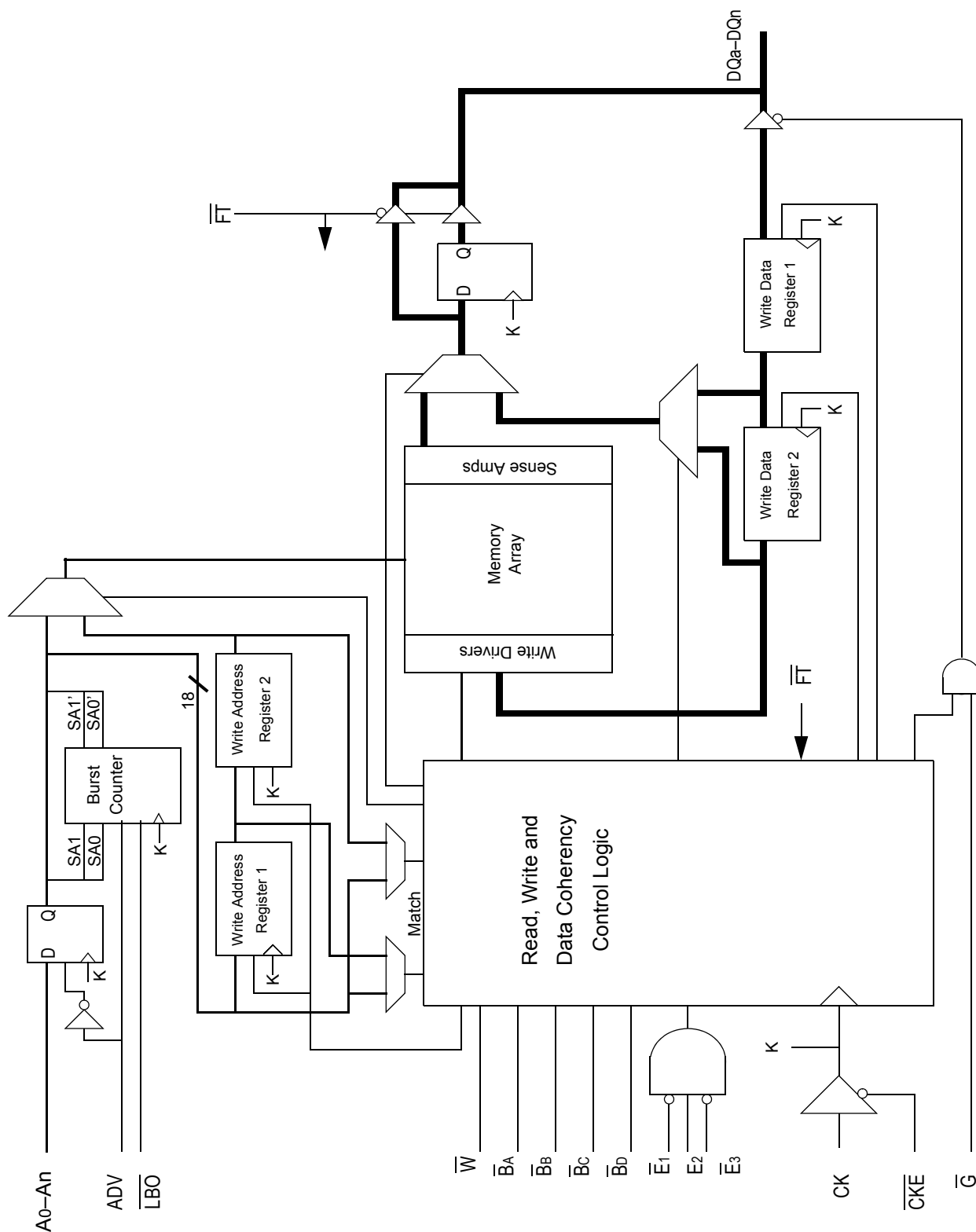
11 x 15 Bump BGA—13 mm x 15 mm Body—1.0 mm Bump Pitch

165 Bump BGA—x36 Common I/O—Top View (Package D)

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	A	$\overline{E1}$	$\overline{BC}$	$\overline{BB}$	$\overline{E3}$	$\overline{CKE}$	ADV	A	A	NC	A
B	NC	A	E2	$\overline{BD}$	$\overline{BA}$	CK	$\overline{W}$	$\overline{G}$	A	A	NC	B
C	DQPC	NC	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	NC	DQPB	C
D	DQC	DQC	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQB	DQB	D
E	DQC	DQC	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQB	DQB	E
F	DQC	DQC	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQB	DQB	F
G	DQC	DQC	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQB	DQB	G
H	$\overline{FT}$	MCH	NC	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	NC	NC	ZZ	H
J	DQD	DQD	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQA	DQA	J
K	DQD	DQD	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQA	DQA	K
L	DQD	DQD	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQA	DQA	L
M	DQD	DQD	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQA	DQA	M
N	DQPD	NC	V _{DDQ}	V _{SS}	NC	NC	NC	V _{SS}	V _{DDQ}	NC	DQPA	N
P	NC	NC	A	A	TDI	A1	TDO	A	A	A	NC	P
R	$\overline{LBO}$	NC	A	A	TMS	A0	TCK	A	A	A	A	R

11 x 15 Bump BGA—13 mm x 15 mm Body—1.0 mm Bump Pitch

GS8161Z18/32/36 NBT SRAM Functional Block Diagram



Functional Details

Clocking

Deassertion of the Clock Enable ($\overline{\text{CKE}}$) input blocks the Clock input from reaching the RAM's internal circuits. It may be used to suspend RAM operations. Failure to observe Clock Enable set-up or hold requirements will result in erratic operation.

Pipeline Mode Read and Write Operations

All inputs (with the exception of Output Enable, Linear Burst Order and Sleep) are synchronized to rising clock edges. Single cycle read and write operations must be initiated with the Advance/Load pin (ADV) held low, in order to load the new address. Device activation is accomplished by asserting all three of the Chip Enable inputs ($\overline{\text{E}}_1$, E_2 and $\overline{\text{E}}_3$). Deassertion of any one of the Enable inputs will deactivate the device.

Function	$\overline{\text{W}}$	$\overline{\text{B}}_A$	$\overline{\text{B}}_B$	$\overline{\text{B}}_C$	$\overline{\text{B}}_D$
Read	H	X	X	X	X
Write Byte "a"	L	L	H	H	H
Write Byte "b"	L	H	L	H	H
Write Byte "c"	L	H	H	L	H
Write Byte "d"	L	H	H	H	L
Write all Bytes	L	L	L	L	L
Write Abort/NOP	L	H	H	H	H

Read operation is initiated when the following conditions are satisfied at the rising edge of clock: $\overline{\text{CKE}}$ is asserted low, all three chip enables ($\overline{\text{E}}_1$, E_2 , and $\overline{\text{E}}_3$) are active, the write enable input signals $\overline{\text{W}}$ is deasserted high, and ADV is asserted low. The address presented to the address inputs is latched in to address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the next rising edge of clock the read data is allowed to propagate through the output register and onto the output pins.

Write operation occurs when the RAM is selected, CKE is active and the write input is sampled low at the rising edge of clock. The Byte Write Enable inputs ($\overline{\text{B}}_A$, $\overline{\text{B}}_B$, $\overline{\text{B}}_C$ & $\overline{\text{B}}_D$) determine which bytes will be written. All or none may be activated. A write cycle with no Byte Write inputs active is a no-op cycle. The pipelined NBT SRAM provides double late write functionality, matching the write command versus data pipeline length (2 cycles) to the read command versus data pipeline length (2 cycles). At the first rising edge of clock, Enable, Write, Byte Write(s), and Address are registered. The Data In associated with that address is required at the third rising edge of clock.

Flow Through Mode Read and Write Operations

Operation of the RAM in Flow Through mode is very similar to operations in Pipeline mode. Activation of a read cycle and the use of the Burst Address Counter is identical. In Flow Through mode the device may begin driving out new data immediately after new address are clocked into the RAM, rather than holding new data until the following (second) clock edge. Therefore, in Flow Through mode the read pipeline is one cycle shorter than in Pipeline mode.

Write operations are initiated in the same way, but differ in that the write pipeline is one cycle shorter as well, preserving the ability to turn the bus from reads to writes without inserting any dead cycles. While the pipelined NBT RAMs implement a double late write protocol, in Flow Through mode a single late write protocol mode is observed. Therefore, in Flow Through mode, address and control are registered on the first rising edge of clock and data in is required at the data input pins at the second rising edge of clock.

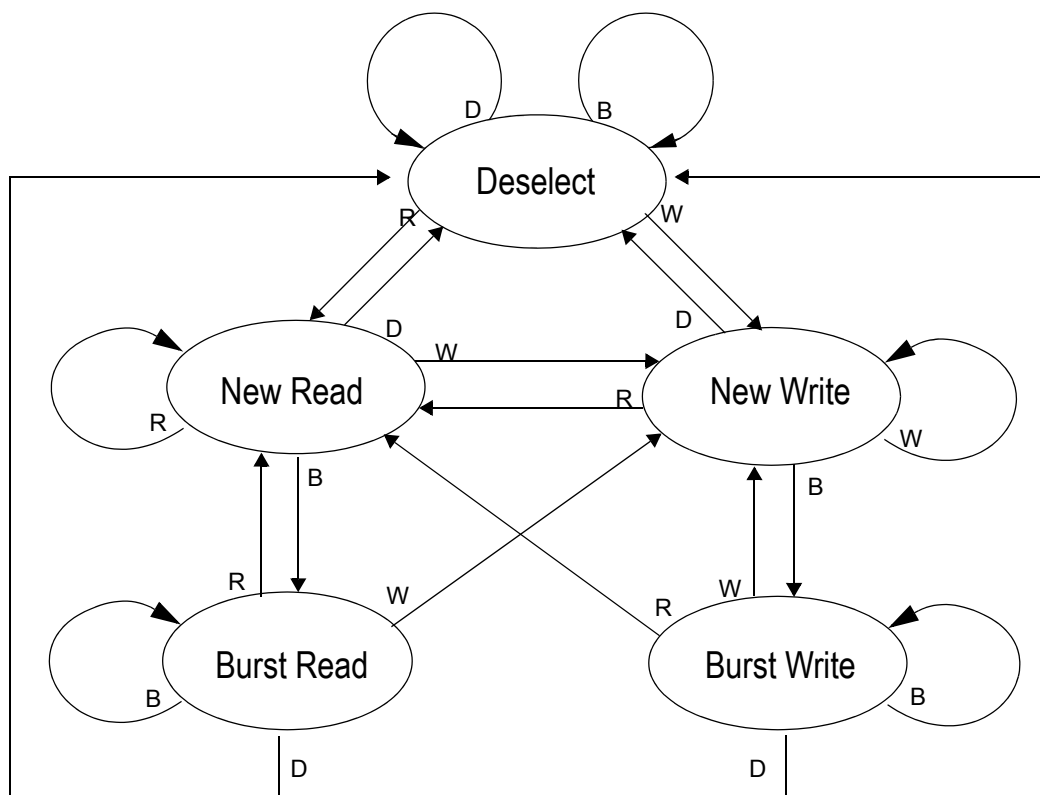
Synchronous Truth Table

Operation	Type	Address	CK	$\overline{\text{CKE}}$	ADV	$\overline{\text{W}}$	$\overline{\text{Bx}}$	$\overline{\text{E1}}$	E2	$\overline{\text{E3}}$	$\overline{\text{G}}$	ZZ	DQ	Notes
Read Cycle, Begin Burst	R	External	L-H	L	L	H	X	L	H	L	L	L	Q	
Read Cycle, Continue Burst	B	Next	L-H	L	H	X	X	X	X	X	L	L	Q	1,10
NOP/Read, Begin Burst	R	External	L-H	L	L	H	X	L	H	L	H	L	High-Z	2
Dummy Read, Continue Burst	B	Next	L-H	L	H	X	X	X	X	X	H	L	High-Z	1,2,10
Write Cycle, Begin Burst	W	External	L-H	L	L	L	L	L	H	L	X	L	D	3
Write Cycle, Continue Burst	B	Next	L-H	L	H	X	L	X	X	X	X	L	D	1,3,10
Write Abort, Continue Burst	B	Next	L-H	L	H	X	H	X	X	X	X	L	High-Z	1,2,3,10
Deselect Cycle, Power Down	D	None	L-H	L	L	X	X	H	X	X	X	L	High-Z	
Deselect Cycle, Power Down	D	None	L-H	L	L	X	X	X	X	H	X	L	High-Z	
Deselect Cycle, Power Down	D	None	L-H	L	L	X	X	X	L	X	X	L	High-Z	
Deselect Cycle	D	None	L-H	L	L	L	H	L	H	L	X	L	High-Z	1
Deselect Cycle, Continue	D	None	L-H	L	H	X	X	X	X	X	X	L	High-Z	1
Sleep Mode		None	X	X	X	X	X	X	X	X	X	H	High-Z	
Clock Edge Ignore, Stall		Current	L-H	H	X	X	X	X	X	X	X	L	-	4

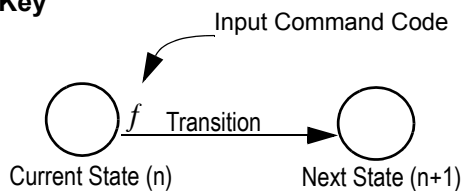
Notes:

- Continue Burst cycles, whether read or write, use the same control inputs. A Deselect continue cycle can only be entered into if a Deselect cycle is executed first.
- Dummy Read and Write abort can be considered NOPs because the SRAM performs no operation. A Write abort occurs when the $\overline{\text{W}}$ pin is sampled low but no Byte Write pins are active so no write operation is performed.
- $\overline{\text{G}}$ can be wired low to minimize the number of control signals provided to the SRAM. Output drivers will automatically turn off during write cycles.
- If $\overline{\text{CKE}}$ High occurs during a pipelined read cycle, the DQ bus will remain active (Low Z). If $\overline{\text{CKE}}$ High occurs during a write cycle, the bus will remain in High Z.
- X = Don't Care; H = Logic High; L = Logic Low; $\overline{\text{Bx}}$ = High = All Byte Write signals are high; $\overline{\text{Bx}}$ = Low = One or more Byte/Write signals are Low
- All inputs, except $\overline{\text{G}}$ and ZZ must meet setup and hold times of rising clock edge.
- Wait states can be inserted by setting $\overline{\text{CKE}}$ high.
- This device contains circuitry that ensures all outputs are in High Z during power-up.
- A 2-bit burst counter is incorporated.
- The address counter is incremented for all Burst continue cycles.

Pipelined and Flow Through Read Write Control State Diagram

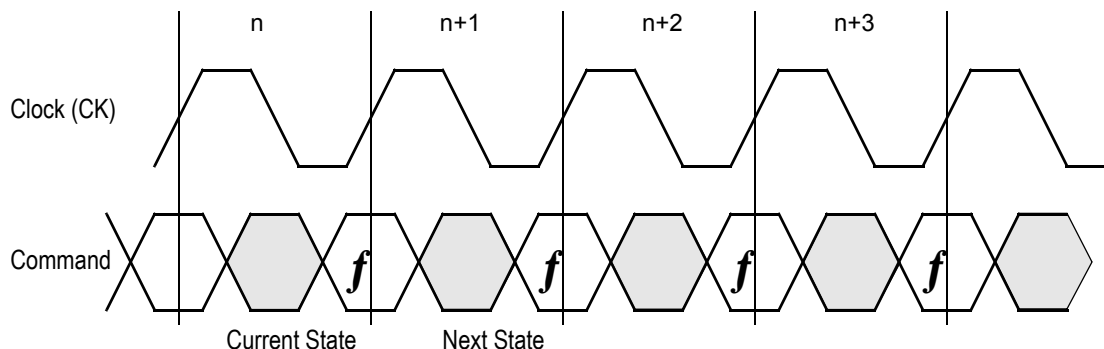


Key



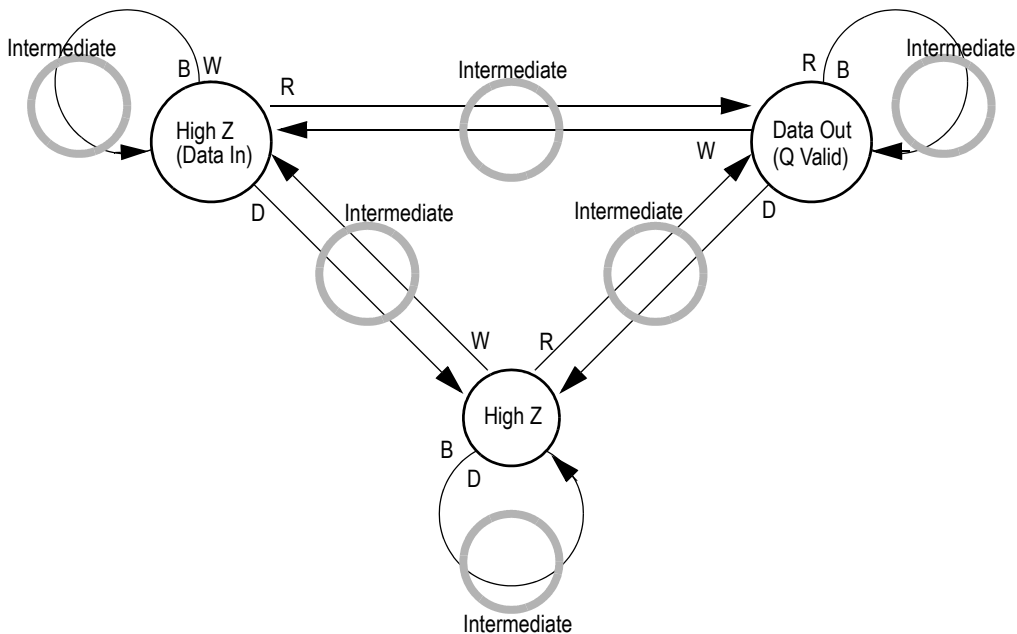
Notes:

1. The Hold command ($\overline{\text{CKE}}$ Low) is not shown because it prevents any state change.
2. W, R, B, and D represent input command codes as indicated in the Synchronous Truth Table.

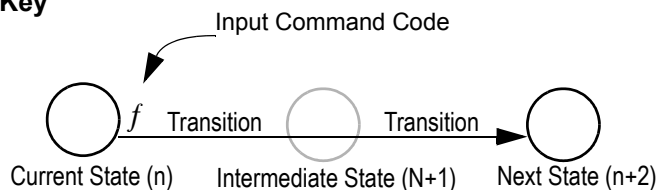


Current State and Next State Definition for Pipelined and Flow Through Read/Write Control State Diagram

Pipeline Mode Data I/O State Diagram

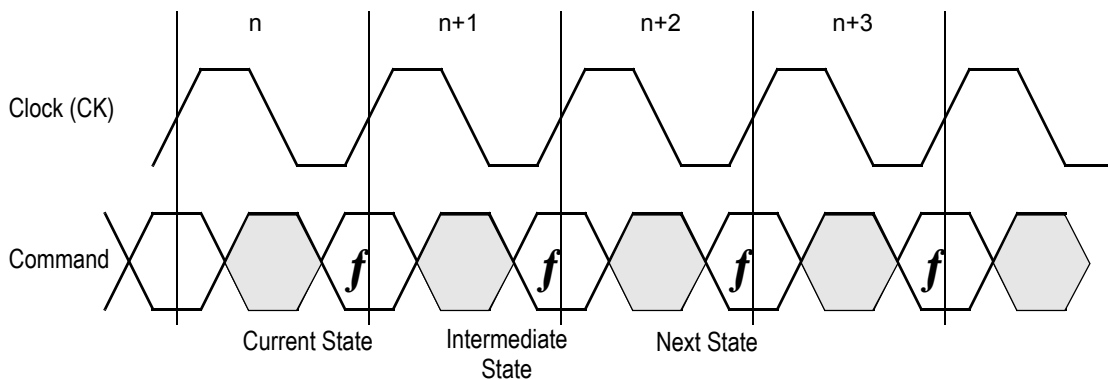


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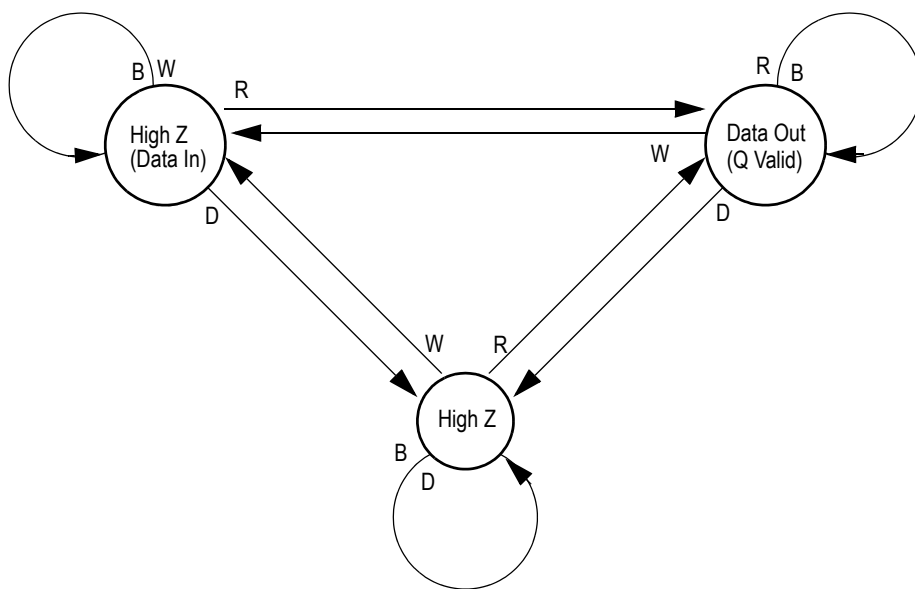
Notes:

1. The Hold command ($\overline{\text{CKE}}$ Low) is not shown because it prevents any state change.
2. W, R, B, and D represent input command codes as indicated in the Truth Tables.

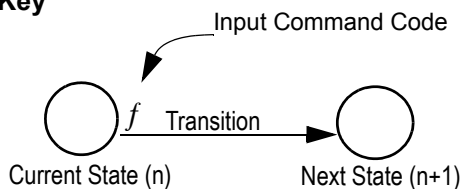


Current State and Next State Definition for Pipeline Mode Data I/O State Diagram

Flow Through Mode Data I/O State Diagram

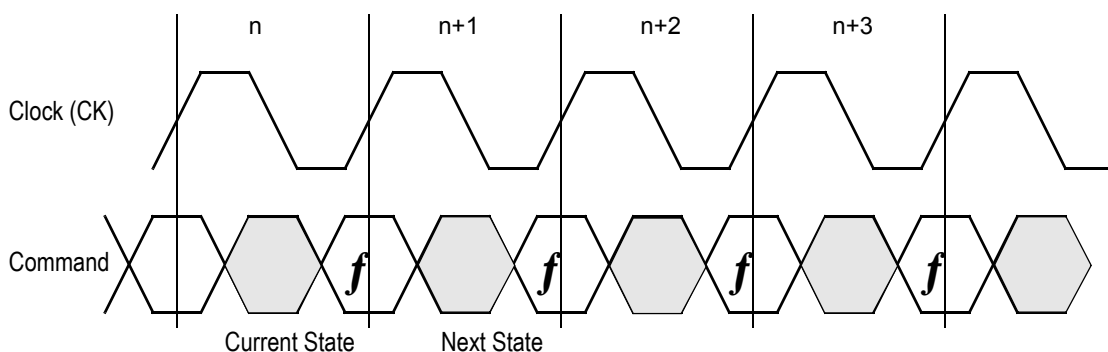


Key



Notes:

1. The Hold command ($\overline{\text{CKE}}$ Low) is not shown because it prevents any state change.
2. W, R, B, and D represent input command codes as indicated in the Truth Tables.



Current State and Next State Definition for: Pipeline and Flow through Read Write Control State Diagram

Burst Cycles

Although NBT RAMs are designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from read to write, multiple back-to-back reads or writes may also be performed. NBT SRAMs provide an on-chip burst address generator that can be utilized, if desired, to further simplify burst read or write implementations. The ADV control pin, when driven high, commands the SRAM to advance the internal address counter and use the counter generated address to read or write the SRAM. The starting address for the first cycle in a burst cycle series is loaded into the SRAM by driving the ADV pin low, into Load mode.

Burst Order

The burst address counter wraps around to its initial state after four addresses (the loaded address and three more) have been accessed. The burst sequence is determined by the state of the Linear Burst Order pin ($\overline{\text{LBO}}$). When this pin is low, a linear burst sequence is selected. When the RAM is installed with the LBO pin tied high, Interleaved burst sequence is selected. See the tables below for details.

Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{\text{LBO}}$	L	Linear Burst
		H	Interleaved Burst
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$

Note:

There are pull-up devices on the $\overline{\text{FT}}$ pin and a pull-down device on the ZZ pin, so those input pins can be unconnected and the chip will operate in the default states as specified in the above tables.

Burst Counter Sequences

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note:

The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

Note:

The burst counter wraps to initial state on the 5th clock.

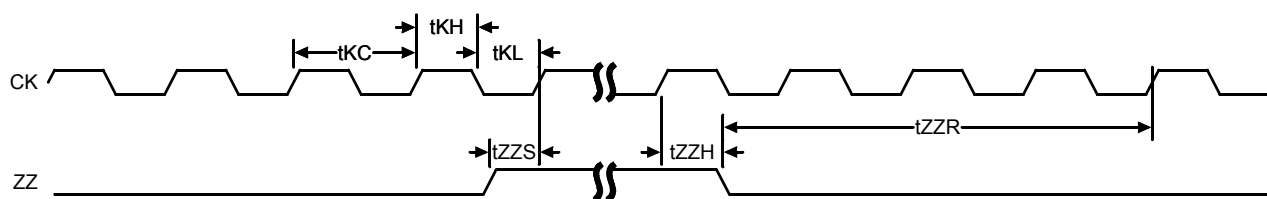
BPR 1999.05.18

Sleep Mode

During normal operation, ZZ must be pulled low, either by the user or by its internal pull down resistor. When ZZ is pulled high, the SRAM will enter a Power Sleep mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates normally after ZZ recovery time.

Sleep mode is a low current, power-down mode in which the device is deselected and current is reduced to I_{SB2} . The duration of Sleep mode is dictated by the length of time the ZZ is in a high state. After entering Sleep mode, all inputs except ZZ become disabled and all outputs go to High-Z. The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep mode. When the ZZ pin is driven high, I_{SB2} is guaranteed after the time t_{ZZI} is met. Because ZZ is an asynchronous input, pending operations or operations in progress may not be properly completed if ZZ is asserted. Therefore, Sleep mode must not be initiated until valid pending operations are completed. Similarly, when exiting Sleep mode during t_{ZZR} , only a Deselect or Read commands may be applied while the SRAM is recovering from Sleep mode.

Sleep Mode Timing Diagram



Designing for Compatibility

The GSI NBT SRAMs offer users a configurable selection between Flow Through mode and Pipelinemode via the $\overline{FT}$ signal found on Pin 14. Not all vendors offer this option, however most mark Pin 14 as V_{DD} or V_{DDQ} on pipelined parts and V_{SS} on flow through parts. GSI NBT SRAMs are fully compatible with these sockets.

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	−0.5 to 4.6	V
V_{DDQ}	Voltage in V_{DDQ} Pins	−0.5 to 4.6	V
$V_{I/O}$	Voltage on I/O Pins	−0.5 to $V_{DDQ} + 0.5$ (≤ 4.6 V max.)	V
V_{IN}	Voltage on Other Input Pins	−0.5 to $V_{DD} + 0.5$ (≤ 4.6 V max.)	V
I_{IN}	Input Current on Any Pin	+/−20	mA
I_{OUT}	Output Current on Any I/O Pin	+/−20	mA
P_D	Package Power Dissipation	1.5	W
T_{STG}	Storage Temperature	−55 to 125	°C
T_{BIAS}	Temperature Under Bias	−55 to 125	°C

Note:

Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

Power Supply Voltage Ranges

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
3.3 V Supply Voltage	V_{DD3}	3.0	3.3	3.6	V	
2.5 V Supply Voltage	V_{DD2}	2.3	2.5	2.7	V	
3.3 V V_{DDQ} I/O Supply Voltage	V_{DDQ3}	3.0	3.3	3.6	V	
2.5 V V_{DDQ} I/O Supply Voltage	V_{DDQ2}	2.3	2.5	2.7	V	

Notes:

1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be $-2\text{ V} > V_i < V_{DDn} + 2\text{ V}$ not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

V_{DDQ3} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
V _{DD} Input High Voltage	V _{IH}	2.0	—	V _{DD} + 0.3	V	1
V _{DD} Input Low Voltage	V _{IL}	−0.3	—	0.8	V	1
V _{DDQ} I/O Input High Voltage	V _{IHQ}	2.0	—	V _{DDQ} + 0.3	V	1,3
V _{DDQ} I/O Input Low Voltage	V _{ILQ}	−0.3	—	0.8	V	1,3

Notes:

1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be $-2\text{ V} > V_i < V_{DDn} + 2\text{ V}$ not to exceed 4.6 V maximum, with a pulse width not to exceed 20% t_{KC}.
3. V_{IHQ} (max) is voltage on V_{DDQ} pins plus 0.3 V.

V_{DDQ2} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
V _{DD} Input High Voltage	V _{IH}	0.6*V _{DD}	—	V _{DD} + 0.3	V	1
V _{DD} Input Low Voltage	V _{IL}	−0.3	—	0.3*V _{DD}	V	1
V _{DDQ} I/O Input High Voltage	V _{IHQ}	0.6*V _{DD}	—	V _{DDQ} + 0.3	V	1,3
V _{DDQ} I/O Input Low Voltage	V _{ILQ}	−0.3	—	0.3*V _{DD}	V	1,3

Notes:

1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be $-2\text{ V} > V_i < V_{DDn} + 2\text{ V}$ not to exceed 4.6 V maximum, with a pulse width not to exceed 20% t_{KC}.
3. V_{IHQ} (max) is voltage on V_{DDQ} pins plus 0.3 V.

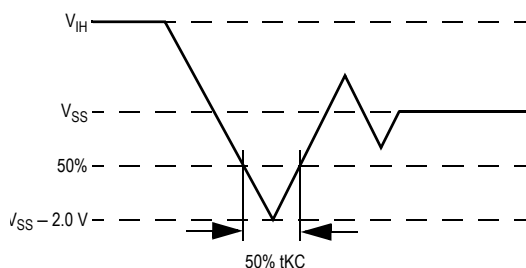
Recommended Operating Temperatures

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Ambient Temperature (Commercial Range Versions)	T _A	0	25	70	°C	2
Ambient Temperature (Industrial Range Versions)	T _A	−40	25	85	°C	2

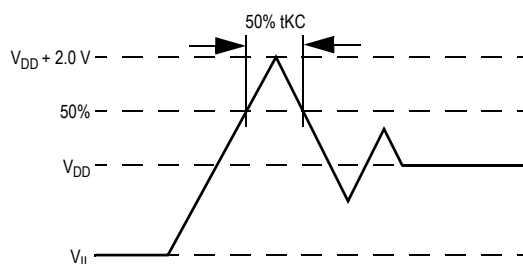
Notes:

1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be $-2\text{ V} > V_i < V_{DDn} + 2\text{ V}$ not to exceed 4.6 V maximum, with a pulse width not to exceed 20% t_{KC}.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



Capacitance

($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{DD} = 2.5\text{ V}$)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0\text{ V}$	4	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{OUT} = 0\text{ V}$	6	7	pF

Note:

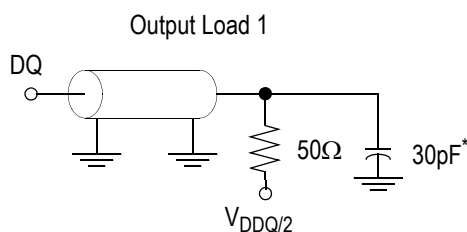
These parameters are sample tested.

AC Test Conditions

Parameter	Conditions
Input high level	$V_{DD} - 0.2\text{ V}$
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	$V_{DD}/2$
Output reference level	$V_{DDQ}/2$
Output load	Fig. 1

Notes:

1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Device is deselected as defined by the Truth Table.



* Distributed Test Jig Capacitance

DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	I_{IL}	$V_{IN} = 0 \text{ to } V_{DD}$	-1 μ A	1 μ A
ZZ Input Current	I_{IN1}	$V_{DD} \geq V_{IN} \geq V_{IH}$ $0 \text{ V} \leq V_{IN} \leq V_{IH}$	-1 μ A -1 μ A	1 μ A 100 μ A
$\overline{FT}$ Input Current	I_{IN2}	$V_{DD} \geq V_{IN} \geq V_{IL}$ $0 \text{ V} \leq V_{IN} \leq V_{IL}$	-100 μ A -1 μ A	1 μ A 1 μ A
Output Leakage Current	I_{OL}	Output Disable, $V_{OUT} = 0 \text{ to } V_{DD}$	-1 μ A	1 μ A
Output High Voltage	V_{OH2}	$I_{OH} = -8 \text{ mA}$, $V_{DDQ} = 2.375 \text{ V}$	1.7 V	—
Output High Voltage	V_{OH3}	$I_{OH} = -8 \text{ mA}$, $V_{DDQ} = 3.135 \text{ V}$	2.4 V	—
Output Low Voltage	V_{OL}	$I_{OL} = 8 \text{ mA}$	—	0.4 V

Operating Currents

Parameter	Test Conditions	Mode	Symbol	-250		-225		-200		-166		-150		-133		Unit
				0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	
Operating Current 3.3 V	Device Selected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Output open	(x36)	Pipeline	290	300	265	275	240	250	205	215	190	200	170	180	mA
			I_{DDQ}	40	40	35	35	30	30	25	25	25	25	20	20	
		(x18)	Pipeline	180	190	170	180	165	175	155	165	150	160	140	150	mA
			I_{DDQ}	20	20	20	20	15	15	15	15	15	15	10	10	
Operating Current 2.5 V	Device Selected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Output open	(x36)	Pipeline	260	270	235	245	215	225	185	195	170	180	155	165	mA
			I_{DDQ}	20	20	20	20	15	15	15	15	15	15	10	10	
		(x18)	Pipeline	165	175	155	165	150	160	140	150	135	145	125	135	mA
			I_{DDQ}	10	10	10	10	10	10	10	10	10	10	10	10	
Standby Current	$ZZ \geq V_{DD} - 0.2 V$	(x36)	Pipeline	290	300	265	275	240	250	205	215	190	200	170	180	mA
			I_{DDQ}	30	30	30	30	25	25	20	20	20	20	15	15	
		(x18)	Pipeline	180	190	170	180	165	175	155	165	150	160	140	150	mA
			I_{DDQ}	20	20	20	20	15	15	15	15	15	15	10	10	
Deselect Current	Device Deselected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$	(x36)	Pipeline	260	270	235	245	215	225	185	195	170	180	155	165	mA
			I_{DDQ}	15	15	15	15	10	10	10	10	10	10	10	10	
		(x18)	Pipeline	165	175	155	165	150	160	140	150	135	145	125	135	mA
			I_{DDQ}	10	10	10	10	10	10	10	10	10	10	10	10	
Standby Current	$ZZ \geq V_{DD} - 0.2 V$	(x36)	Pipeline	20	30	20	30	20	30	20	30	20	30	20	30	mA
			I_{SB}	20	30	20	30	20	30	20	30	20	30	20	30	
		(x18)	Pipeline	85	90	80	85	75	80	64	70	60	65	50	55	mA
			I_{SB}	60	65	60	65	50	55	50	55	50	55	45	50	

Notes:

- I_{DD} and I_{DDQ} apply to any combination of V_{DD3} , V_{DD2} , V_{DDQ3} , and V_{DDQ2} operation.
- All parameters listed are worst case scenario.

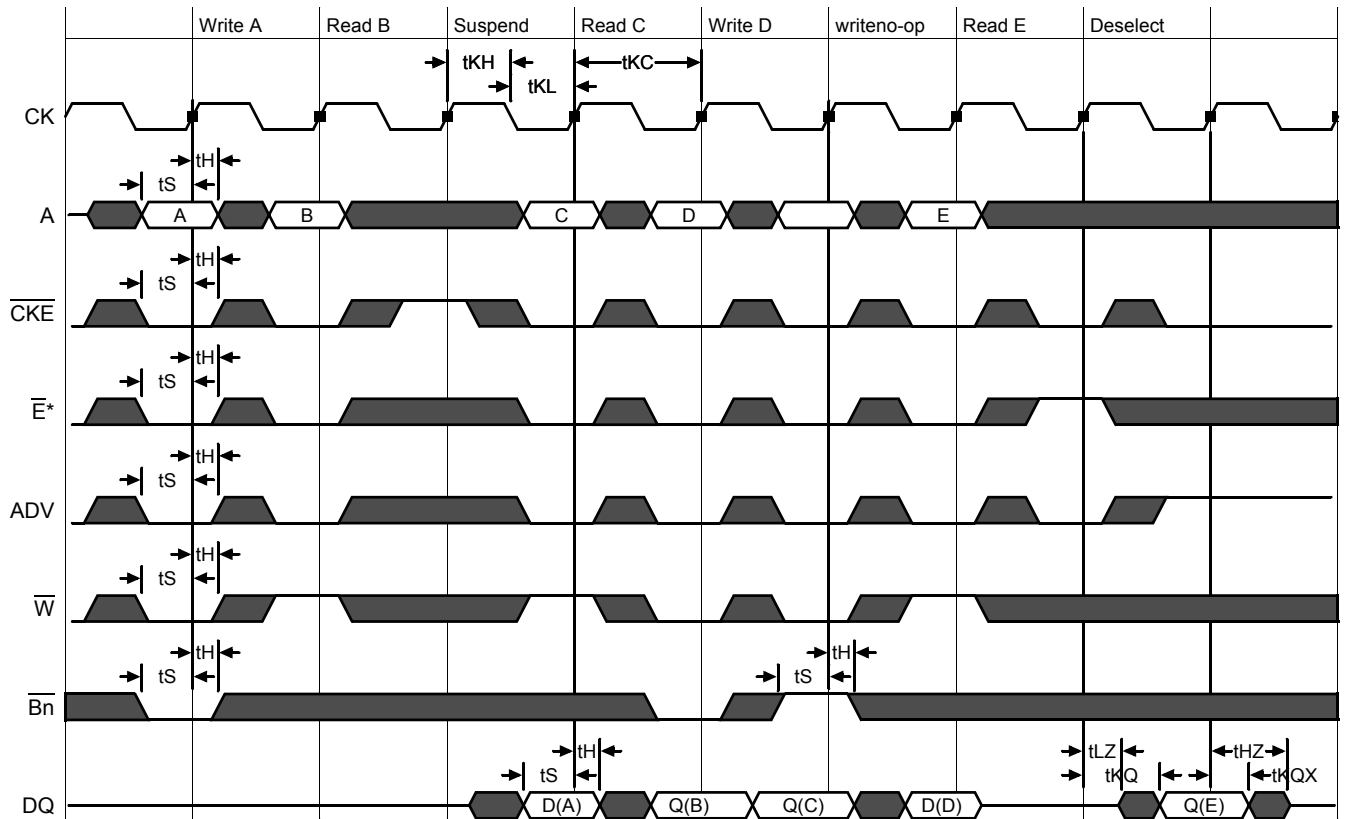
AC Electrical Characteristics

	Parameter	Symbol	-250		-225		-200		-166		-150		-133		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Pipeline	Clock Cycle Time	t _{KC}	4.0	—	4.4	—	5.0	—	6.0	—	6.7	—	7.5	—	ns
	Clock to Output Valid	t _{KQ}	—	2.5	—	2.7	—	3.0	—	3.4	—	3.8	—	4.0	ns
	Clock to Output Invalid	t _{KQX}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Clock to Output in Low-Z	t _{LZ} ¹	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Setup time	t _S	1.2	—	1.3	—	1.4	—	1.5	—	1.5	—	1.5	—	ns
	Hold time	t _H	0.2	—	0.3	—	0.4	—	0.5	—	0.5	—	0.5	—	ns
Flow Through	Clock Cycle Time	t _{KC}	5.5	—	6.0	—	6.5	—	7.0	—	7.5	—	8.5	—	ns
	Clock to Output Valid	t _{KQ}	—	5.5	—	6.0	—	6.5	—	7.0	—	7.5	—	8.5	ns
	Clock to Output Invalid	t _{KQX}	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock to Output in Low-Z	t _{LZ} ¹	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Setup time	t _S	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Hold time	t _H	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
	Clock HIGH Time	t _{KH}	1.3	—	1.3	—	1.3	—	1.3	—	1.5	—	1.7	—	ns
	Clock LOW Time	t _{KL}	1.5	—	1.5	—	1.5	—	1.5	—	1.7	—	2	—	ns
	Clock to Output in High-Z	t _{HZ} ¹	1.5	2.3	1.5	2.5	1.5	3.0	1.5	3.0	1.5	3.0	1.5	3.0	ns
	$\overline{G}$ to Output Valid	t _{OE}	—	2.3	—	2.5	—	3.2	—	3.5	—	3.8	—	4.0	ns
	$\overline{G}$ to output in Low-Z	t _{OLZ} ¹	0	—	0	—	0	—	0	—	0	—	0	—	ns
	$\overline{G}$ to output in High-Z	t _{OHZ} ¹	—	2.3	—	2.5	—	3.0	—	3.0	—	3.0	—	3.0	ns
	ZZ setup time	t _{ZZS} ²	5	—	5	—	5	—	5	—	5	—	5	—	ns
	ZZ hold time	t _{ZZH} ²	1	—	1	—	1	—	1	—	1	—	1	—	ns
	ZZ recovery	t _{ZZR}	20	—	20	—	20	—	20	—	20	—	20	—	ns

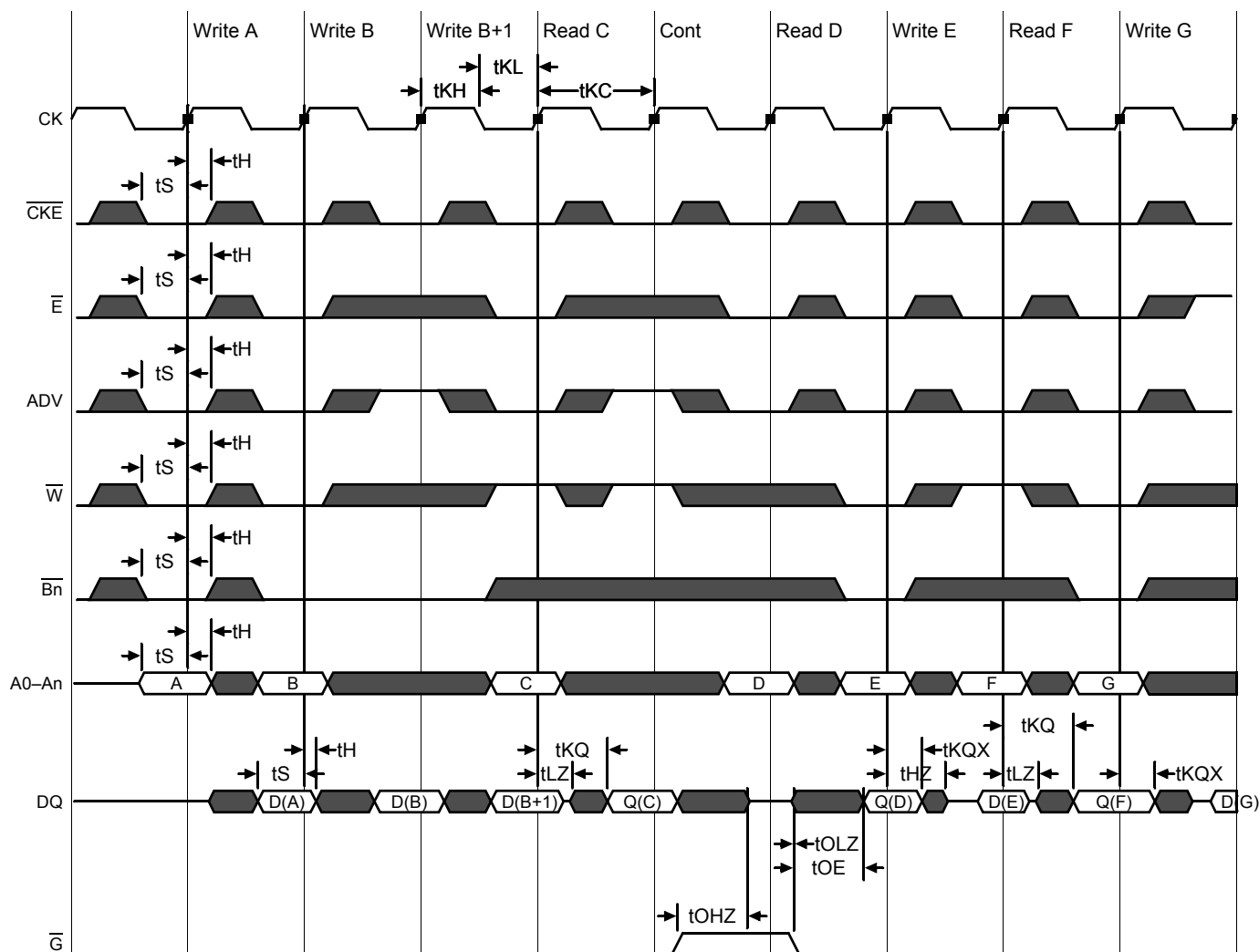
Notes:

- These parameters are sampled and are not 100% tested.
- ZZ is an asynchronous signal. However, in order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

Pipeline Mode Timing



Flow Through Mode Timing



*Note: $\overline{E}$ = High(False) if $\overline{E1} = 1$ or $E2 = 0$ or $\overline{E3} = 1$

JTAG Port Operation

Overview

The JTAG Port on this RAM operates in a manner that is compliant with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG). The JTAG Port input interface levels scale with V_{DD} . The JTAG output drivers are powered by V_{DDO} .

Disabling the JTAG Port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. TCK, TDI, and TMS are designed with internal pull-up circuits. To assure normal operation of the RAM with the JTAG Port unused, TCK, TDI, and TMS may be left floating or tied to either V_{DD} or V_{SS} . TDO should be left unconnected.

JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	Test Mode Select	In	The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.
TDI	Test Data In	In	The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP Controller state machine and the instruction that is currently loaded in the TAP Instruction Register (refer to the TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.
TDO	Test Data Out	Out	Output that is active depending on the state of the TAP state machine. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

Note:

This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automatically at power-up.

JTAG Port Registers

Overview

The various JTAG registers, referred to as Test Access Port or TAP Registers, are selected (one at a time) via the sequences of 1s and 0s applied to TMS as TCK is strobed. Each of the TAP Registers is a serial shift register that captures serial input data on the rising edge of TCK and pushes serial data out on the next falling edge of TCK. When a register is selected, it is placed between the TDI and TDO pins.

Instruction Register

The Instruction Register holds the instructions that are executed by the TAP controller when it is moved into the Run, Test/Idle, or the various data register states. Instructions are 3 bits long. The Instruction Register can be loaded when it is placed between the TDI and TDO pins. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in Test-Logic-Reset state.

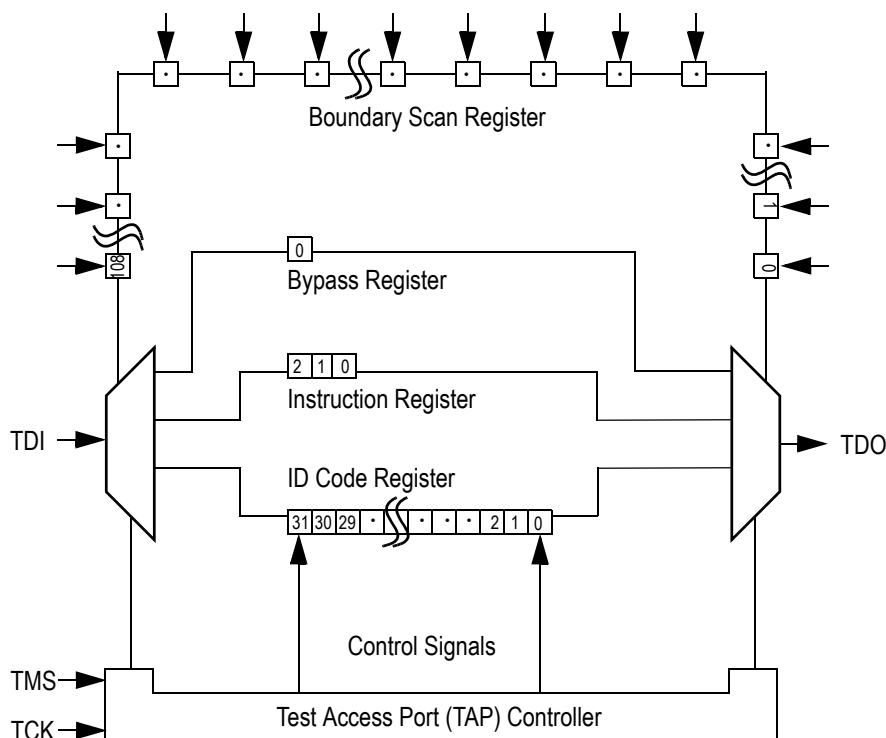
Bypass Register

The Bypass Register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAM's JTAG Port to another device in the scan chain with as little delay as possible.

Boundary Scan Register

The Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the RAM's input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port's TDO pin. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the Scan Order Table following. The Boundary Scan Register, under the control of the TAP Controller, is loaded with the contents of the RAMs I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. SAMPLE-Z, SAMPLE/PRELOAD and EXTEST instructions can be used to activate the Boundary Scan Register.

JTAG TAP Block Diagram



Identification (ID) Register

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Contents

	Die Revision Code				Not Used												I/O Configuration				GSI Technology JEDEC Vendor ID Code												Presence Register
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
x36	X	X	X	X	0	0	0	X	1	0	0	1	0	0	0	0	1	0	0	0	0	0	0	1	1	0	1	1	0	0	1	1	
x18	X	X	X	X	0	0	0	X	1	0	0	1	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1	1	0	0	1	1	

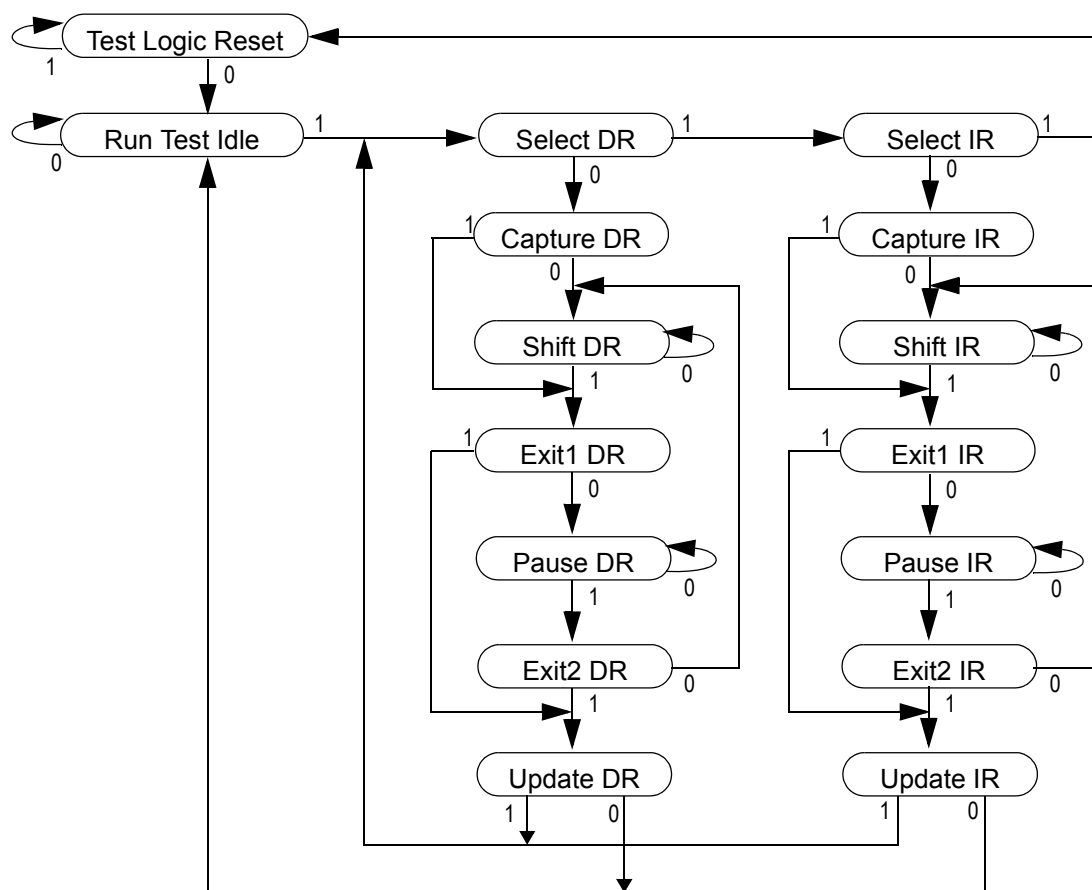
Tap Controller Instruction Set

Overview

There are two classes of instructions defined in the Standard 1149.1-1990; the standard (Public) instructions, and device specific (Private) instructions. Some Public instructions are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. The TAP on this device may be used to monitor all input and I/O pads, and can be used to load address, data or control signals into the RAM or to preload the I/O buffers.

When the TAP controller is placed in Capture-IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state the Instruction Register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction set for this device is listed in the following table.

JTAG Tap Controller State Diagram



Instruction Descriptions

BYPASS

When the BYPASS instruction is loaded in the Instruction Register the Bypass Register is placed between TDI and TDO. This occurs when the TAP controller is moved to the Shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the Instruction Register, moving the TAP controller into the Capture-DR state loads the data in the RAMs input and I/O buffers into the Boundary Scan Register. Boundary Scan Register locations are not associated with an input or I/O pin, and are loaded with the default state identified in the Boundary Scan Chain table at the end of this section of the datasheet. Because the RAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set-up plus hold time (tTS plus tTH). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to Shift-DR state then places the boundary scan register between the TDI and TDO pins.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register is loaded with all logic 0s. The EXTEST command does not block or override the RAM's input pins; therefore, the RAM's internal state is still determined by its input pins.

Typically, the Boundary Scan Register is loaded with the desired pattern of data with the SAMPLE/PRELOAD command. Then the EXTEST command is used to output the Boundary Scan Register's contents, in parallel, on the RAM's data output drivers on the falling edge of TCK when the controller is in the Update-IR state.

Alternately, the Boundary Scan Register may be loaded in parallel using the EXTEST command. When the EXTEST instruction is selected, the state of all the RAM's input and I/O pins, as well as the default values at Scan Register locations not associated with a pin, are transferred in parallel into the Boundary Scan Register on the rising edge of TCK in the Capture-DR state, the RAM's output pins drive out the value of the Boundary Scan Register location with which each output pin is associated.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.

SAMPLE-Z

If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z) and the Boundary Scan Register is connected between TDI and TDO when the TAP controller is moved to the Shift-DR state.

RFU

These instructions are Reserved for Future Use. In this device they replicate the BYPASS instruction.

JTAG TAP Instruction Set Summary

Instruction	Code	Description	Notes
EXTEST	000	Places the Boundary Scan Register between TDI and TDO.	1
IDCODE	001	Preloads ID Register and places it between TDI and TDO.	1, 2
SAMPLE-Z	010	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all RAM output drivers to High-Z.	1
RFU	011	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
SAMPLE/ PRELOAD	100	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO.	1
GSI	101	GSI private instruction.	1
RFU	110	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
BYPASS	111	Places Bypass Register between TDI and TDO.	1

Notes:

1. Instruction codes expressed in binary, MSB on left, LSB on right.
2. Default instruction automatically loaded at power-up and in test-logic-reset state.

JTAG Port Recommended Operating Conditions and DC Characteristics

Parameter	Symbol	Min.	Max.	Unit	Notes
3.3 V Test Port Input High Voltage	V_{IHJ3}	2.0	$V_{DD3} + 0.3$	V	1
3.3 V Test Port Input Low Voltage	V_{ILJ3}	-0.3	0.8	V	1
2.5 V Test Port Input High Voltage	V_{IHJ2}	$0.6 * V_{DD2}$	$V_{DD2} + 0.3$	V	1
2.5 V Test Port Input Low Voltage	V_{ILJ2}	-0.3	$0.3 * V_{DD2}$	V	1
TMS, TCK and TDI Input Leakage Current	I_{INHJ}	-300	1	uA	2
TMS, TCK and TDI Input Leakage Current	I_{INLJ}	-1	100	uA	3
TDO Output Leakage Current	I_{OLJ}	-1	1	uA	4
Test Port Output High Voltage	V_{OHJ}	1.7	—	V	5, 6
Test Port Output Low Voltage	V_{OLJ}	—	0.4	V	5, 7
Test Port Output CMOS High	V_{OHJC}	$V_{DDQ} - 100 \text{ mV}$	—	V	5, 8
Test Port Output CMOS Low	V_{OLJC}	—	100 mV	V	5, 9

Notes:

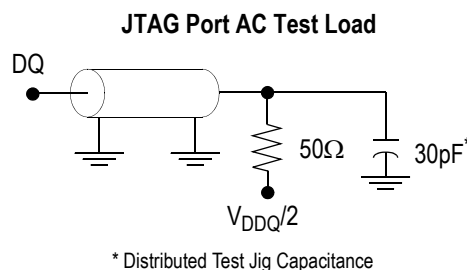
- Input Under/overshoot voltage must be $-2 \text{ V} > V_i < V_{DDn} + 2 \text{ V}$ not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tTKC.
- $V_{ILJ} \leq V_{IN} \leq V_{DDn}$
- $0 \text{ V} \leq V_{IN} \leq V_{ILJn}$
- Output Disable, $V_{OUT} = 0$ to V_{DDn}
- The TDO output driver is served by the V_{DDQ} supply.
- $I_{OHJ} = -4 \text{ mA}$
- $I_{OLJ} = +4 \text{ mA}$
- $I_{OHJC} = -100 \text{ uA}$
- $I_{OHJC} = +100 \text{ uA}$

JTAG Port AC Test Conditions

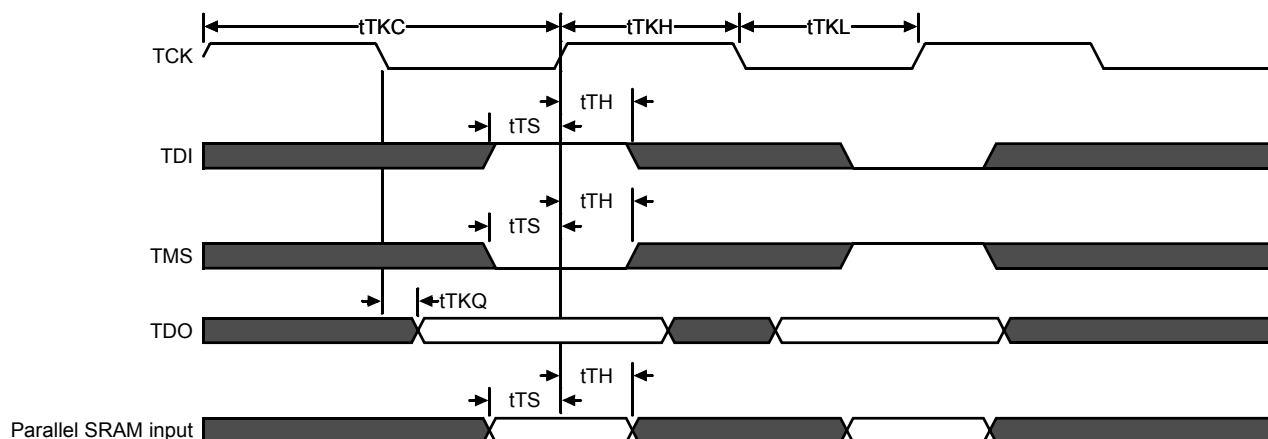
Parameter	Conditions
Input high level	$V_{DD} - 0.2 \text{ V}$
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	$V_{DDQ}/2$
Output reference level	$V_{DDQ}/2$

Notes:

- Include scope and jig capacitance.
- Test conditions as shown unless otherwise noted.



JTAG Port Timing Diagram



JTAG Port AC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
TCK Cycle Time	t_{TKC}	50	—	ns
TCK Low to TDO Valid	t_{TKQ}	—	20	ns
TCK High Pulse Width	t_{TKH}	20	—	ns
TCK Low Pulse Width	t_{TKL}	20	—	ns
TDI & TMS Set Up Time	t_{TS}	10	—	ns
TDI & TMS Hold Time	t_{TH}	10	—	ns

Boundary Scan (BSDL Files)

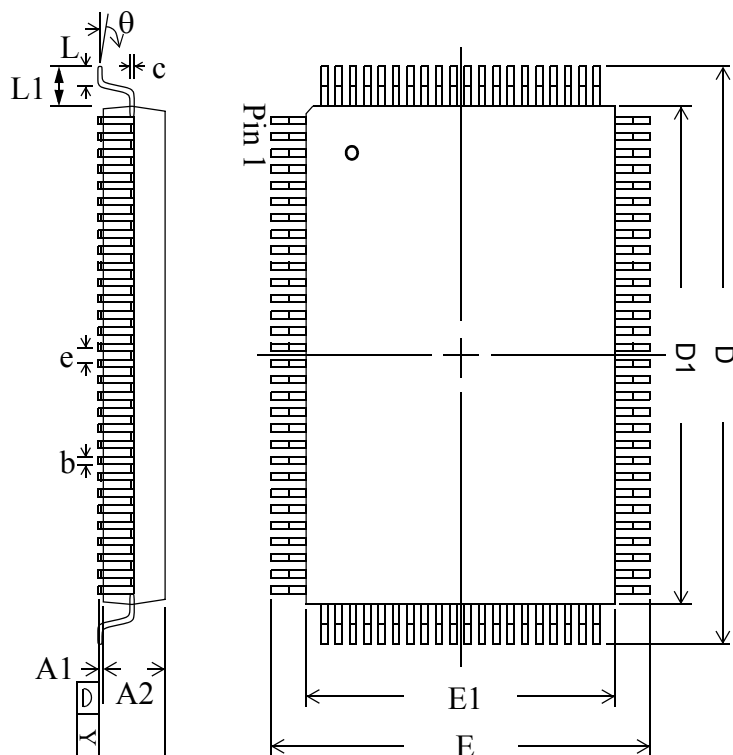
For information regarding the Boundary Scan Chain, or to obtain BSDL files for this part, please contact our Applications Engineering Department at: apps@gsitechnology.com.

TQFP Package Drawing (Package T)

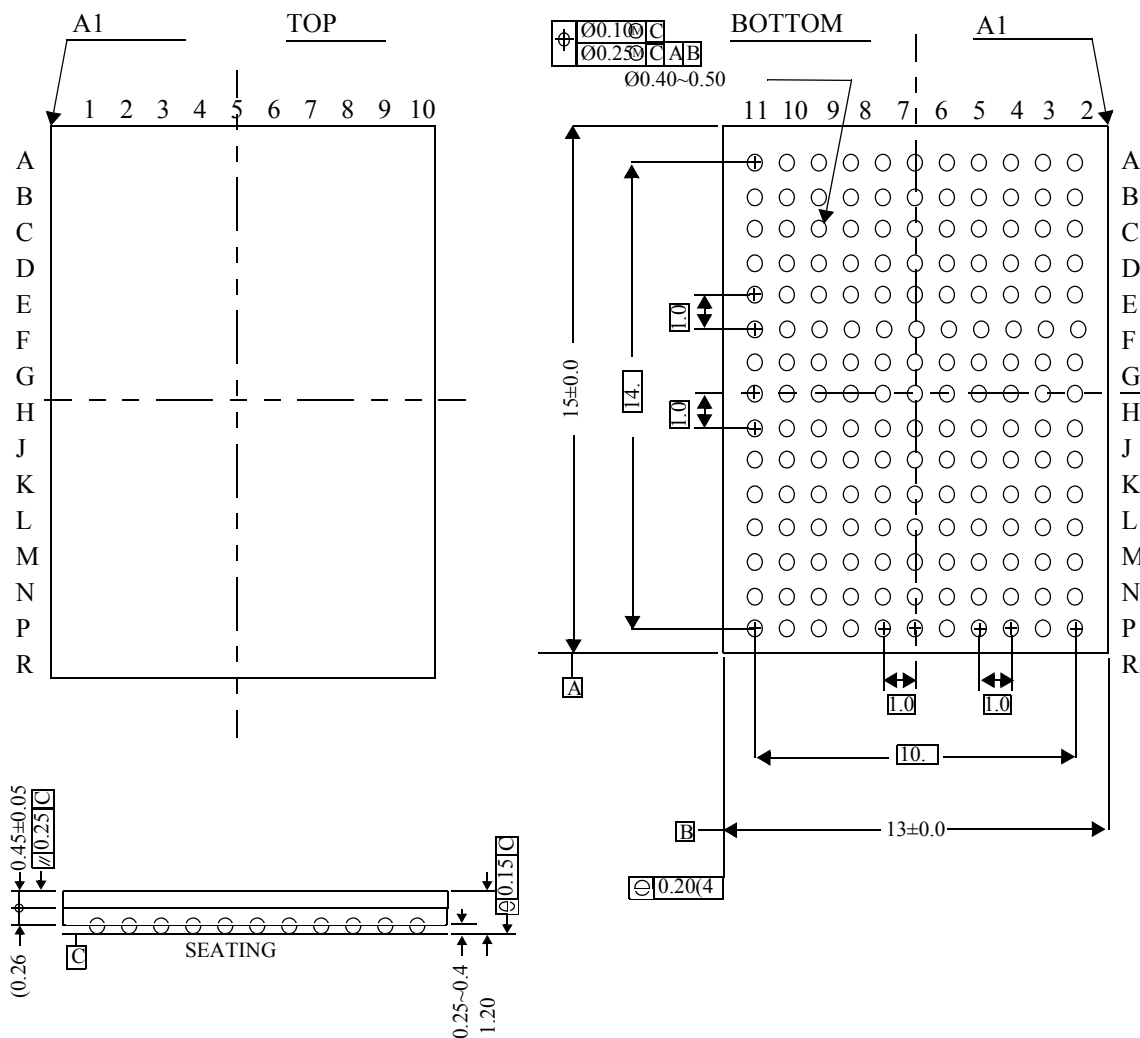
Symbol	Description	Min.	Nom.	Max
A1	Standoff	0.05	0.10	0.15
A2	Body Thickness	1.35	1.40	1.45
b	Lead Width	0.20	0.30	0.40
c	Lead Thickness	0.09	—	0.20
D	Terminal Dimension	21.9	22.0	22.1
D1	Package Body	19.9	20.0	20.1
E	Terminal Dimension	15.9	16.0	16.1
E1	Package Body	13.9	14.0	14.1
e	Lead Pitch	—	0.65	—
L	Foot Length	0.45	0.60	0.75
L1	Lead Length	—	1.00	—
Y	Coplanarity			0.10
θ	Lead Angle	0°	—	7°

Notes:

1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion.



Package Dimensions—165-Bump FPBGA (Package D; Variation 1)



Ordering Information—GSI NBT Synchronous SRAM

Org	Part Number ¹	Type	Package	Speed ² (MHz/ns)	T _A ³	Status
1M x 18	GS8161Z18T-250	NBT Pipeline/Flow Through	TQFP	250/5.5	C	
1M x 18	GS8161Z18T-225	NBT Pipeline/Flow Through	TQFP	225/6	C	
1M x 18	GS8161Z18T-200	NBT Pipeline/Flow Through	TQFP	200/6.5	C	
1M x 18	GS8161Z18T-166	NBT Pipeline/Flow Through	TQFP	166/7	C	
1M x 18	GS8161Z18T-150	NBT Pipeline/Flow Through	TQFP	150/7.5	C	
1M x 18	GS8161Z18T-133	NBT Pipeline/Flow Through	TQFP	133/8.5	C	
512K x 36	GS8161Z36T-250	NBT Pipeline/Flow Through	TQFP	250/5.5	C	
512K x 36	GS8161Z36T-225	NBT Pipeline/Flow Through	TQFP	225/6	C	
512K x 36	GS8161Z36T-200	NBT Pipeline/Flow Through	TQFP	200/6.5	C	
512K x 36	GS8161Z36T-166	NBT Pipeline/Flow Through	TQFP	166/7	C	
512K x 36	GS8161Z36T-150	NBT Pipeline/Flow Through	TQFP	150/7.5	C	
512K x 36	GS8161Z36T-133	NBT Pipeline/Flow Through	TQFP	133/8.5	C	
1M x 18	GS8161Z18T-250I	NBT Pipeline/Flow Through	TQFP	250/5.5	I	
1M x 18	GS8161Z18T-225I	NBT Pipeline/Flow Through	TQFP	225/6	I	
1M x 18	GS8161Z18T-200I	NBT Pipeline/Flow Through	TQFP	200/6.5	I	
1M x 18	GS8161Z18T-166I	NBT Pipeline/Flow Through	TQFP	166/7	I	
1M x 18	GS8161Z18T-150I	NBT Pipeline/Flow Through	TQFP	150/7.5	I	
1M x 18	GS8161Z18T-133I	NBT Pipeline/Flow Through	TQFP	133/8.5	I	
512K x 36	GS8161Z36T-250I	NBT Pipeline/Flow Through	TQFP	250/5.5	I	
512K x 36	GS8161Z36T-225I	NBT Pipeline/Flow Through	TQFP	225/6	I	
512K x 36	GS8161Z36T-200I	NBT Pipeline/Flow Through	TQFP	200/6.5	I	
512K x 36	GS8161Z36T-166I	NBT Pipeline/Flow Through	TQFP	166/7	I	
512K x 36	GS8161Z36T-150I	NBT Pipeline/Flow Through	TQFP	150/7.5	I	
512K x 36	GS8161Z36T-133I	NBT Pipeline/Flow Through	TQFP	133/8.5	I	
1M x 18	GS8161Z18D-250	NBT Pipeline/Flow Through	165 BGA (var. 1)	250/5.5	C	
1M x 18	GS8161Z18D-225	NBT Pipeline/Flow Through	165 BGA (var. 1)	225/6	C	
1M x 18	GS8161Z18D-200	NBT Pipeline/Flow Through	165 BGA (var. 1)	200/6.5	C	
1M x 18	GS8161Z18D-166	NBT Pipeline/Flow Through	165 BGA (var. 1)	166/7	C	
1M x 18	GS8161Z18D-150	NBT Pipeline/Flow Through	165 BGA (var. 1)	150/7.5	C	
1M x 18	GS8161Z18D-133	NBT Pipeline/Flow Through	165 BGA (var. 1)	133/8.5	C	

Notes:

- Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS816Z36-166IT.
- The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow through mode-selectable by the user.
- T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.
- GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsistechnology.com) for a complete listing of current offerings

Ordering Information—GSI NBT Synchronous SRAM (Continued)

Org	Part Number ¹	Type	Package	Speed ² (MHz/ns)	T _A ³	Status
512K x 32	GS8161Z32D-250	NBT Pipeline/Flow Through	165 BGA (var. 1)	250/5.5	C	
512K x 32	GS8161Z32D-225	NBT Pipeline/Flow Through	165 BGA (var. 1)	225/6	C	
512K x 32	GS8161Z32D-200	NBT Pipeline/Flow Through	165 BGA (var. 1)	200/6.5	C	
512K x 32	GS8161Z32D-166	NBT Pipeline/Flow Through	165 BGA (var. 1)	166/7	C	
512K x 32	GS8161Z32D-150	NBT Pipeline/Flow Through	165 BGA (var. 1)	150/7.5	C	
512K x 32	GS8161Z32D-133	NBT Pipeline/Flow Through	165 BGA (var. 1)	133/8.5	C	
512K x 36	GS8161Z36D-250	NBT Pipeline/Flow Through	165 BGA (var. 1)	250/5.5	C	
512K x 36	GS8161Z36D-225	NBT Pipeline/Flow Through	165 BGA (var. 1)	225/6	C	
512K x 36	GS8161Z36D-200	NBT Pipeline/Flow Through	165 BGA (var. 1)	200/6.5	C	
512K x 36	GS8161Z36D-166	NBT Pipeline/Flow Through	165 BGA (var. 1)	166/7	C	
512K x 36	GS8161Z36D-150	NBT Pipeline/Flow Through	165 BGA (var. 1)	150/7.5	C	
512K x 36	GS8161Z36D-133	NBT Pipeline/Flow Through	165 BGA (var. 1)	133/8.5	C	
1M x 18	GS8161Z18D-250I	NBT Pipeline/Flow Through	165 BGA (var. 1)	250/5.5	I	
1M x 18	GS8161Z18D-225I	NBT Pipeline/Flow Through	165 BGA (var. 1)	225/6	I	
1M x 18	GS8161Z18D-200I	NBT Pipeline/Flow Through	165 BGA (var. 1)	200/6.5	I	
1M x 18	GS8161Z18D-166I	NBT Pipeline/Flow Through	165 BGA (var. 1)	166/7	I	
1M x 18	GS8161Z18D-150I	NBT Pipeline/Flow Through	165 BGA (var. 1)	150/7.5	I	
1M x 18	GS8161Z18D-133I	NBT Pipeline/Flow Through	165 BGA (var. 1)	133/8.5	I	
512K x 32	GS8161Z32D-250I	NBT Pipeline/Flow Through	165 BGA (var. 1)	250/5.5	I	
512K x 32	GS8161Z32D-225I	NBT Pipeline/Flow Through	165 BGA (var. 1)	225/6	I	
512K x 32	GS8161Z32D-200I	NBT Pipeline/Flow Through	165 BGA (var. 1)	200/6.5	I	
512K x 32	GS8161Z32D-166I	NBT Pipeline/Flow Through	165 BGA (var. 1)	166/7	I	
512K x 32	GS8161Z32D-150I	NBT Pipeline/Flow Through	165 BGA (var. 1)	150/7.5	I	
512K x 32	GS8161Z32D-133I	NBT Pipeline/Flow Through	165 BGA (var. 1)	133/8.5	I	
512K x 36	GS8161Z36D-250I	NBT Pipeline/Flow Through	165 BGA (var. 1)	250/5.5	I	
512K x 36	GS8161Z36D-225I	NBT Pipeline/Flow Through	165 BGA (var. 1)	225/6	I	
512K x 36	GS8161Z36D-200I	NBT Pipeline/Flow Through	165 BGA (var. 1)	200/6.5	I	
512K x 36	GS8161Z36D-166I	NBT Pipeline/Flow Through	165 BGA (var. 1)	166/7	I	
512K x 36	GS8161Z36D-150I	NBT Pipeline/Flow Through	165 BGA (var. 1)	150/7.5	I	
512K x 36	GS8161Z36D-133I	NBT Pipeline/Flow Through	165 BGA (var. 1)	133/8.5	I	

Notes:

- Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS816Z36-166IT.
- The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow through mode-selectable by the user.
- T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.
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18Mb Sync SRAM Data Sheet Revision History

DS/DateRev. Code: Old; New	Types of Changes Format or Content	Page;Revisions;Reason
GS18/36 1.00 9/ 1999A;GS18/362.0012/ 1999B	Content	• Converted from 0.25u 3.3V process to 0.18u 2.5V process. • Master File Rev B • Added x72 Pinout.
GS18/362.00 12/ 1999BGS18/362.01 1/2000C	Format	• Added new GSI Logo
GS18/362.0 1/2000DGS18/ 362.03 2/2000E		• Front page; Features - changed 2.5V I/O supply to 2.5V or 3.3V I/O supply; Completeness • Absolute Maximum Ratings; Changed VDDQ - Value: From: -.05 to VDD : to : -.05 to 3.6; Completeness. • Recommended Operating Conditions; Changed: I/O Supply Voltage- Max. from VDD to 3.6; Input High Voltage- Max. from VDD +0.3 to 3.6; Same page - took out Note 1; Completeness • Electrical Characteristics - Added second Output High Voltage line to table; completeness. • Note: There was not a Rev 2.02 for the 8160Z or the 8161Z.
GS18/362.03 2/2000E; 8161Z18_r2_04	Content	• Pin 14 removed from V_{SS} in pin description table. • ADV changed to pin 85 in pin description table.
8161Z18_r2_04; 8161Z18_r2_05	Content	• Changed the value of ZZ recovery in the AC Electrical Characteristics table on page 18 from 20 ns to 100 ns
8161Z18_r2_05; 8161Z18_r2_06	Content/Format	• Added 225 MHz speed bin • Updated page 1 table, AC Characteristics table, and Operating Currents table • Updated format to comply with Technical Publications standards • Updated Capacitance table—removed Input row and updated Output row to I/O
8161Z18_r2_06; 8161Z18_r2_07	Content	• Updated Features list on page 1 • Completely reworked table on page 1 • Updated Mode Pin Functions on page 12
8161Z18_r2_07; 8161Z18_r2_08	Content	• Added 3.3 V references to entire document • Updated Operating Conditions table • Updated JTAG Operating Conditions table • Updated Boundary Scan Chain table • Updated Operating Currents table and added note • Updated table on page 1; added power numbers
8161Z18_r2_08; 8161Z18_r2_09	Content	• Updated Pin Description table • Updated DQ on page 21 • Updated DQ on page 23 • Updated Operating Currents table • Updated table on page 1; updated power numbers • Updated Recommended Operating Conditions table (added V_{DDQ} references)

18Mb Sync SRAM Data Sheet Revision History

DS/DateRev. Code: Old; New	Types of Changes Format or Content	Page;Revisions;Reason
8161Z18_r2_09; 8161Z18_r2_10	Content	• Updated table on page 1 • Created recommended operating conditions tables on pages 15 and 16 • Updated AC Electrical Characteristics table • Updated Ordering Information for 225 MHz part (changed from 7ns to 6.5 ns) • Updated BSR table (2 and 3 changed to X (value undefined)) • Added 250 MHz speed bin • Deleted 180 MHz speed bin
8161Z18_r2_10; 8161Z18_r2_11	Content	• Updated AC Characteristics table • Updated FT power numbers • Updated Mb references from 16Mb to 18Mb • Removed ByteSafe references • Changed DP and QE pins to NC • Updated ZZ recovery time diagram • Updated AC Test Conditions table and removed Output Load 2 diagram
8161Z18_r2_11; 8161Z18_r2_12	Content	• Removed Preliminary banner • Removed BSR table • Removed pin locations from pin description table
8161Z18_r2_12; 8161Z18_r2_13	Content	• Removed erroneous references to parity check • Added 165 BGA parts for x18 and x36; add x32 165 part • Update Abs Max table
8161Z18_r2_13; 8161Z18_r2_14	Content/Format	• Added missing JTAG pin descriptions to TQFP pin description table • Updated Synchronous Truth Table • Removed A and DQ numbers from pinouts • Updated timing diagrams • Added commercial "D" parts to ordering information table • Format updated
8161Z18_r2_14; 8161Z18_r2_15	Content/Format	• Updated format • Updated timing diagrams • Updated mechanical drawings