
HA19216/MP

6-Bit Flash Type Analog-to Digital Converter

HITACHI

Description

The HA19216/MP bipolar LSI performs high speed 6-bit A/D conversion. Digital data output and clock input terminals are compatible with TTL and CMOS. The HA19216/MP are designed for video signal processing application.

Features

- 6-bit resolution (including overflow)
- 6-bit latched three-state outputs
- Maximum conversion Rate: 20 Msps (Min)
- Single Power Supply: +5 V
- Digital data output, high impedance state control and clock input terminals compatible with TTL and CMOS
- Needs no sample and hold circuit
- 18-pin DIP package and 28-pin surface mount package.
- Output current:
 - $I_{OL} = 1.4$ mA (guaranteed)
 - $I_{OH} = -5$ mA (guaranteed)

Application

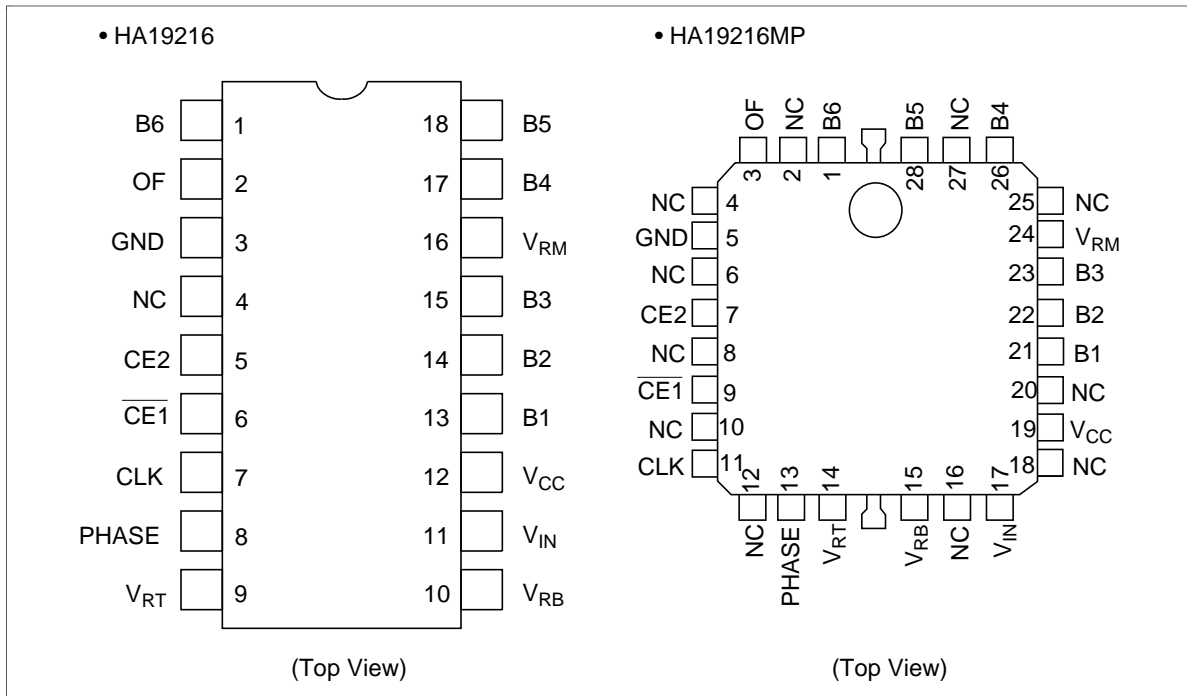
- Pattern recognition using a computer
- High-speed measuring instruments

Ordering Information

Type No.	Package
HA19216	300mil 18 pin plastic DIP (DP-18A)
HA19216MP	28 pin plastic QFI (MP-28)

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Pin Arrangement



Pin Function

Pin No.		Symbol	Function	Remarks
HA19216	HA19216MP			
1	1	B6	Bit 6 digital output (MSB)	
2	3	OF	Digital output (Overflow)	
3	5	GND	Ground	
4	—	NC	Not connected	
5	7	CE2	Digital output high	Impedance control input
6	9	$\overline{CE1}$	Digital output high	Impedance control input
7	11	CLK	Clock input	
8	13	PHASE	Clock phase control input	
9	14	V_{RT}	High level reference voltage input	
10	15	V_{BR}	Low level reference voltage input	
11	17	V_{IN}	Analog input	
12	19	V_{CC}	Power supply	
13	21	B1	Bit 1 digital output (LSB)	

Pin Function (Cont)

Pin No.		Symbol	Function	Remarks
HA19216	HA19216MP			
14	22	B2	Bit 2 digital output	
15	23	B3	Bit 3 digital output	
16	24	V _{RM}	Reference voltage center tap	
17	26	B4	Bit 4 digital output	
18	28	B5	Bit 5 digital output	

Note:

$\overline{\text{CE1}}$	CE2	B1 – B6	OF
x	L	Z	Z
L	H	H/L	H/L
H	H	Z	H/L

H: High level

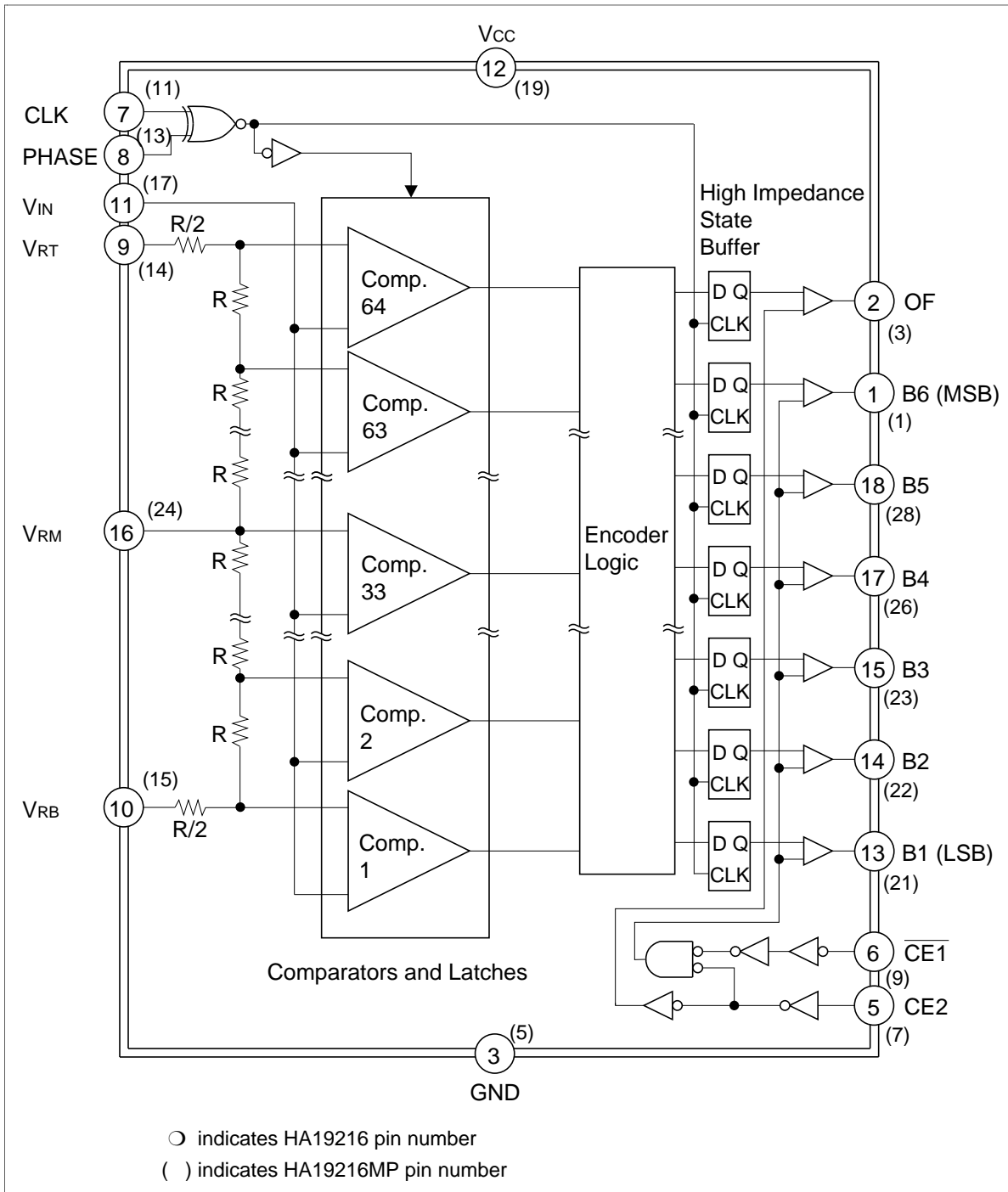
L: Low level

x: Don't care

Z: High impedance

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Block Diagram



Interface

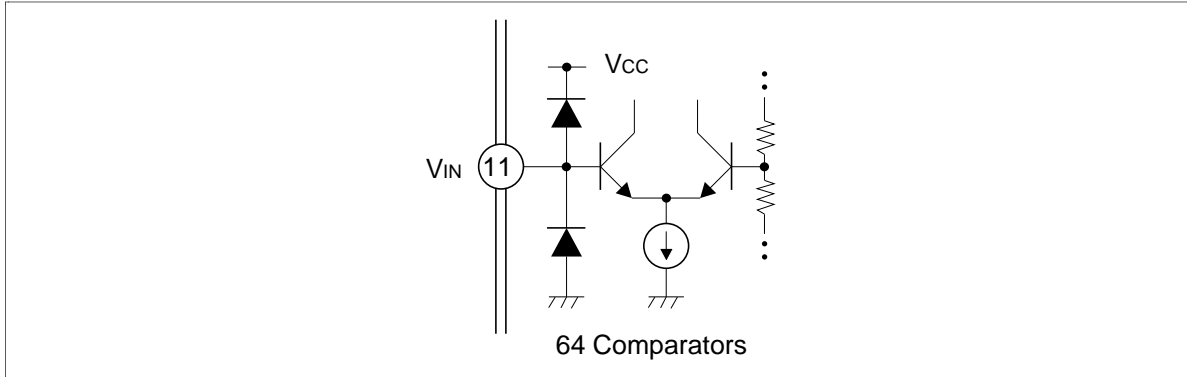


Figure 1 Analog Input

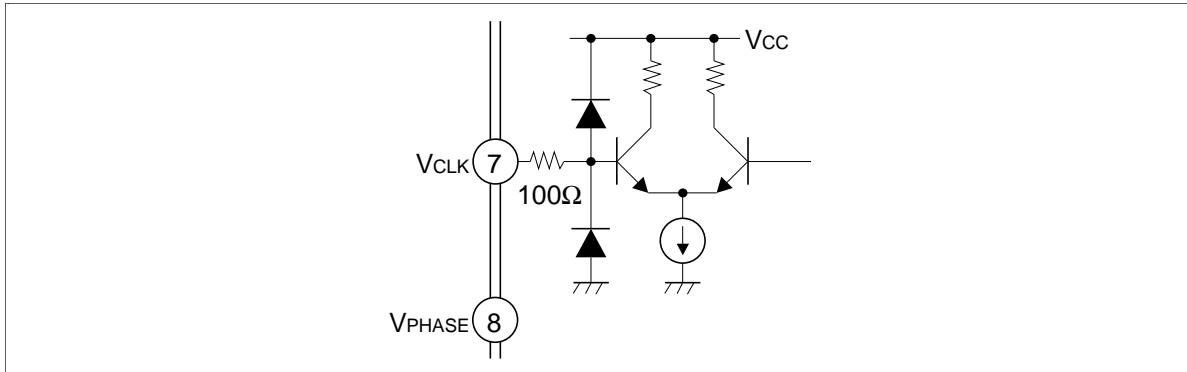


Figure 2 Clock Input

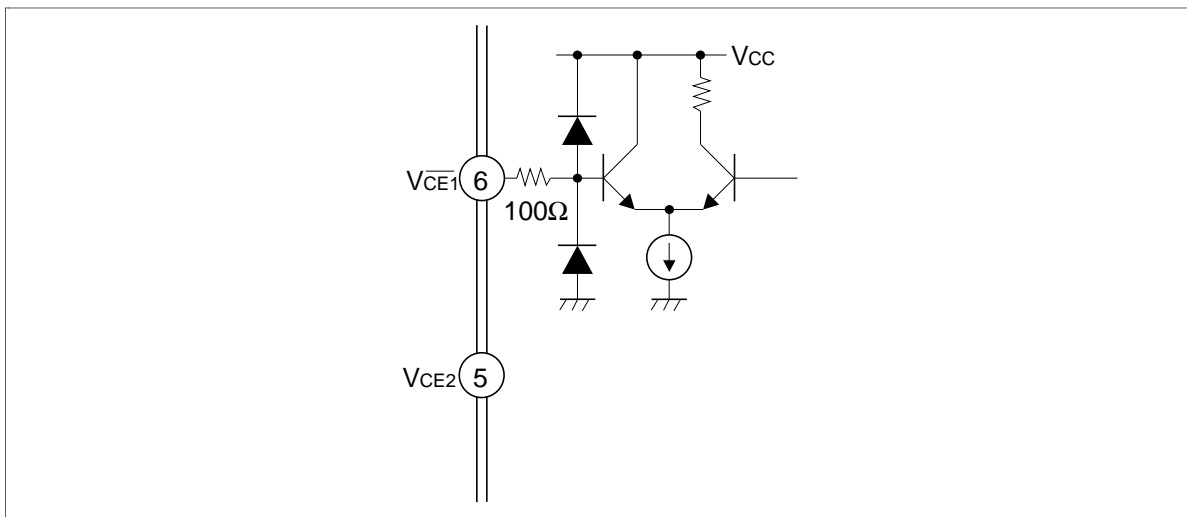


Figure 3 High Impedance State Control Input

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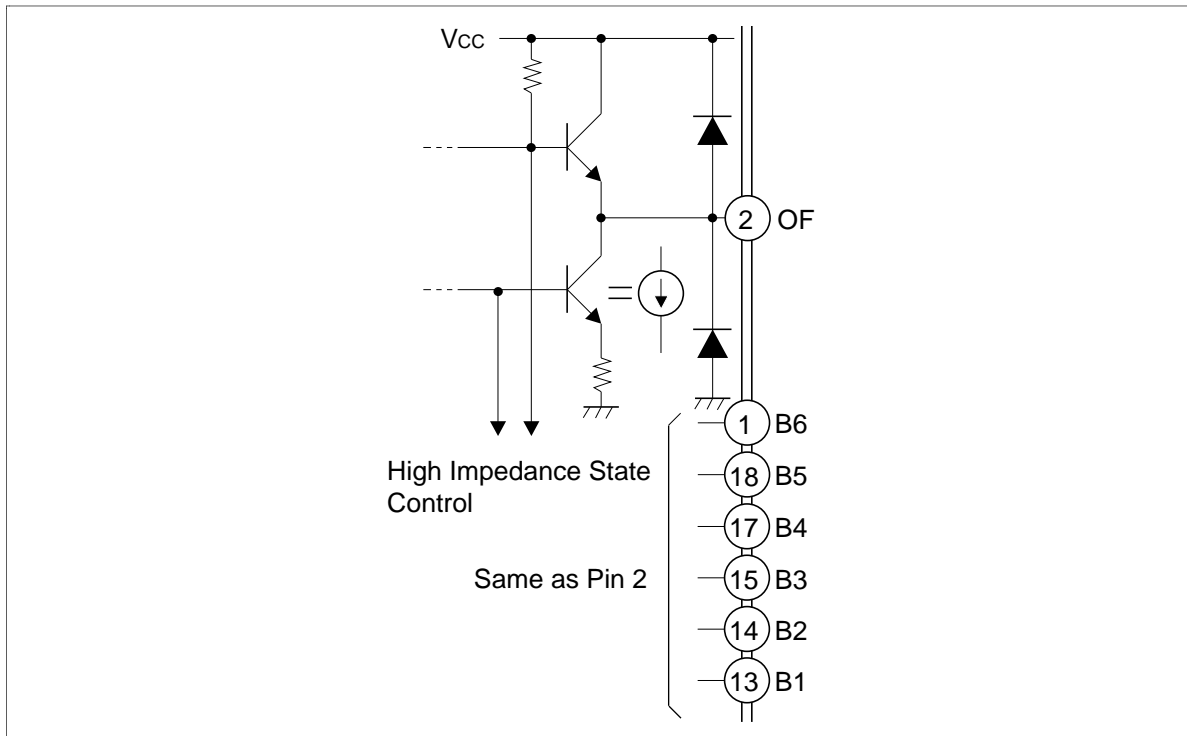


Figure 4 Digital Output

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$, unless otherwise specified)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	+7.0	V
Input signal voltage*	V_{IN}	0 to V_{CC}	V
Input reference voltage*	V_R	0 to V_{CC}	V
Digital input voltage	V_I	0 to V_{CC}	V
Voltage applied to digital output pin in high impedance	V_O	0 to V_{CC}	V
Power dissipation	P_T	550	mW
Operating temperature	T_{opr}	0 to +70	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +125	$^\circ\text{C}$
Reference voltage difference	$V_{RT} - V_{RB}$	1.3	V
Reference center tap voltage	V_{RM}	Open state voltage ± 0.1	V

Note: V_{IN} and V_R should not be lower than 1.5 V at the same time.

Electrical Characteristics ($T_a = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$, $V_{RT} = 3.0\text{ V}$, $V_{RB} = 2.0\text{ V}$, unless otherwise specified)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Resolution			6	6	6	bits	
Operating supply voltage		V_{CC}	4.75	5.0	5.25	V	
Quiescent current		I_{CC}	—	50	84	mA	$f_{CLK} = 20\text{ Msps}$
Digital input voltage	High	V_{IH}	2.0	—	V_{CC}	V	
	Low	V_{IL}	0	—	0.8	V	
Digital input current	High	I_{IH}	—	—	100	μA	$V_I = 2.7\text{ V}$
	Low	I_{IL}	-100	—	—	μA	$V_I = 0.4\text{ V}$
Digital output voltage	High	V_{OH}	3.4	3.8	—	V	$I_{OH} = -5\text{ mA}$
	Low	V_{OL}	—	0.61	0.76	V	$I_{OL} = 1.4\text{ mA}$
Digital output current (High impedance)	High	I_{OZH}	—	—	100	μA	$V_O = 5.0\text{ V}$
	Low	I_{OZL}	-100	—	—	μA	$V_O = 0.5\text{ V}$
Reference current	RT	I_{RT}	—	8	12	mA	$V_{IN} = 1.9\text{ V}$
	RB	I_{RB}	-12	-8	—	mA	$V_{IN} = 3.1\text{ V}$
Input current		I_{IN}	—	20	50	μA	$V_{IN} = 3.1\text{ V}$
Input capacitance		C_{IN}	—	15	—	pF	$V_{RB} < V_{IN} < V_{RT}$, $f(V_{IN}) = 1\text{ MHz}$
Static linearity error	Differential	D.N.L.	-0.25	—	+0.25	LSB	
	Integral	I.N.L.	—	—	1.0	LSB _{p,p}	
Maximum conversion rate		f_{CLK} max.	20	—	—	Msps	
Digital output propagation delay		t_{PD}	—	34	50	ns	$C_L = 15\text{ pF}$
Digital output rise time		t_{TLH}	—	10	15	ns	$C_L = 15\text{ pF}$
Digital output fall time		t_{THL}	—	17	25	ns	$C_L = 15\text{ pF}$
Digital output enable time (High impedance)		t_{ZH}	—	12	20	ns	
		t_{ZL}	—	48	70	ns	
Digital output disable time (High impedance)		t_{HZ}	—	32	43	ns	
		t_{LZ}	—	23	33	ns	
Clock pulse width	Vphase = 0.8 V	t_{WH}	28	32	—	ns	
		t_{WL}	15	18	—	ns	
	Vphase = 2.0V	t_{WH}	10	13	—	ns	
		t_{WL}	33	37	—	ns	

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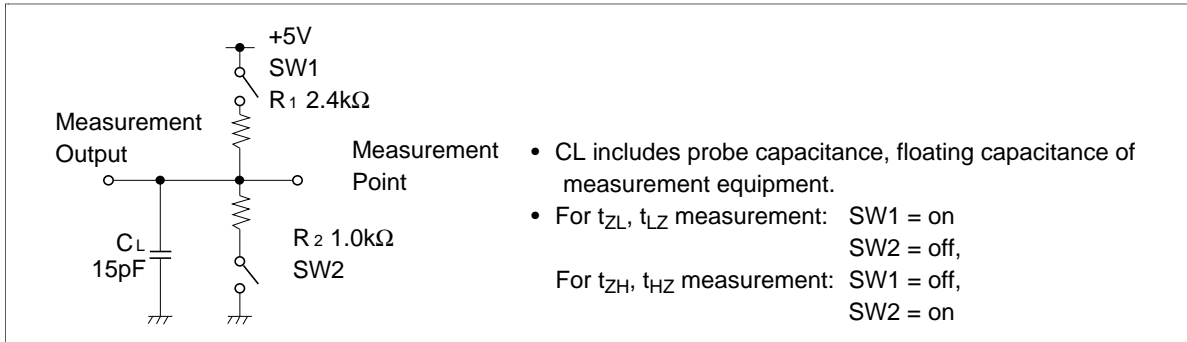


Figure 5 Measurement Load for Digital Output, Enable Time, Disable Time

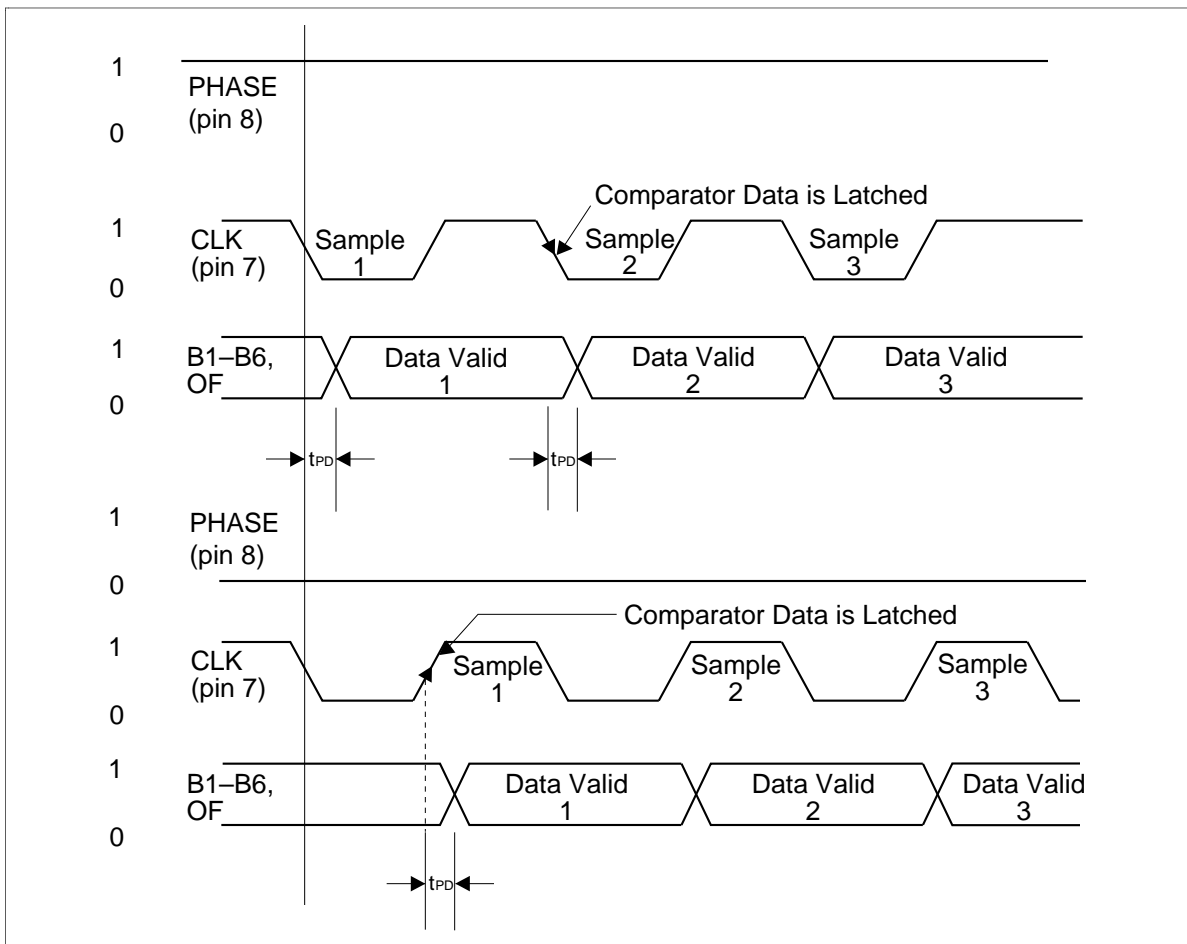


Figure 6 Timing Diagram

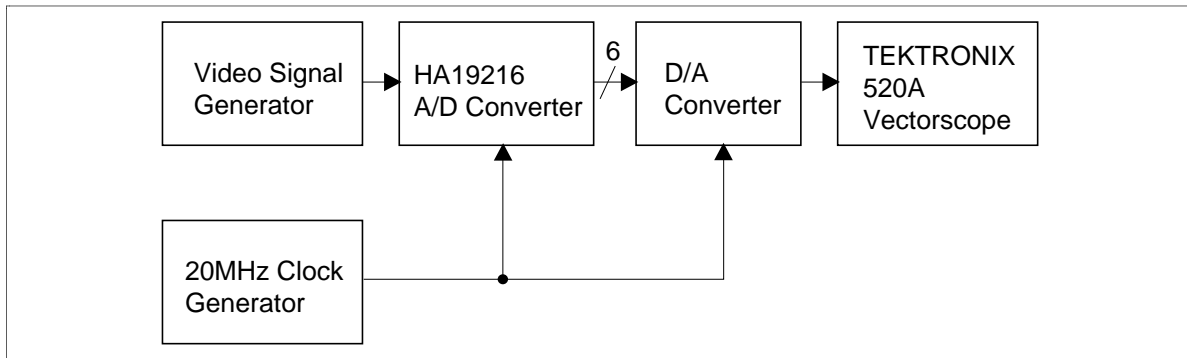


Figure 7 Measuring Circuit for DG and DP

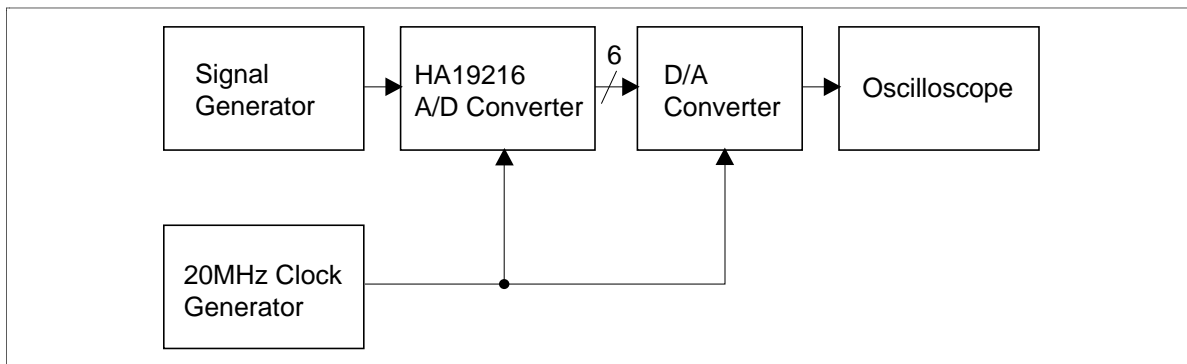


Figure 8 Measuring Circuit for Analog Input Frequency Response

High Frequency Input Response

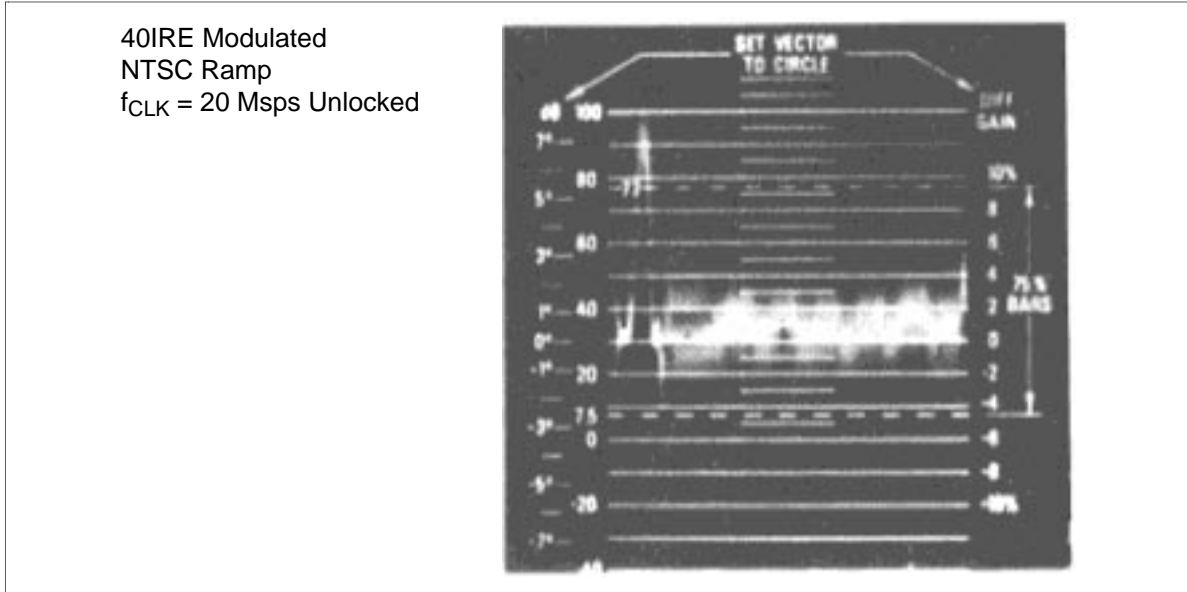


Figure 9 High Frequency Analog Input Response Differential Phase

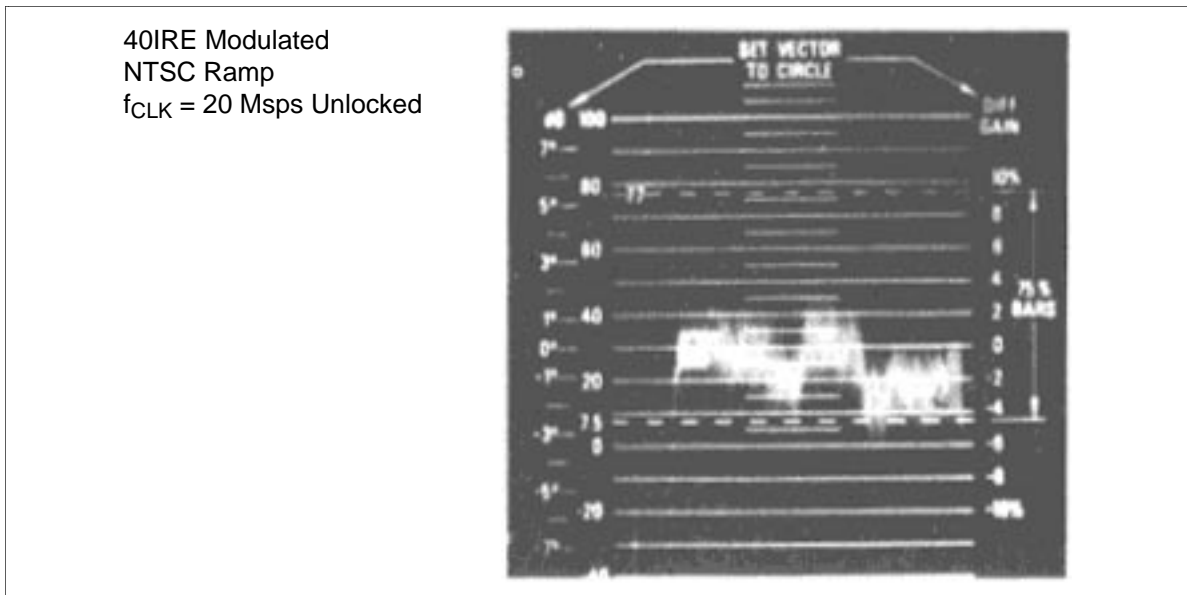


Figure 10 High Frequency Analog Input Response Differential Gain

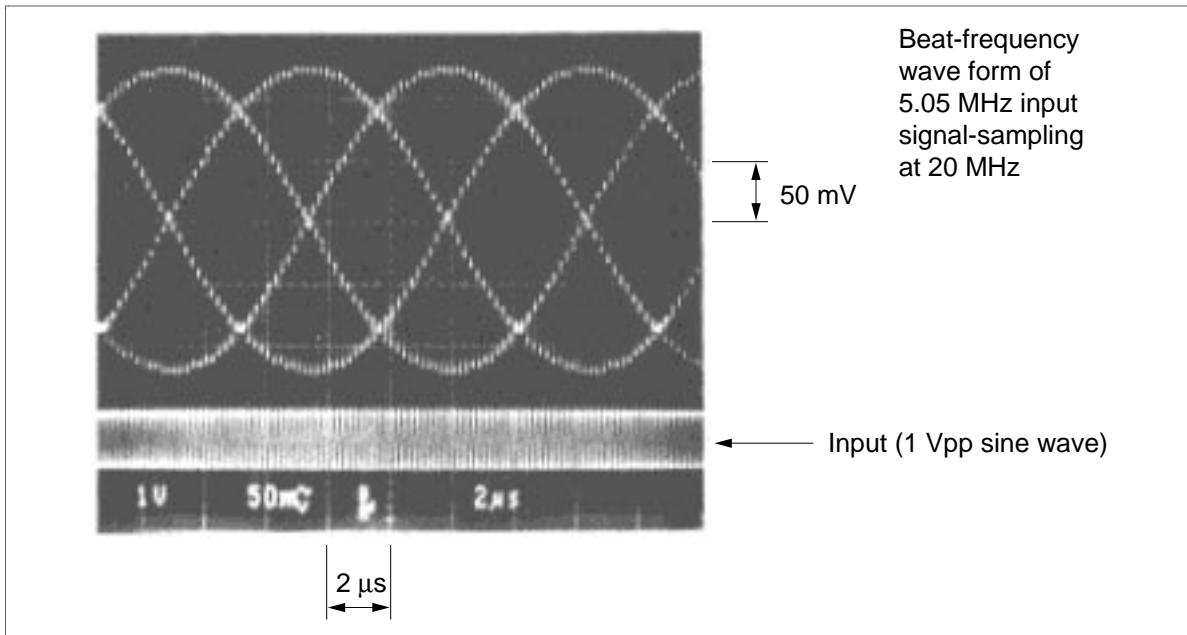


Figure 11 Beat-Frequency Waveform of 5.05 MHz Input Signal-Sampled at 20 MHz

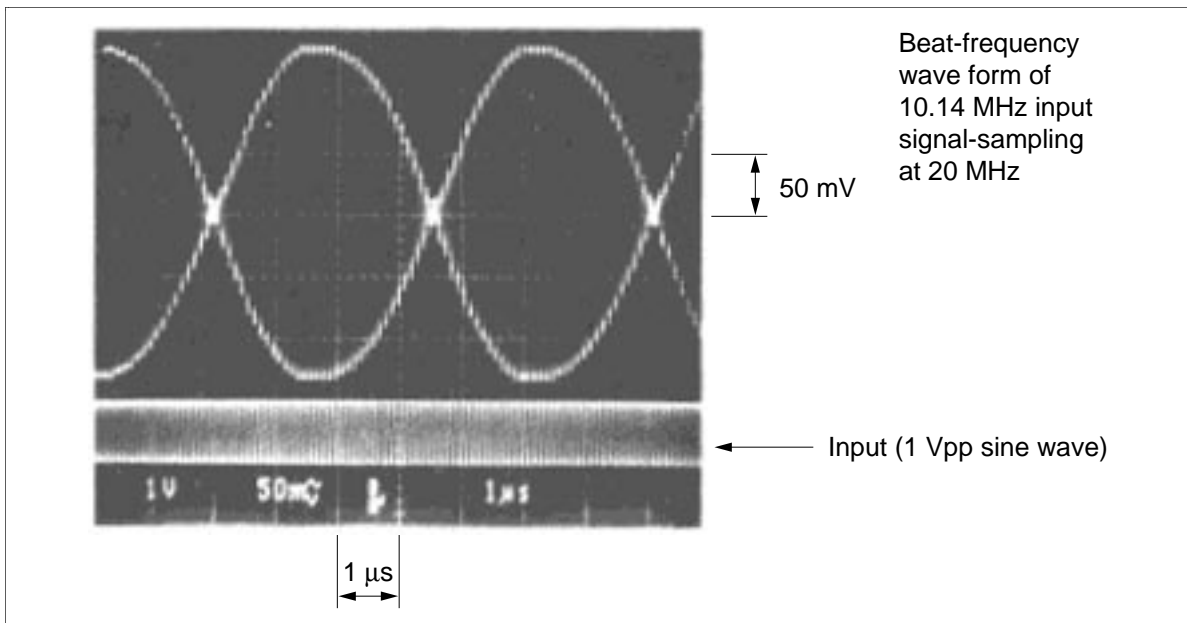


Figure 12 Beat-Frequency Waveform of 10.14 MHz Input Signal-Sampled at 20 MHz

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