

Uncompensated, High Slew Rate High Output Current, Operational Amplifier

July 1997

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- High Slew Rate 135V/ μ s (Min)
150V/ μ s (Typ)
- High Output Current \pm 30mA (Min)
- High Gain-Bandwidth Product 15MHz (Min)
20MHz(Typ)
- Wide Power Bandwidth 2.1MHz (Min)
- High Input Impedance 50M Ω (Min)
130M Ω (Typ)
- Low Offset Current 25nA (Max)
5nA (Typ)
- Fast Settling (10V Step to 0.1%) 200ns (Typ)
- Low Quiescent Supply Current 6mA (Max)

Applications

- Data Acquisition Systems
- RF Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

Description

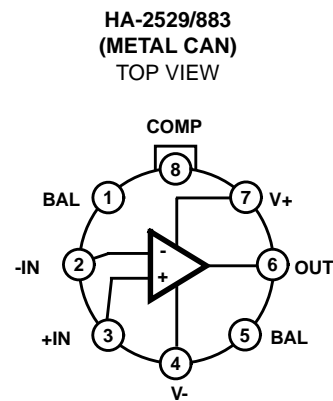
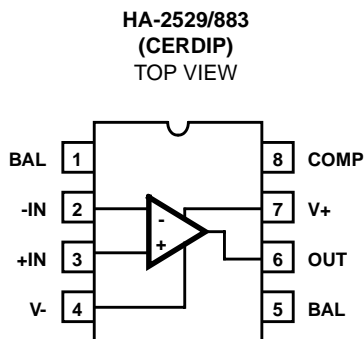
The HA-2529/883 is a monolithic operational amplifier which typifies excellence of design. With a design based on years of experience coupled with the reliable dielectric isolation process, these amplifiers provide an outstanding combination of DC and AC parameters at closed loop gains of 3 or greater without external compensation.

The HA-2529/883 offers 135V/ μ s (min) slew rate and fast settling time (200ns typ), while consuming a mere 6mA (max) quiescent supply current, making these amplifiers ideal components for video circuitry and data acquisition designs. With 15MHz minimum gain-bandwidth product combined with 7.5kV/V minimum open loop gain, the HA-2529/883 is an ideal component for demanding signal conditioning designs. These devices provide \pm 30mA (min) output current drive with an output voltage swing of \pm 10V (min), making them suited for pulse amplifier and RF amplifier components. HA-2529/883 will upgrade a system presently using the HA-2520/22/883 or EHA-2520/22/883 in regards to output current, slew rate, offset voltage drift, and offset current drift. To insure compliance with slew rate and transient response specifications, all devices are 100% tested for AC performance characteristics over full temperature.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA2-2529/883	-55 to 125	8 Pin Metal Can	T8.C
HA7-2529/883	-55 to 125	8 Ld CERDIP	F8.3A

Pinouts



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$

Voltage Between V+ and V- Terminals	40V
Differential Input Voltage.....	15V
Voltage at Either Input Terminal	V+ to V-
Peak Output Current50mA
ESD Rating.....	<2000V

Operating Conditions

Temperature Range	-55°C to 125°C
Supply Voltage	±15V
$V_{INCM} \leq 1/2 (V+ - V-)$	
$R_L \geq 500\Omega$	

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA}	θ_{JC}
CERDIP Package	115°C/W	28°C/W
Metal Can Package	160°C/W	75°C/W
Package Power Dissipation Limit at 75°C for $T_J \leq 175^\circ\text{C}$		
CERDIP Package	870mW	
Metal Can Package	625mW	
Package Power Dissipation Derating Factor Above 75°C		
CERDIP Package	8.7mW/°C	
Metal Can Package	6.3mW/°C	
Maximum Junction Temperature	175°C	
Maximum Storage Temperature Range	-65°C to 150°C	
Maximum Lead Temperature (Soldering 10s).....	300°C	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $V_{SUPPLY} = \pm 15V$, $R_{SOURCE} = 100\Omega$, $R_{LOAD} = 500k\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMP. (°C)	MIN	MAX	UNITS
Input Offset Voltage	V_{IO}	$V_{CM} = 0V$	1	25	-5	5	mV
			2, 3	125, -55	-8	8	mV
Input Bias Current	+ I_B	$V_{CM} = 0V$, $+R_S = 100k\Omega$, $-R_S = 100k\Omega$	1	25	-200	200	nA
			2, 3	125, -55	-400	400	nA
	- I_B	$V_{CM} = 0V$, $+R_S = 100k\Omega$, $-R_S = 100k\Omega$	1	25	-200	200	nA
			2, 3	125, -55	-400	400	nA
Input Offset Current	I_{IO}	$V_{CM} = 0V$, $+R_S = 100k\Omega$, $-R_S = 100k\Omega$	1	25	-25	25	nA
			2, 3	125, -55	-50	50	nA
Common Mode Range	+CMR	$V+ = 5V$, $V- = -25V$	1	25	+10	-	V
			2, 3	125, -55	+10	-	V
	-CMR	$V+ = 25V$, $V- = -5V$	1	25	-	-10	V
			2, 3	125, -55	-	-10	V
Large Signal Voltage Gain	+ A_{VOL}	$V_{OUT} = 0V$ and +10V, $R_L = 2k\Omega$	4	25	10	-	kV/V
			5, 6	125, -55	7.5	-	kV/V
	- A_{VOL}	$V_{OUT} = 0V$ and -10V, $R_L = 2k\Omega$	4	25	10	-	kV/V
			5, 6	125, -55	7.5	-	kV/V
Common Mode Rejection Ratio	+CMRR	$\Delta V_{CM} = +10V$, $V+ = +5V$, $V- = -25V$, $V_{OUT} = -10V$	1	25	83	-	dB
			2, 3	125, -55	80	-	dB
	-CMRR	$\Delta V_{CM} = -10V$, $V+ = +25V$, $V- = -5V$, $V_{OUT} = +10V$	1	25	83	-	dB
			2, 3	125, -55	80	-	dB
Output Voltage Swing	+ V_{OUT}	$R_L = 2k\Omega$	4	25	10	-	V
			5, 6	125, -55	10	-	V
	- V_{OUT}	$R_L = 2k\Omega$	4	25	-	-10	V
			5, 6	125, -55	-	-10	V

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TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: $V_{SUPPLY} = \pm 15V$, $R_{SOURCE} = 100\Omega$, $R_{LOAD} = 500k\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMP. (°C)	MIN	MAX	UNITS
Output Current	+I _{OUT}	V _{OUT} = -10V	4	25	30	-	mA
			5, 6	125, -55	20	-	mA
	-I _{OUT}	V _{OUT} = +10V	4	25	-	-30	mA
			5, 6	125, -55	-	-20	mA
Quiescent Power Supply Current	+I _{CC}	V _{OUT} = 0V, I _{OUT} = 0mA	1	25	-	6	mA
			2, 3	125, -55	-	7	mA
	-I _{CC}	V _{OUT} = 0V, I _{OUT} = 0mA	1	25	-6	-	mA
			2, 3	125, -55	-7	-	mA
Power Supply Rejection Ratio	+PSRR	$\Delta V_{SUP} = 10V$, V ₊ = +20V, V ₋ = -15V, V ₊ = +10V, V ₋ = -15V	1	25	80	-	dB
			2, 3	125, -55	80	-	dB
	-PSRR	$\Delta V_{SUP} = 10V$, V ₊ = +15V, V ₋ = -20V, V ₊ = +15V, V ₋ = -10V	1	25	80	-	dB
			2, 3	125, -55	80	-	dB
Offset Voltage Adjustment	+V _{IOAdj}	Note 2	1	25	V _{IO-1}	-	mV
			2, 3	125, -55	V _{IO-1}	-	mV
	-V _{IOAdj}	Note 2	1	25	V _{IO+1}	-	mV
			2, 3	125, -55	V _{IO+1}	-	mV

NOTE:

- Offset adjustment range is [V_{IO} (Measured) ±1mV] minimum referred to output. This test is for functionality only to assure adjustment through 0V.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $V_{SUPPLY} = \pm 15V$, $R_{SOURCE} = 50\Omega$, $R_{LOAD} = 2k\Omega$, $C_{LOAD} = 50pF$, $A_{VCL} = +3V/V$, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMP. (°C)	MIN	MAX	UNITS
Slew Rate	+SR	V _{OUT} = -5V to +5V 25% ≤ +SR ≤ 75%	7	25	135	-	V/μs
			8A, 8B	125, -55	125	-	V/μs
	-SR	V _{OUT} = +5V to -5V 75% ≥ -SR ≥ 25%	7	25	135	-	V/μs
			8A, 8B	125, -55	125	-	V/μs
Rise and Fall Time	t _r	V _{OUT} = 0 to +200mV 10% ≤ t _r ≤ 90%	7	25	-	45	ns
			8A, 8B	125, -55	-	50	ns
	t _f	V _{OUT} = 0 to -200mV 10% ≤ t _f ≤ 90%	7	25	-	45	ns
			8A, 8B	125, -55	-	50	ns
Overshoot	+OS	V _{OUT} = 0 to +200mV	7	25	-	40	%
			8A, 8B	125, -55	-	40	%
	-OS	V _{OUT} = 0 to -200mV	7	25	-	40	%
			8A, 8B	125, -55	-	40	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: $V_{SUPPLY} = \pm 15V$, $R_{LOAD} = 2k\Omega$, $C_{LOAD} = 50pF$, $C_{COMP} = 0pF$, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMP. (°C)	MIN	MAX	UNITS
Differential Input Resistance	R_{IN}	$V_{CM} = 0V$	3	25	50	-	$M\Omega$
Gain Power Bandwidth	GBWP	$V_O = 200mV$, $f_O \geq 10kHz$	3	25	15	-	MHz
Full Power Bandwidth	FPBW	$V_{PEAK} = 10V$	3, 4	25	2.1	-	MHz
Minimum Closed Loop Stable Gain	CLSG	$R_L = 2k\Omega$, $C_L = 50pF$	3	-55 to 125	± 3	-	V/V
Output Resistance	R_{OUT}	Open Loop	3	25	-	60	Ω
Power Consumption	PC	$V_{OUT} = 0V$, $I_{OUT} = 0mA$	3, 5	-55 to 125	-	210	mW

NOTES:

3. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
4. Full Power Bandwidth guarantee based on Slew Rate measurement using $FPBW = \text{Slew Rate} / (2\pi V_{PEAK})$.
5. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 AND 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 6), 2, 3, 4, 5, 6, 7, 8A, 8B
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7, 8A, 8B
Groups C and D Endpoints	1

NOTE:

6. PDA applies to Subgroup 1 only.

Die Characteristics

DIE DIMENSIONS:

67 mils x 57 mils x 19 mils
1700µm x 1440µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:

Type: Nitride (Si3N4) over Silox (SiO2, 5% Phos.)
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1.5kÅ

WORST CASE CURRENT DENSITY:

$0.78 \times 10^5 \text{ A/cm}^2$

SUBSTRATE POTENTIAL (Powered Up):

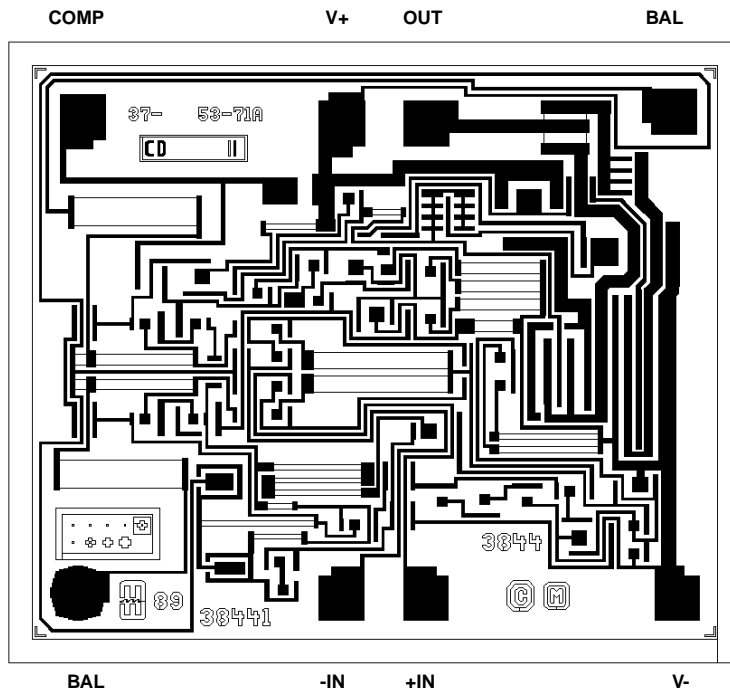
Unbiased

TRANSISTOR COUNT: 40

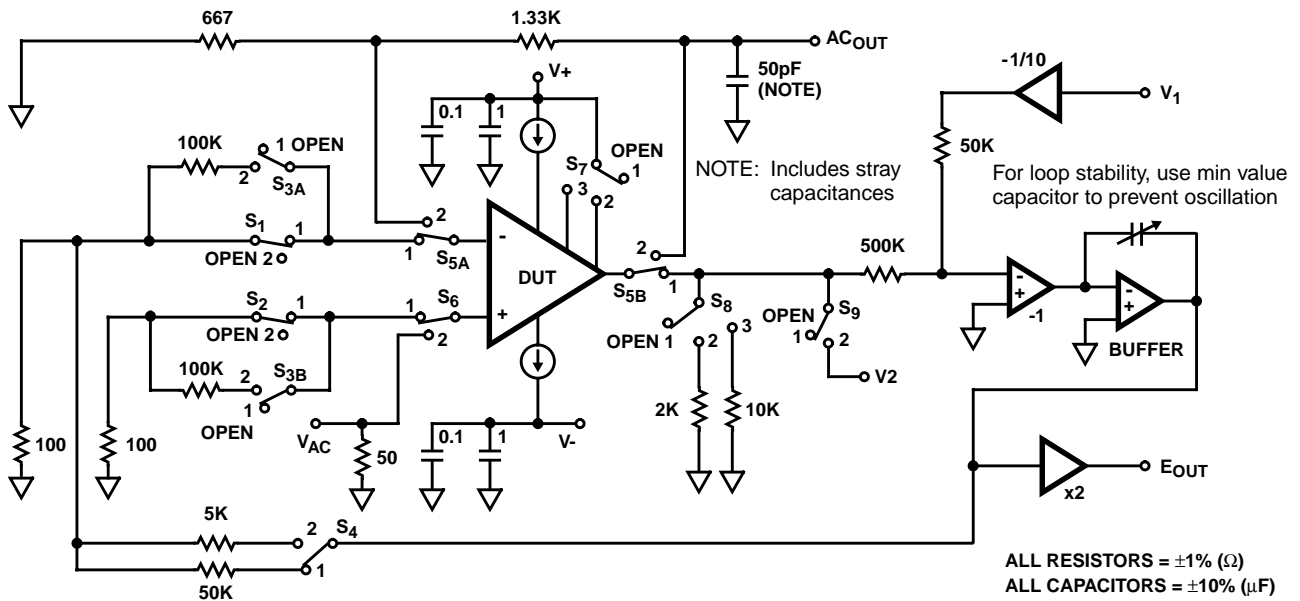
PROCESS: Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2529/883



Test Circuit (Applies to Tables 1 and 2)



Test Circuits and Waveforms

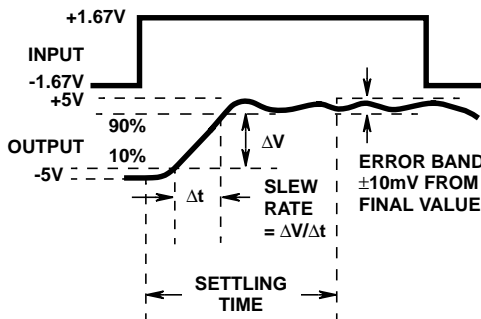
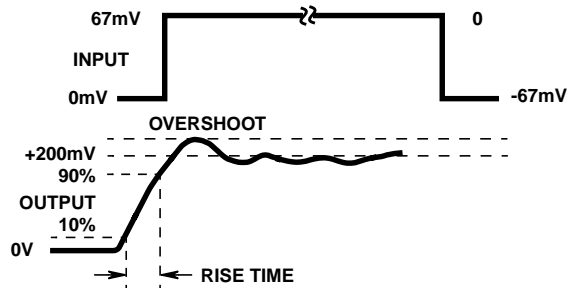


FIGURE 1. SLEW RATE AND SETTling TIME



NOTE: Measured on both positive and negative transitions from 0V to +200mV and 0V to -200mV at the output.

FIGURE 2. TRANSIENT RESPONSE

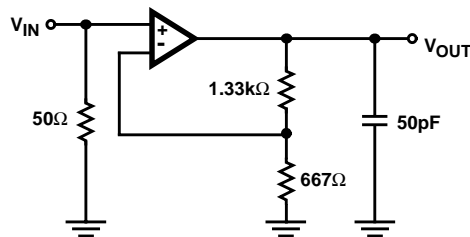
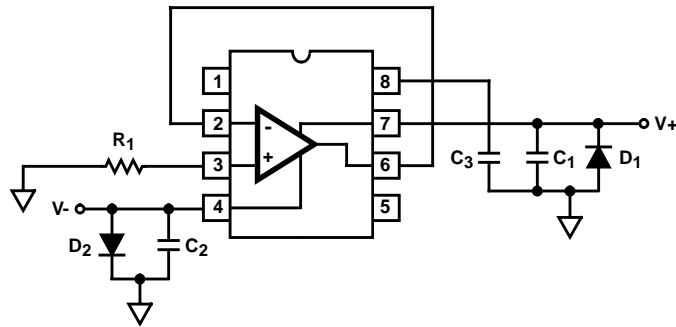


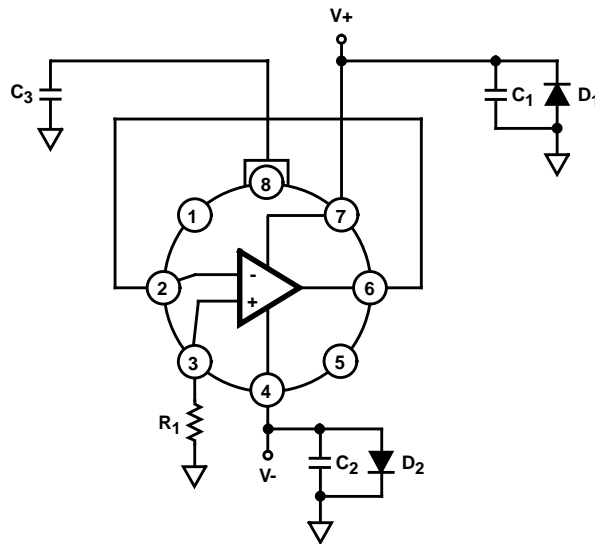
FIGURE 3. SIMPLIFIED TEST CIRCUIT (APPLIES TO TABLE 2)

Burn-In Circuits

HA7-2529/883 Cerdip



HA2-2529/883 METAL CAN



NOTES:

$R_1 = 1M\Omega, \pm 5\%, 1/4W$ (Min)

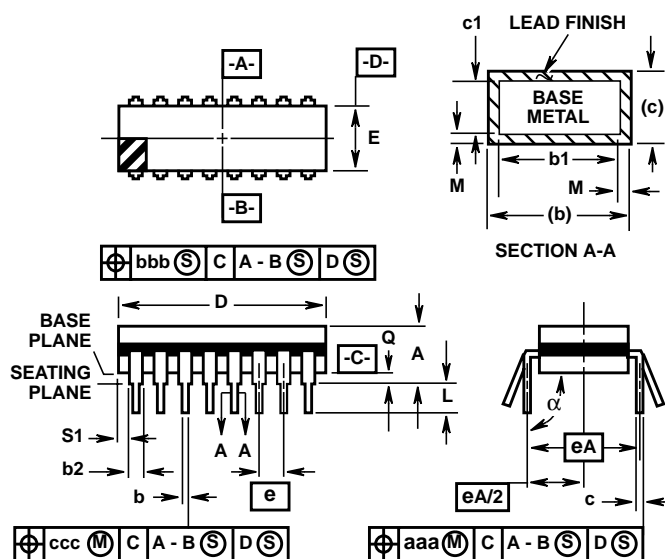
$C_1 = C_2 = 0.01\mu F$ /Socket (Min) or $0.1\mu F$ /Row (Min)

$C_3 = 0.01\mu F$ /Socket (10%)

$D_1 = D_2 = 1N4002$ or Equivalent/Board

$|(V+) - (V-)| = 30V$

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



**F8.3A MIL-STD-1835 GDIP1-T8 (D-4, CONFIGURATION A)
8 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE**

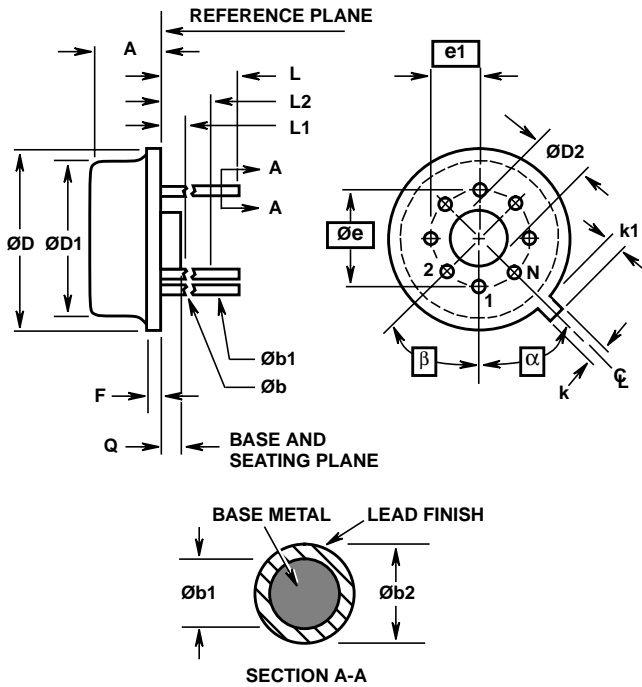
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	8		8		8

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

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Metal Can Packages (Can)



**T8.C MIL-STD-1835 MACY1-X8 (A1)
8 LEAD METAL CAN PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	-
$\varnothing b$	0.016	0.019	0.41	0.48	1
$\varnothing b1$	0.016	0.021	0.41	0.53	1
$\varnothing b2$	0.016	0.024	0.41	0.61	-
$\varnothing D$	0.335	0.375	8.51	9.40	-
$\varnothing D1$	0.305	0.335	7.75	8.51	-
$\varnothing D2$	0.110	0.160	2.79	4.06	-
e	0.200 BSC		5.08 BSC		-
e1	0.100 BSC		2.54 BSC		-
F	-	0.040	-	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
Q	0.010	0.045	0.25	1.14	-
α	45° BSC		45° BSC		3
β	45° BSC		45° BSC		3
N	8		8		4

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NOTES:

1. (All leads) $\varnothing b$ applies between L1 and L2. $\varnothing b1$ applies between L2 and 0.500 from the reference plane. Diameter is uncontrolled in L1 and beyond 0.500 from the reference plane.
2. Measured from maximum diameter of the product.
3. α is the basic spacing from the centerline of the tab to terminal 1 and β is the basic spacing of each lead or lead position (N - 1 places) from α , looking at the bottom of the package.
4. N is the maximum number of terminal positions.
5. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
6. Controlling dimension: INCH.

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