HEWLETT PACKARD

40 ns Prop. Delay, SO-8 Optocoupler

Preliminary Technical Data

HCPL-0710

Features

- **+5 V CMOS Compatibility**
- **8 ns Pulse Width Distortion**
- **High Speed: 12 Mbd**
- **10 kV/μs Minimum Common Mode Rejection**
- **Industrial Temperature Range: 0°C to 85°C**
- **Safety and Regulatory Approvals**
  UL Recognized 2500 V rms for 1 min. per UL 1577
  CSA Component Acceptance Notice #5

Applications

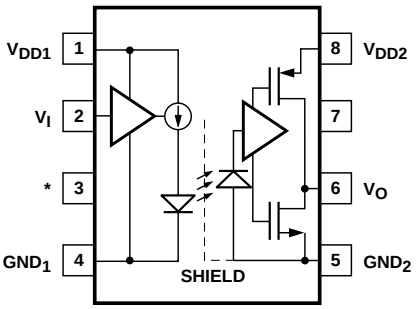
- **Digital Fieldbus Isolation: DeviceNet, SDS, PROFIBUS**
- **Multiplexed Data Transmission**
- **Computer Peripheral Interface**
- **Microprocessor System Interface**

Description

Available in the SO-8 package style, the HCPL-0710 optocoupler utilizes the latest CMOS IC technology to achieve outstanding performance with very low power consumption. The HCPL-0710 requires only two bypass capacitors for complete CMOS compatibility.

Basic building blocks of the HCPL-0710 are a CMOS LED driver IC and a CMOS detector IC. A CMOS logic input signal controls the LED driver IC which supplies current to the LED. The detector IC incorporates an integrated photodiode, a high-speed transimpedance amplifier, and a voltage comparator with an output driver.

Functional Diagram



TRUTH TABLE

V_I, INPUT	V_I, OUTPUT
H	H
L	L

*Pin 3 is the anode of the internal LED and must be left unconnected for guaranteed data sheet performance. Pin 7 is not connected internally. External connections to pin 7 are not recommended.
***A 0.1 μF bypass capacitor must be connected between pins 1 and 4, and 5 and 8.*

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

This data sheet represents the latest information at the time of publication of this catalog. All specifications subject to change. Samples available Fall 1996.

Electrical Specifications

Unless otherwise noted, all specifications are guaranteed across recommended operating conditions. All Typical specifications are at T_A = +25°C, V_{DD1} = V_{DD2} = +5 V. Test conditions that are not specified can be anywhere within the recommended operating range.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
DC Specifications						
Logic Low Input Supply Current	I_{DDIL}		1.5	3.0	mA	V_{DD1} = 5.5 V, V_I = 0 V
Logic High Input Supply Current	I_{DDIH}		6.0	10.0	mA	V_{DD1} = 5.5 V, V_I = V_{DDI}
Input Supply Current	I_{DDI}			13.0	mA	V_{DD1} = 5.5 V
Output Supply Current	I_{DD2}		5.5	10.0	mA	V_{DD2} = 5.5 V
Input Current	I_I	-10		10	µA	
Logic High Output Voltage	V_{OH}	V_{DD2} - 0.1	V_{DD2}		V	I_O = -20 µA, V_I = V_{IH}
		0.8 *V_{DD2}	4.5			I_O = -4 mA, V_I = V_{IH}
Logic Low Output Voltage	V_{OL}		0	0.1	V	I_O = 20 µA, V_I = V_{IL}
			0.2	0.8		I_O = 4 mA, V_I = V_{IL}
Switching Specifications						
Propagation Delay Time to Logic Low Output	t_{PHL}		20	40	ns	C_L = 15 pF CMOS Signal Levels
Propagation Delay Time to Logic High Output	t_{PLH}		23	40		
Pulse Width	PW	80				
Data Rate				12.5	MBd	
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD		3	8	ns	C_L = 15 pF CMOS Signal Levels
Propagation Delay Skew	t_{PSK}			20		
Output Rise Time (10 - 90%)	t_R		13			C_L = 15 pF CMOS Signal Levels
Output Fall Time (90 - 10%)	t_F		5			
Common Mode Transient Immunity at Logic High Output	$\lvert CM_H \rvert$	10	20		kV/µs	V_I = V_{DDI}, V_O > 0.8 V_{DDI}, V_{CM} = 1000 V
Common Mode Transient Immunity at Logic Low Output	$\lvert CM_L \rvert$	10	20			V_I = 0 V, V_O > 0.8 V, V_{CM} = 1000 V
Input Dynamic Power Dissipation Capacitance	C_{PD1}		60		pF	
Output Dynamic Power Dissipation Capacitance	C_{PD2}		10			