# HD74AC164/HD74ACT164

Serial-In, Parallel-Out Shift Register

HITACHI

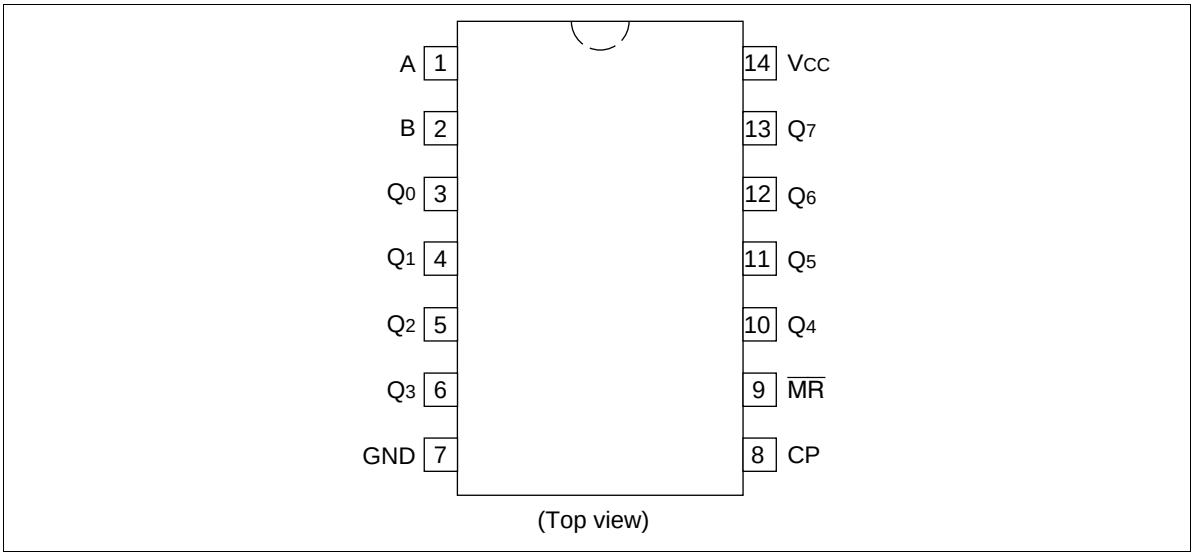
## Description

The HD74AC164/HD74ACT164 is a high-speed 8-bit serial-in/parallel-out shift register. Serial data is entered through a 2-input AND gate synchronous with the Low-to-High transition of the clock. The device features an asynchronous Master Reset which clears the register, setting all outputs Low independent of the clock.

## Features

- Outputs Source/Sink 24 mA
- HD74ACT164 has TTL-Compatible Inputs

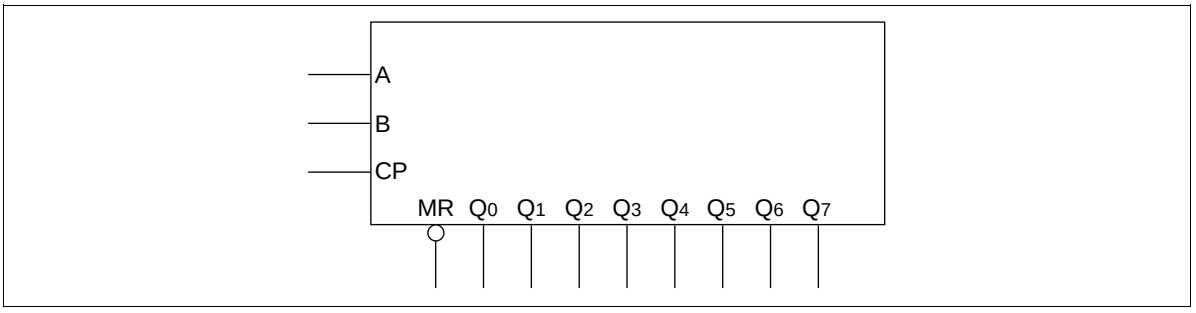
## Pin Arrangement




(Top view)

Hitachi semiconductor

## Logic Symbol




## Pin Names

| | |
|---|---|
| A, B | Data Inputs |
| CP | Clock Pulse Input (Active Rising Edge) |
| $\overline{MR}$ | Master Reset Input (Active Low) |
| $Q_0$ to $Q_7$ | Outputs |

## Functional Description

The HD74AC164/HD74ACT164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active High Enable for data entry through the other inputs. An unused input must be tied High.

Each Low-to-High transition on the Clock (CP) input shifts data one place to the right and enters into $Q_0$ the logical AND of the two data inputs (A•B) that existed before the rising clock edge. A Low level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs Low.

## Mode Select Table

| | Inputs | | | Outputs | |
|---|---|---|---|---|---|
| **Operating Mode** | **$\overline{MR}$** | **A** | **B** | **$Q_0$** | **$Q_1$ to $Q_7$** |
| Reset (Clear) | L | X | X | L | L to L |
| Shift | H | L | L | L | $q_0$ to $q_6$ |
| | H | L | H | L | $q_0$ to $q_6$ |
| | H | H | L | L | $q_0$ to $q_6$ |
| | H | H | H | H | $q_0$ to $q_6$ |

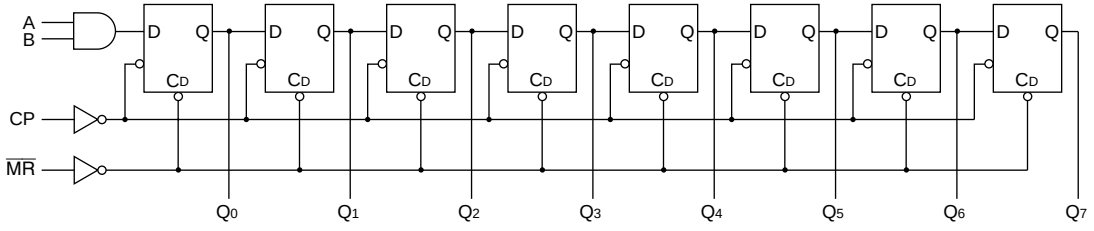
H : High Voltage Level

L : Low Voltage Level

X : Immaterial

$q_n$ : Lower case letters indicate the state of the referenced input or output one setup time prior to the Low-to-High clock transition.

## Logic Diagram




Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## DC Characteristics (unless otherwise specified)

| Item | Symbol | Max | Unit | Condition |
|---|---|---|---|---|
| Maximum quiescent supply current | $I_{CC}$ | 80 | µA | $V_{IN}$ = $V_{CC}$ or ground, $V_{CC}$ = 5.5 V, Ta = Worst case |
| Maximum quiescent supply current | $I_{CC}$ | 8.0 | µA | $V_{IN}$ = $V_{CC}$ or ground, $V_{CC}$ = 5.5 V, Ta = 25°C |
| Maximum additional $I_{CC}$/input (HD74ACT164) | $I_{CCT}$ | 1.5 | mA | $V_{IN}$ = $V_{CC}$ – 2.1 V, $V_{CC}$ = 5.5 V, Ta = Worst case |

## AC Characteristics: HD74AC164

| Item | Symbol | $V_{CC}$ (V)*[1] | Ta = +25°C, $C_L$ = 50 pF | | | Ta = –40°C to +85°C, $C_L$ = 50 pF | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| Maximum clock | $f_{max}$ | 3.3 | 125 | — | — | 100 | — | MHz |
| frequency | | 5.0 | 150 | — | — | 125 | — | |
| Propagation delay | $t_{PLH}$ | 3.3 | 1.0 | 8.5 | 13.0 | 1.0 | 13.5 | ns |
| CP to $Q_n$ | | 5.0 | 1.0 | 6.5 | 10.0 | 1.0 | 10.5 | |
| Propagation delay | $t_{PHL}$ | 3.3 | 1.0 | 8.5 | 13.0 | 1.0 | 14.5 | |
| CP to $Q_n$ | | 5.0 | 1.0 | 6.5 | 10.0 | 1.0 | 10.5 | |
| Propagation delay | $t_{PHL}$ | 3.3 | 1.0 | 9.5 | 16.0 | 1.0 | 18.0 | |
| $\overline{MR}$ to $Q_n$ | | 5.0 | 1.0 | 7.5 | 11.5 | 1.0 | 13.5 | |

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

## AC Operating Requirements: HD74AC164

| Item | Symbol | $V_{CC}$ (V)*[1] | Ta = +25°C, $C_L$ = 50 pF | Ta = –40°C to +85°C, $C_L$ = 50 pF | | Unit |
|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Minimum | | |
| Setup time A or B to CP | $t_{su}$ | 3.3 | 3.0 | 5.5 | 6.0 | ns |
| | | 5.0 | 2.0 | 4.6 | 4.5 | |
| Hold time CP to A or B | $t_h$ | 3.3 | –1.5 | 0.0 | 0.0 | |
| | | 5.0 | –1.5 | 0.0 | 0.0 | |
| Pulse width CP or $\overline{MR}$ | $t_w$ | 3.3 | 2.0 | 5.5 | 7.0 | |
| | | 5.0 | 2.0 | 4.5 | 5.0 | |
| Recovery time $\overline{MR}$ or CP | $t_{rec}$ | 3.3 | –2.5 | 0.0 | 0.0 | |
| | | 5.0 | –1.5 | 0.0 | 0.0 | |

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

## AC Characteristics: HD74ACT164

| | | | Ta = +25°C $C_L$ = 50 pF | | | Ta = –40°C to +85°C $C_L$ = 50 pF | | |
|---|---|---|---|---|---|---|---|---|
| **Item** | **Symbol** | **$V_{CC}$ (V)*[1]** | **Min** | **Typ** | **Max** | **Min** | **Max** | **Unit** |
| Maximum clock frequency | $f_{max}$ | 5.0 | 100 | — | — | 80 | — | MHz |
| Propagation delay CP to $Q_n$ | $t_{PLH}$ | 5.0 | 1.0 | 9.0 | 11.5 | 1.0 | 12.5 | ns |
| Propagation delay CP to $Q_n$ | $t_{PHL}$ | 5.0 | 1.0 | 9.0 | 11.5 | 1.0 | 12.5 | |
| Propagation delay $\overline{MR}$ to $Q_n$ | $t_{PHL}$ | 5.0 | 1.0 | 9.5 | 13.0 | 1.0 | 14.5 | |

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

## AC Operating Requirements: HD74ACT164

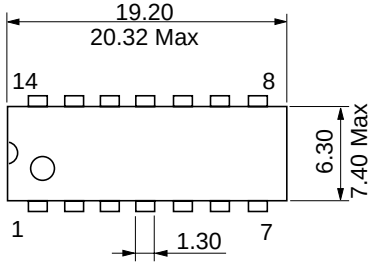
| | | | Ta = +25°C $C_L$ = 50 pF | Ta = –40°C to +85°C $C_L$ = 50 pF | |
|---|---|---|---|---|---|
| **Item** | **Symbol** | **$V_{CC}$ (V)*[1]** | **Typ** | **Guaranteed Minimum** | **Unit** |
| Setup time A or B to CP | $t_{su}$ | 5.0 | 2.5 | 7.0 | 8.0 | ns |
| Hold time CP to A or B | $t_h$ | 5.0 | 0.0 | 1.5 | 1.5 | |
| Pulse width CP or $\overline{MR}$ | $t_w$ | 5.0 | 4.5 | 7.0 | 8.0 | |
| Recovery time $\overline{MR}$ or CP | $t_{rec}$ | 5.0 | 0.0 | 2.0 | 2.0 | |

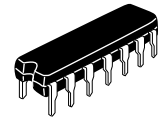
Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

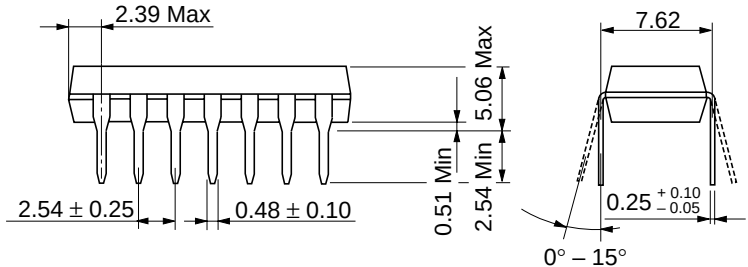
## Capacitance

| **Item** | **Symbol** | **Typ** | **Unit** | **Condition** |
|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | 4.5 | pF | $V_{CC}$ = 5.5 V |
| Power dissipation capacitance | $C_{PD}$ | 20.0 | pF | $V_{CC}$ = 5.0 V |

Unit: mm

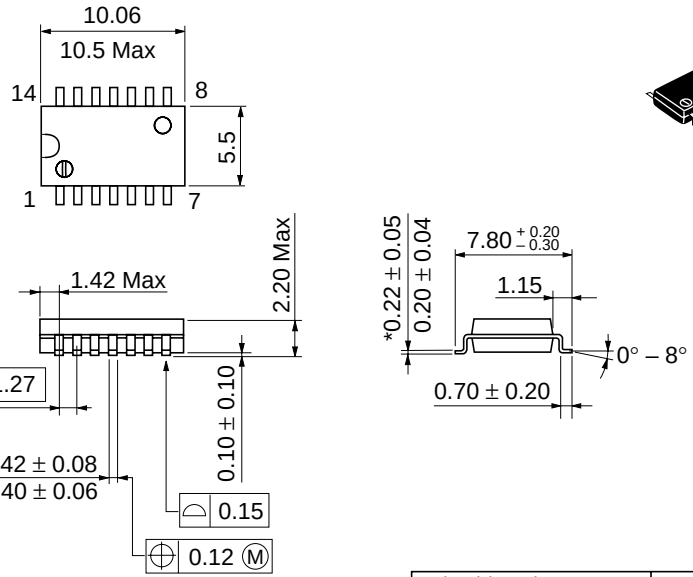


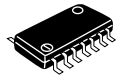






| | |
|---|---|
| Hitachi Code | DP-14 |
| JEDEC | Conforms |
| EIAJ | Conforms |
| Weight (reference value) | 0.97 g |

Unit: mm

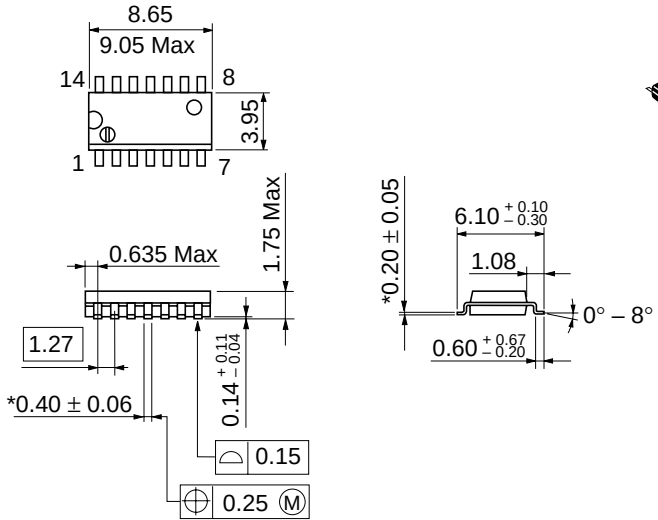


| | |
|---|---|
| Hitachi Code | FP-14DA |
| JEDEC | — |
| EIAJ | Conforms |
| Weight (reference value) | 0.23 g |

*Dimension including the plating thickness
Base material dimension

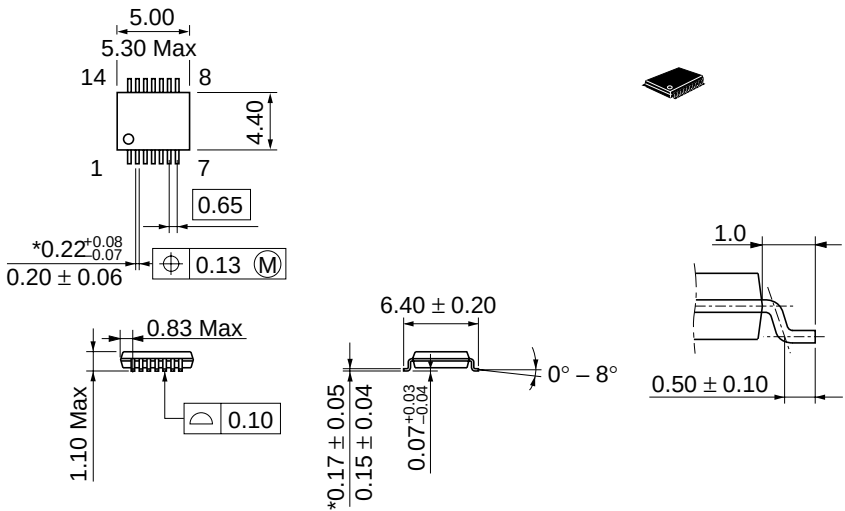
Unit: mm




| | |
|---|---|
| Hitachi Code | FP-14DN |
| JEDEC | Conforms |
| EIAJ | Conforms |
| Weight (reference value) | 0.13 g |

*Pd plating

Unit: mm




| | |
|---|---|
| Hitachi Code | TTP-14D |
| JEDEC | — |
| EIAJ | — |
| Weight (reference value) | 0.05 g |

*Dimension including the plating thickness
Base material dimension

## Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

# HITACHI

**Hitachi, Ltd.**
Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL
NorthAmerica : http:semiconductor.hitachi.com/
Europe : http://www.hitachi-eu.com/hel/ecg
Asia (Singapore) : http://www.has.hitachi.com.sg/grp3/sicd/index.htm
Asia (Taiwan) : http://www.hitachi.com.tw/E/Product/SICD_Frame.htm
Asia (HongKong) : http://www.hitachi.com.hk/eng/bo/grp3/index.htm
Japan : http://www.hitachi.co.jp/Sicd/indx.htm

**For further information write to:**

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX