# HD74AC165/HD74ACT165

Parallel-Load 8-bit Shift Register

HITACHI

## Description

This 8-bit serial shift register shifts data from $Q_A$ to $Q_H$ when clocked, Parallel inputs to each stage are enabled by a low level at the Shift/Load Input. Also included is a gated clock input and a complementary output from the eighth bit.

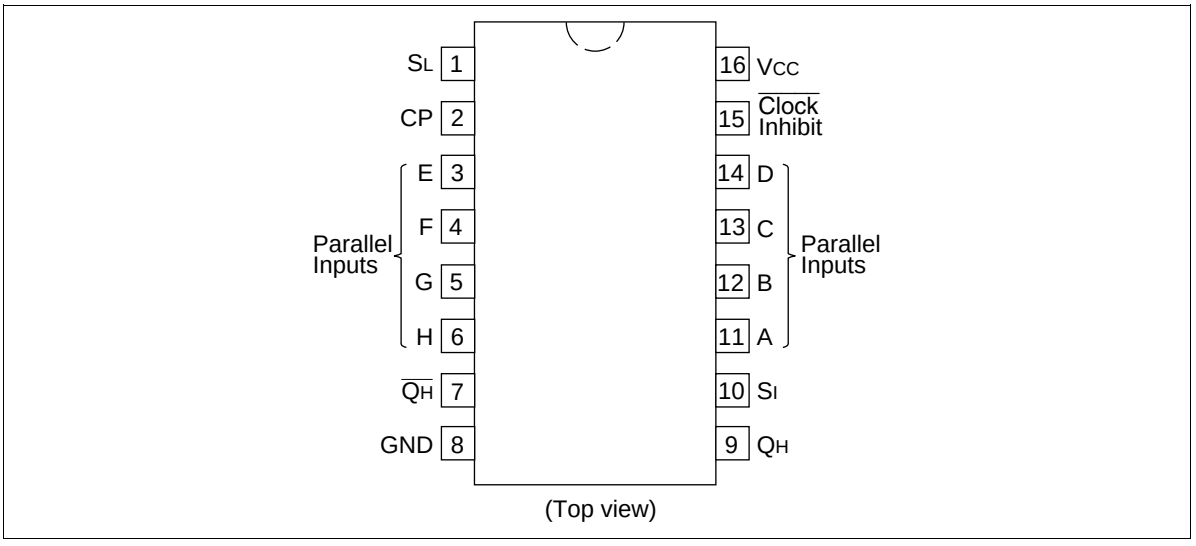
Clocking is accomplished through a 2-input NOR gate permitting one input to be used as a clock inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the Shift/Load input high enables the other clock input. Data transfer occurs on the positive going edge of the clock. Parallel loading is inhibited as long as the Shift/Load input is high. When taken low, data at the parallel inputs is loaded directly into the register independent of the state of the clock.

## Features

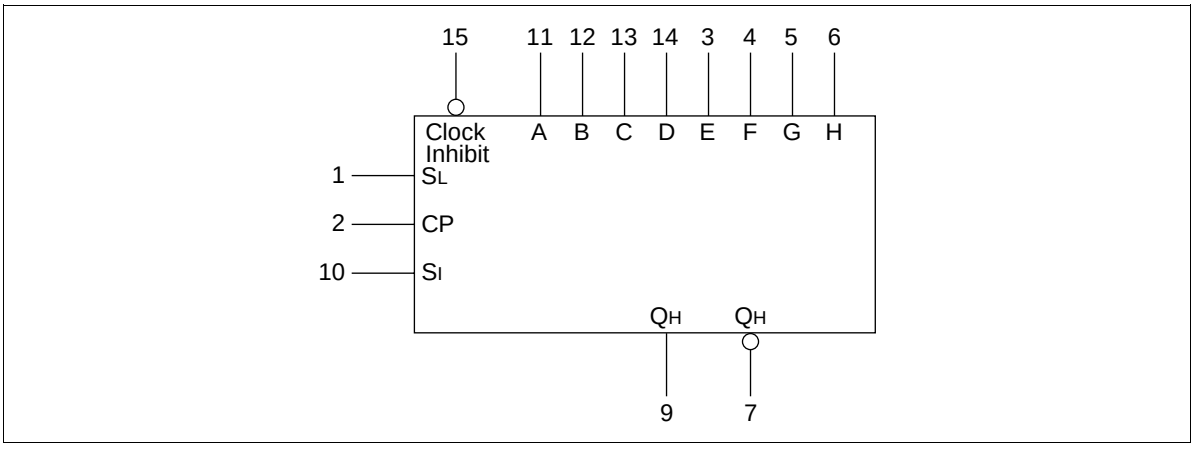
- Outputs Source/Sink 24 mA
- HD74ACT165 has TTL-Compatible Inputs

Hitachi semiconductor

## Pin Arrangement




## Logic Symbol




## Pin Names

| | |
|---|---|
| A to H | Parallel Inputs |
| $S_I$ | Serial Input |
| CP | Clock Input |
| $S_L$ | Shift Load |
| $\overline{\text{Clock}}$ Inhibit | Clock Inhibit |
| $Q_H$, $\overline{Q}_H$ | Outputs |

## Truth Table

**Inputs**

| | $\overline{\text{Clock}}$ | | | Parallel | Internal Outputs | | Outputs |
|---|---|---|---|---|---|---|---|
| $S_L$ | Inhibit | CP | $S_I$ | A ····· H | $Q_A$ | $Q_B$ | $Q_H$ |
| L | X | X | X | a ····· h | a | b | h |
| H | L | L | X | X | $Q_{A\overline{D}}$ | $Q_{B\overline{O}}$ | $Q_{HO}$ |
| H | L | ⎍ | H | X | H | $Q_{An}$ | $Q_{Gn}$ |
| H | L | ⎍ | L | X | L | $Q_{An}$ | $Q_{Cn}$ |
| H | H | X | X | X | $Q_{A\overline{D}}$ | $Q_{B\overline{O}}$ | $Q_{HO}$ |

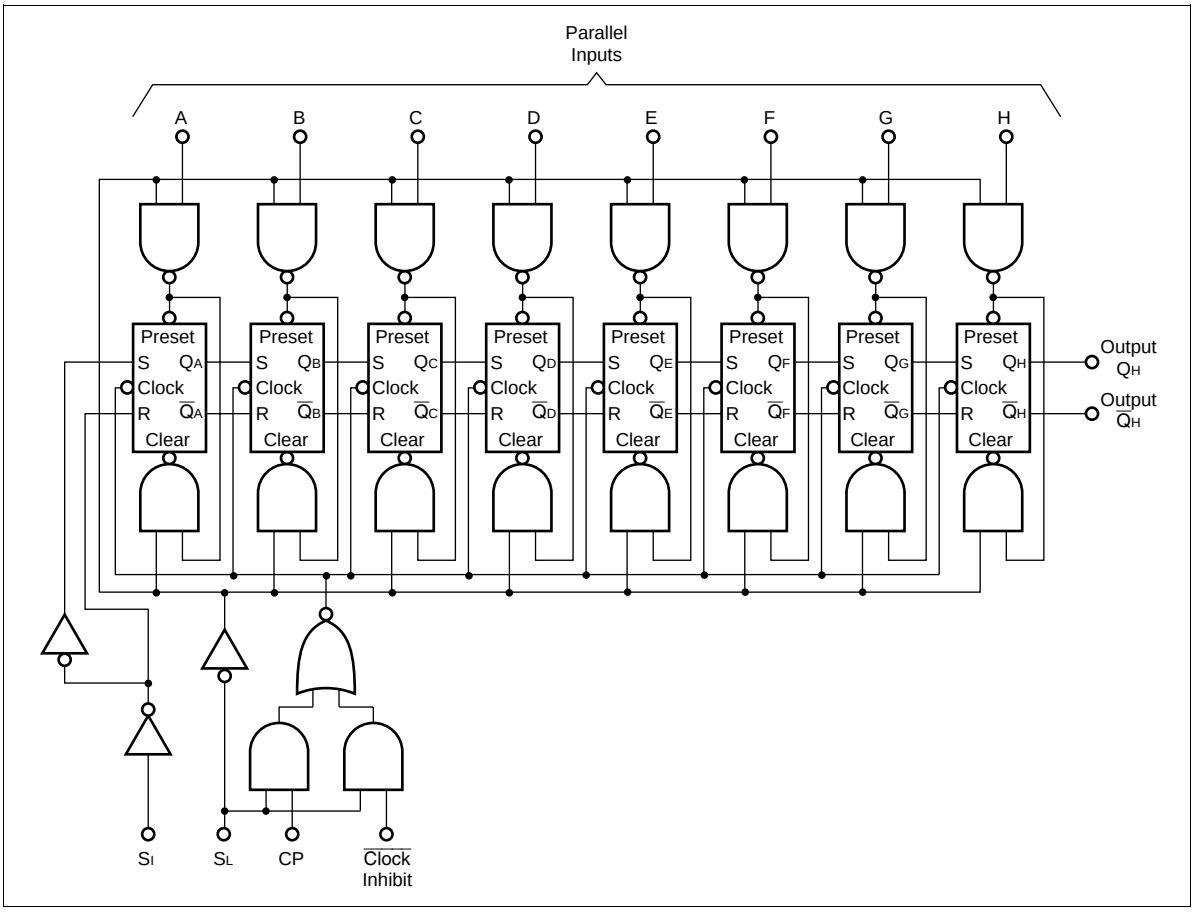
H : High Voltage Level

L : Low Voltage Level

X : Immaterial

⎍ : Low-to-High Clock Transition

## Logic Diagram




## DC Characteristics (unless otherwise specified)

| Item | Symbol | Max | Unit | Condition |
|---|---|---|---|---|
| Maximum quiescent supply current | $I_{CC}$ | 80 | µA | $V_{IN}$ = $V_{CC}$ or ground, $V_{CC}$ = 5.5 V, Ta = Worst case |
| Maximum quiescent supply current | $I_{CC}$ | 8.0 | µA | $V_{IN}$ = $V_{CC}$ or ground, $V_{CC}$ = 5.5 V, Ta = 25°C |
| Maximum additional $I_{CC}$/input (HD74ACT165) | $I_{CCT}$ | 1.5 | mA | $V_{IN}$ = $V_{CC}$ – 2.1 V, $V_{CC}$ = 5.5 V, Ta = Worst case |

## AC Characteristics: HD74AC165

| | | | Ta = +25°C<br>$C_L$ = 50 pF | | | Ta = –40°C to +85°C<br>$C_L$ = 50 pF | | |
|---|---|---|---|---|---|---|---|---|
| **Item** | **Symbol** | **$V_{cc}$ (V)*[1]** | **Min** | **Typ** | **Max** | **Min** | **Max** | **Unit** |
| Maximum count | $f_{max}$ | 3.3 | 85 | — | — | 70 | — | MHz |
| frequency | | 5.0 | 100 | — | — | 90 | — | |
| Propagation delay | $t_{PLH}$ | 3.3 | 1.0 | 11.0 | 17.5 | 1.0 | 20.5 | ns |
| CP to $Q_H$ or $\overline{Q}_H$ | | 5.0 | 1.0 | 8.0 | 11.5 | 1.0 | 13.5 | |
| Propagation delay | $t_{PHL}$ | 3.3 | 1.0 | 12.0 | 18.0 | 1.0 | 21.5 | ns |
| CP to $Q_H$ or $\overline{Q}_H$ | | 5.0 | 1.0 | 8.5 | 12.5 | 1.0 | 14.5 | |
| Propagation delay | $t_{PLH}$ | 3.3 | 1.0 | 13.5 | 19.5 | 1.0 | 22.5 | ns |
| H to $Q_H$ or $\overline{Q}_H$ | | 5.0 | 1.0 | 9.5 | 13.5 | 1.0 | 15.5 | |
| Propagation delay | $t_{PHL}$ | 3.3 | 1.0 | 9.0 | 14.0 | 1.0 | 16.5 | ns |
| H to $Q_H$ or $\overline{Q}_H$ | | 5.0 | 1.0 | 6.5 | 9.5 | 1.0 | 11.0 | |
| Propagation delay | $t_{PLH}$ | 3.3 | 1.0 | 11.5 | 20.5 | 1.0 | 23.5 | ns |
| $S_L$ to $Q_H$ or $\overline{Q}_H$ | | 5.0 | 1.0 | 8.5 | 14.0 | 1.0 | 16.0 | |
| Propagation delay | $t_{PHL}$ | 3.3 | 1.0 | 10.0 | 16.5 | 1.0 | 19.5 | ns |
| $S_L$ to $Q_H$ or $\overline{Q}_H$ | | 5.0 | 1.0 | 7.5 | 11.0 | 1.0 | 12.5 | |

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

## AC Operating Requirements: HD74AC165

| Item | Symbol | $V_{CC}$ (V)*[1] | Ta = +25°C, $C_L$ = 50 pF | Ta = –40°C to +85°C, $C_L$ = 50 pF | | Unit |
|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Minimum | | |
| Setup time, HIGH or LOW | $t_{su}$ | 3.3 | 3.5 | 5.0 | 6.0 | ns |
| H to $S_L$ | | 5.0 | 2.5 | 4.0 | 4.5 | |
| Hold time, HIGH or LOW | $t_h$ | 3.3 | –1.0 | 0.5 | 0.5 | ns |
| H to $S_L$ | | 5.0 | –0.5 | 0.5 | 0.5 | |
| Setup time, HIGH or LOW | $t_{su}$ | 3.3 | 1.0 | 3.5 | 4.0 | ns |
| $S_{in}$ to CP | | 5.0 | 0.5 | 3.0 | 3.5 | |
| Hold time, HIGH or LOW | $t_h$ | 3.3 | 1.5 | 2.0 | 2.0 | ns |
| $S_{in}$ to CP | | 5.0 | 1.0 | 2.0 | 2.0 | |
| Setup time, HIGH or LOW | $t_{su}$ | 3.3 | 3.0 | 5.0 | 6.0 | ns |
| $S_L$ to CP | | 5.0 | 2.0 | 4.0 | 4.5 | |
| Hold time, HIGH or LOW | $t_h$ | 3.3 | –2.0 | 0.0 | 0.0 | ns |
| $S_L$ to CP | | 5.0 | –1.0 | 0.0 | 0.0 | |
| Recovery time clock inhibit | $t_{rec}$ | 3.3 | 2.5 | 3.5 | 3.5 | ns |
| to CP | | 5.0 | 2.0 | 3.0 | 3.0 | |
| Clock pulse width | $t_w$ | 3.3 | 3.0 | 5.5 | 7.0 | ns |
| | | 5.0 | 3.0 | 4.5 | 5.0 | |

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

## AC Characteristics: HD74ACT165

| | | | Ta = +25°C<br>$C_L$ = 50 pF | | | Ta = –40°C to +85°C<br>$C_L$ = 50 pF | | |
|---|---|---|---|---|---|---|---|---|
| **Item** | **Symbol** | **$V_{cc}$ (V)*[1]** | **Min** | **Typ** | **Max** | **Min** | **Max** | **Unit** |
| Maximum count frequency | $f_{max}$ | 5.0 | 7.0 | — | — | 60 | — | MHz |
| Propagation delay CP to $Q_H$ or $\overline{Q}_H$ | $t_{PLH}$ | 5.0 | 1.0 | 8.5 | 13.5 | 1.0 | 15.5 | ns |
| Propagation delay CP to $Q_H$ or $\overline{Q}_H$ | $t_{PHL}$ | 5.0 | 1.0 | 9.5 | 14.0 | 1.0 | 16.5 | ns |
| Propagation delay H to $Q_H$ or $\overline{Q}_H$ | $t_{PLH}$ | 5.0 | 1.0 | 10.5 | 13.5 | 1.0 | 15.5 | ns |
| Propagation delay H to $Q_H$ or $\overline{Q}_H$ | $t_{PHL}$ | 5.0 | 1.0 | 7.5 | 11.0 | 1.0 | 12.5 | ns |
| Propagation delay $S_L$ to $Q_H$ or $\overline{Q}_H$ | $t_{PLH}$ | 5.0 | 1.0 | 9.5 | 15.0 | 1.0 | 18.0 | ns |
| Propagation delay $S_L$ to $Q_H$ or $\overline{Q}_H$ | $t_{PHL}$ | 5.0 | 1.0 | 8.5 | 13.0 | 1.0 | 15.5 | ns |

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

## AC Operating Requirements: HD74ACT165

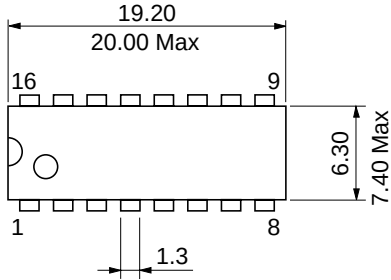
| Item | Symbol | $V_{CC}$ (V)*[1] | Ta = +25°C, $C_L$ = 50 pF | Ta = –40°C to +85°C, $C_L$ = 50 pF | | Unit |
|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Minimum | | |
| Setup time, HIGH or LOW H to $S_L$ | $t_{su}$ | 5.0 | 3.0 | 4.0 | 4.5 | ns |
| Hold time, HIGH or LOW H to $S_L$ | $t_h$ | 5.0 | –1.0 | 0.0 | 0.0 | ns |
| Setup time, HIGH or LOW $S_{in}$ to CP | $t_{su}$ | 5.0 | 0.5 | 3.0 | 3.5 | ns |
| Hold time, HIGH or LOW $S_{in}$ to CP | $t_h$ | 5.0 | 0.5 | 2.0 | 2.0 | ns |
| Setup time, HIGH or LOW $S_L$ to CP | $t_{su}$ | 5.0 | 2.0 | 4.0 | 4.5 | ns |
| Hold time, HIGH or LOW $S_L$ to CP | $t_h$ | 5.0 | –1.5 | 0.0 | 0.0 | ns |
| Recovery time clock inhibit to CP | $t_{rec}$ | 5.0 | 2.0 | 3.0 | 3.0 | ns |
| Clock pulse width | $t_w$ | 5.0 | 3.5 | 7.0 | 8.0 | ns |

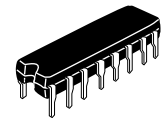
Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

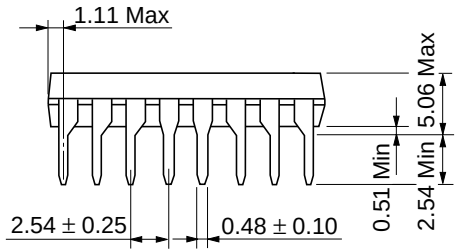
## Capacitance

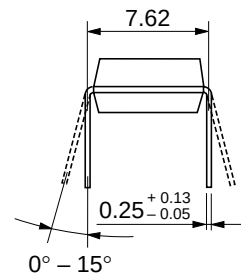
| Item | Symbol | Typ | Unit | Condition |
|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | 4.5 | pF | $V_{CC}$ = 5.5 V |
| Power dissipation capacitance | $C_{PD}$ | 5.0 | pF | $V_{CC}$ = 5.0 V |

Unit: mm



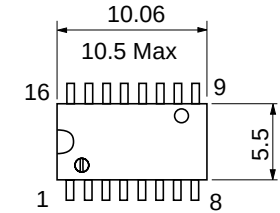



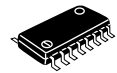


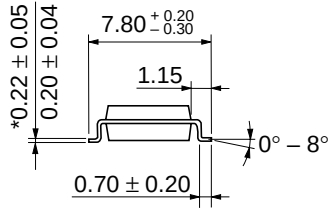



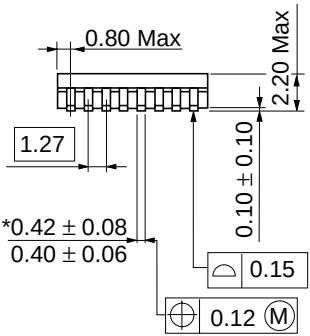

| | |
|---|---|
| Hitachi Code | DP-16 |
| JEDEC | Conforms |
| EIAJ | Conforms |
| Weight (reference value) | 1.07 g |

Unit: mm



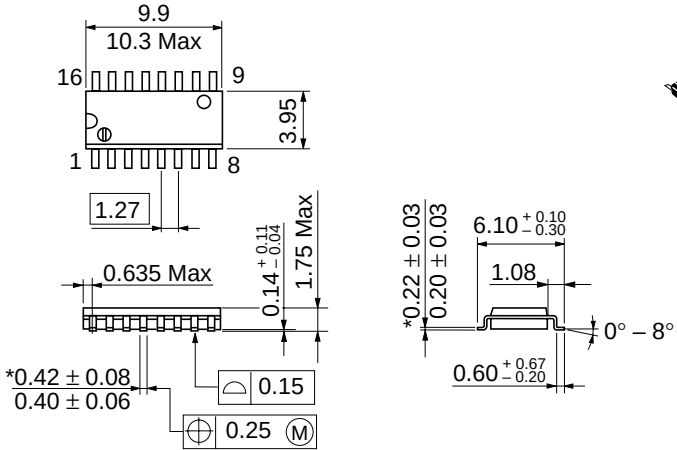


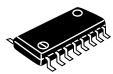




*Dimension including the plating thickness
Base material dimension

| | |
|---|---|
| Hitachi Code | FP-16DA |
| JEDEC | — |
| EIAJ | Conforms |
| Weight (reference value) | 0.24 g |

Unit: mm

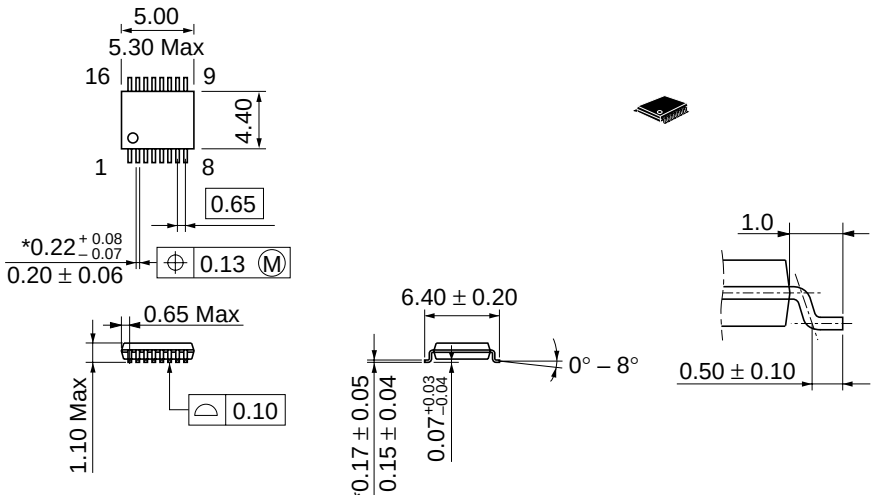


| | |
|---|---|
| Hitachi Code | FP-16DN |
| JEDEC | Conforms |
| EIAJ | Conforms |
| Weight (reference value) | 0.15 g |

*Dimension including the plating thickness
Base material dimension

Unit: mm




| | |
|---|---|
| Hitachi Code | TTP-16DA |
| JEDEC | — |
| EIAJ | — |
| Weight (reference value) | 0.05 g |

*Dimension including the plating thickness
Base material dimension

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