
HD74AC259

8-bit Addressable Latch

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Description

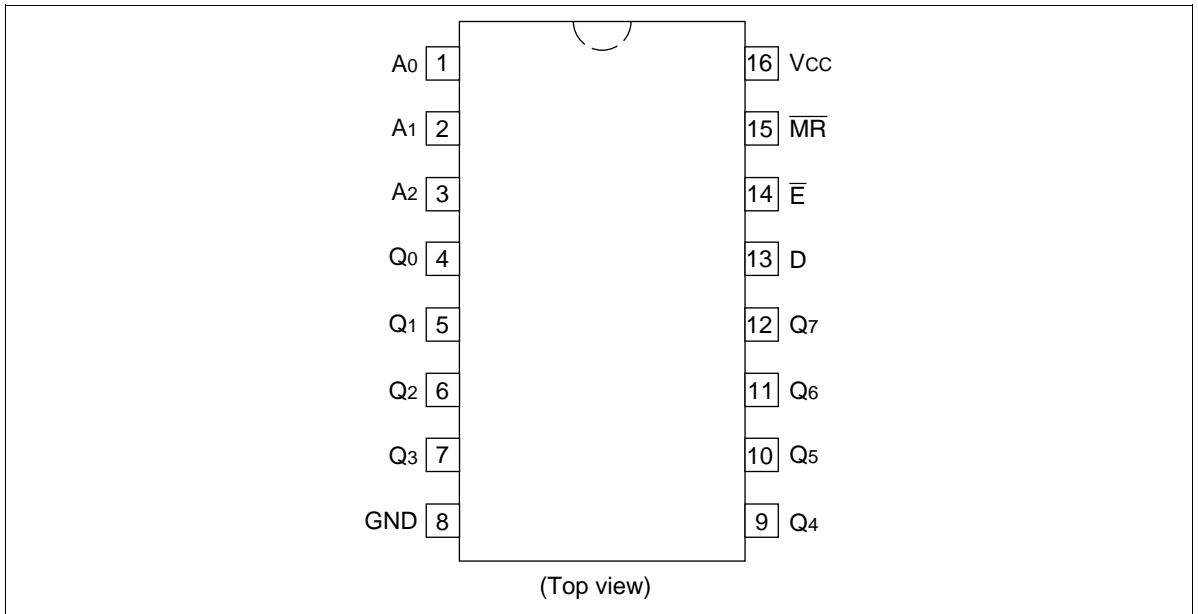
The HD74AC259 is a high-speed 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW Common Clear for resetting all latches, as well as an active LOW Enable.

Features

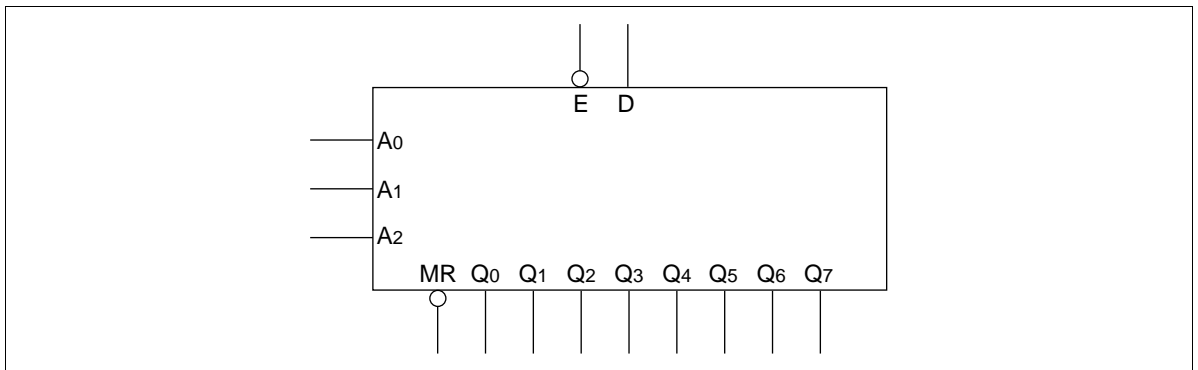
- Serial-to-Parallel Conversion
- Eight Bits of Storage with Output of Each Bit Available
- Random (Addressable) Data Entry
- Active High Demultiplexing or Decoding Capability
- Easily Expandable
- Common Clear
- Outputs Source/Sink 24 mA

HD74AC259

Pin Arrangement



Logic Symbol

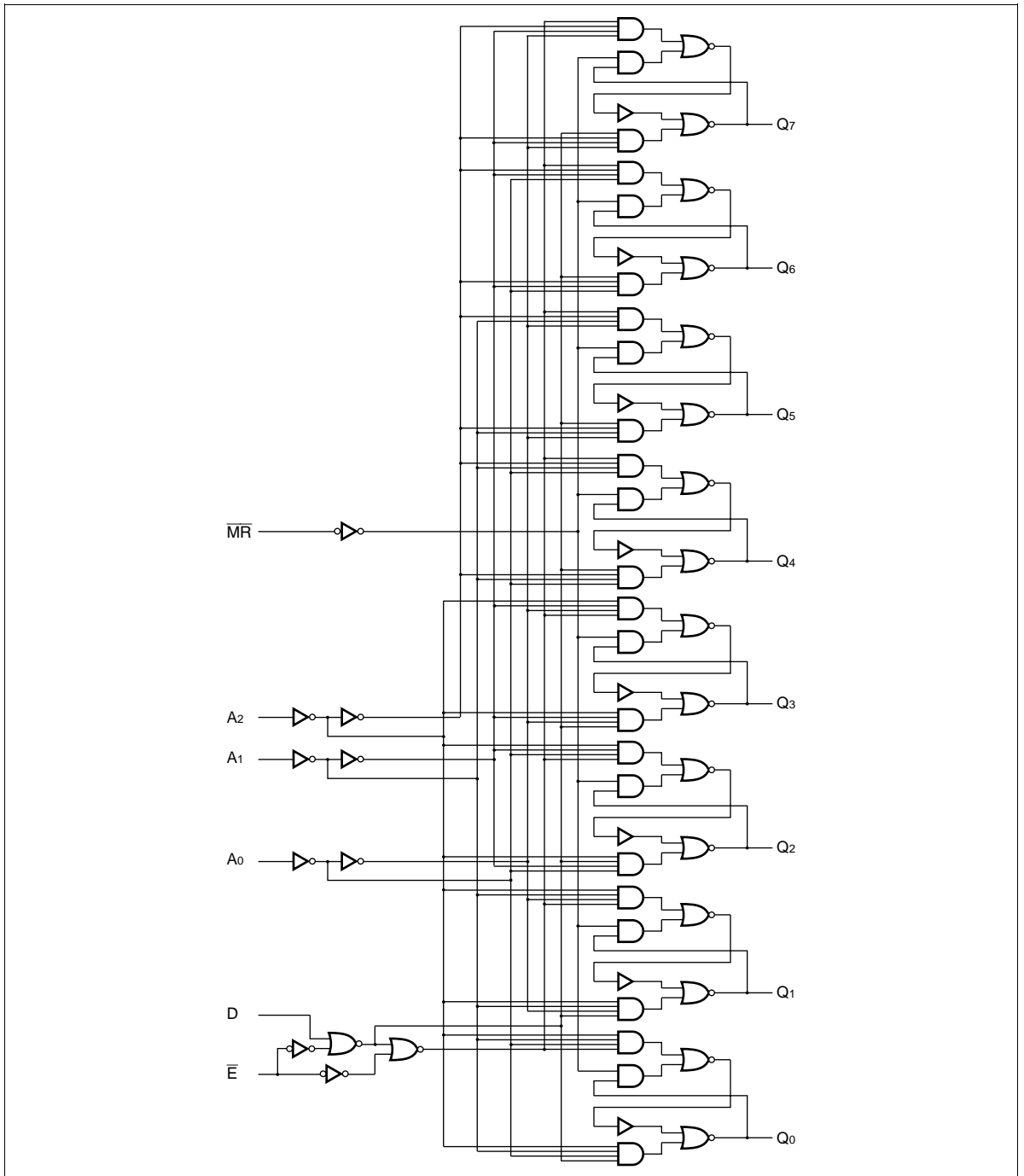


Pin Names

- A₀ – A₂ Address Inputs
- D Data Inputs
- \bar{E} Enable Input (Active LOW)
- \overline{MR} Master Reset (Active LOW)
- Q₀ – Q₇ Latch Outputs

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Logic Diagram



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Function Table

Operating Mode	Inputs						Outputs							
	\overline{MR}	\overline{E}	D	A ₀	A ₁	A ₂	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇
Master reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplex	L	L	d	L	L	L	Q = d	L	L	L	L	L	L	L
(Active HIGH	L	L	d	H	L	L	L	Q = d	L	L	L	L	L	L
Decoder when	L	L	d	L	H	L	L	L	Q = d	L	L	L	L	L
D = H)	L	L	d	H	H	L	L	L	L	Q = d	L	L	L	L
	L	L	d	L	L	H	L	L	L	L	Q = d	L	L	L
	L	L	d	H	L	H	L	L	L	L	L	Q = d	L	L
	L	L	d	L	H	H	L	L	L	L	L	L	Q = d	L
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q = d
Store (Do nothing)	H	H	X	X	X	X	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
Addressable latch	H	L	d	L	L	L	Q = d	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	H	L	L	q ₀	Q = d	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	L	H	L	q ₀	q ₁	Q = d	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	H	H	L	q ₀	q ₁	q ₂	Q = d	q ₄	q ₅	q ₆	q ₇
	H	L	d	L	L	H	q ₀	q ₁	q ₂	q ₃	Q = d	q ₅	q ₆	q ₇
	H	L	d	H	L	H	q ₀	q ₁	q ₂	q ₃	q ₄	Q = d	q ₆	q ₇
	H	L	d	L	H	H	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	Q = d	q ₇
	H	L	d	H	H	H	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	Q = d

H : High Voltage Level

L : Low Voltage Level

X : Immaterial

d : High or Low data one setup time prior to the Low-to-High Enable transition.

q : Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I _{CC}	80	μA	V _{IN} = V _{CC} or ground, V _{CC} = 5.5 V, Ta = Worst case
Maximum quiescent supply current	I _{CC}	8.0	μA	V _{IN} = V _{CC} or ground, V _{CC} = 5.5 V, Ta = 25°C

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AC Characteristics: HD74AC259

Item	Symbol	V _{cc} (V)*1	Ta = +25°C C _L = 50 pF			Ta = -40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f _{max}	3.3	65	—	—	60	—	MHz
		5.0	110	—	—	95	—	
Propagation delay MR̄ to Q _n	t _{PHL}	3.3	1.0	8.5	14.5	1.0	16.5	ns
		5.0	1.0	6.5	9.0	1.0	10.5	
Propagation delay D _n to Q _n	t _{PLH}	3.3	1.0	7.0	10.5	1.0	12.0	ns
		5.0	1.0	5.5	7.5	1.0	8.5	
Propagation delay D _n to Q _n	t _{PHL}	3.3	1.0	7.0	10.5	1.0	12.0	ns
		5.0	1.0	5.5	7.5	1.0	8.5	
Propagaion delay A _n to Q _n	t _{PLH}	3.3	1.0	11.5	18.5	1.0	21.5	ns
		5.0	1.0	8.0	11.5	1.0	14.0	
Propagation delay A _n to Q _n	t _{PHL}	3.3	1.0	11.5	18.5	1.0	21.0	ns
		5.0	1.0	8.0	11.5	1.0	13.5	
Propagation delay Ē to Q	t _{PLH}	3.3	1.0	9.0	15.0	1.0	17.0	ns
		5.0	1.0	6.5	9.0	1.0	10.5	
Propagation delay Ē to Q _n	t _{PHL}	3.3	1.0	9.0	14.0	1.0	16.0	ns
		5.0	1.0	6.5	8.5	1.0	10.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

HD74AC259

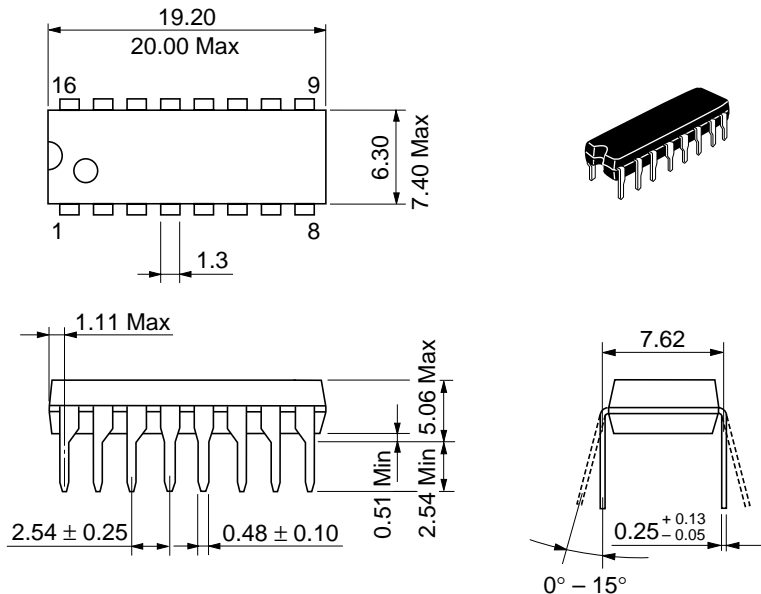
AC Operating Requirements: HD74AC259

Item	Symbol	V_{CC} (V)*1	Ta = +25°C CL = 50 pF		Ta = -40°C to +85°C CL = 50 pF		Unit
			Typ	Guaranteed Minimum	Guaranteed Minimum	Guaranteed Minimum	
Setup time, HIGH or LOW	t_{su}	3.3	1.0	3.5	3.5	ns	
D to \bar{E}		5.0	0.0	3.0	3.0		
Hold time, HIGH or LOW	t_h	3.3	0.5	2.0	2.0	ns	
D to \bar{E}		5.0	0.5	2.0	2.0		
Setup time, HIGH or LOW	t_{su}	3.3	1.0	6.0	7.0	ns	
A_n to \bar{E}		5.0	0.0	4.5	5.0		
Hold time, HIGH or LOW	t_h	3.3	-3.0	0.0	0.0	ns	
A_n to \bar{E}		5.0	-1.0	0.0	0.0		
Pulse width	t_w	3.3	3.0	5.5	7.0	ns	
		5.0	3.0	4.5	5.0		

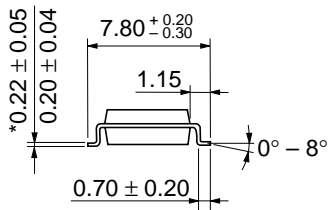
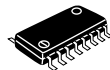
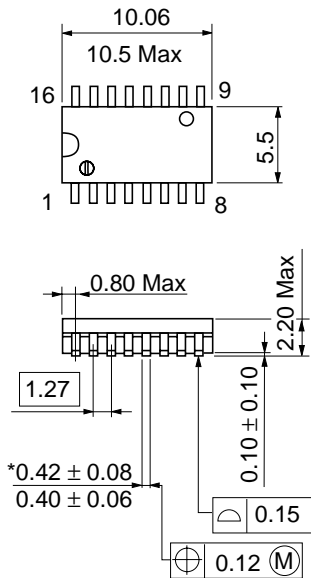
Note: 1. Voltage Range 3.3 is $3.3\text{ V} \pm 0.3\text{ V}$
Voltage Range 5.0 is $5.0\text{ V} \pm 0.5\text{ V}$

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	$V_{CC} = 5.5\text{ V}$
Power dissipation capacitance	C_{PD}	3.5	pF	$V_{CC} = 5.0\text{ V}$

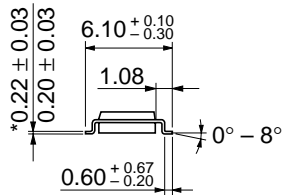
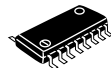
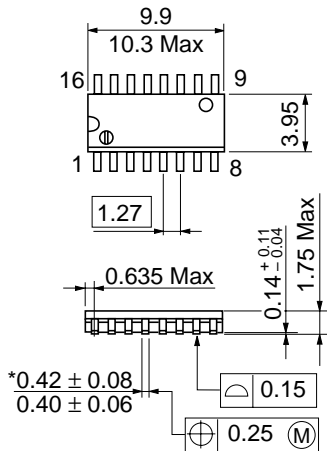


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



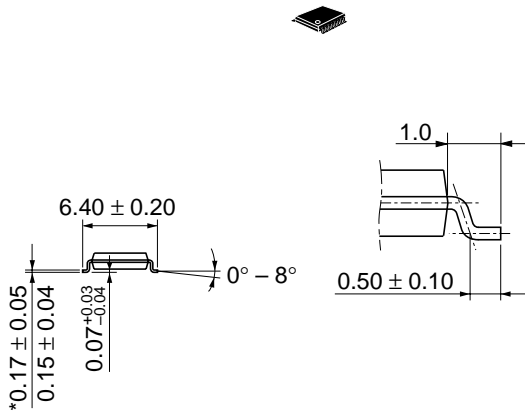
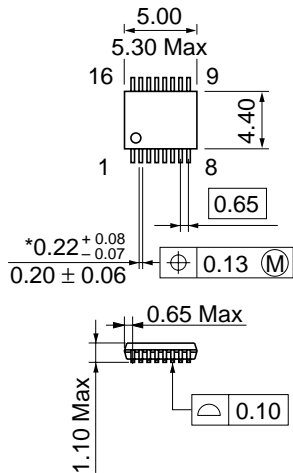
*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g



*Dimension including the plating thickness
 Base material dimension

Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

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