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# HD74AC670

4 × 4 Register File with 3-State Output

# HITACHI

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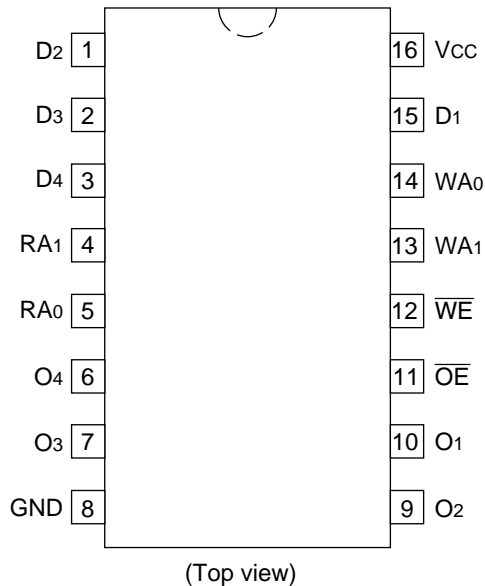
## Description

The HD74AC670 contains 16 high speed, low power, transparent D-type latches arranged as four words of four bits each, to function as a 4 × 4 register file. Separate read and write inputs, both address and enable, allow simultaneous read and write operation. The 3-state outputs make it possible to connect up to 128 outputs to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length.

## Features

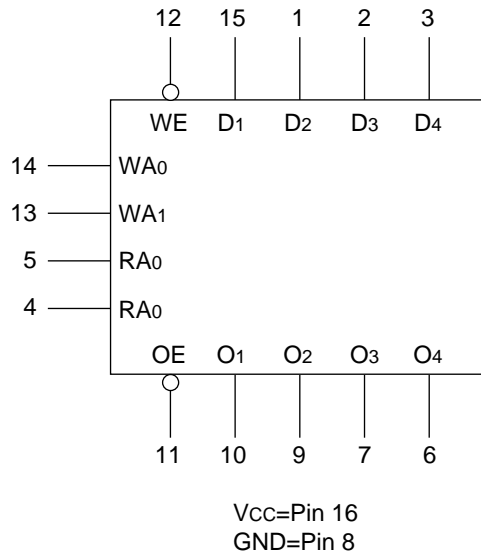
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Outputs Source/Sink 24 mA

## Pin Arrangement



# HD74AC670

## Logic Symbol



## Pin Names

D <sub>1</sub> to D <sub>4</sub>	Data Inputs
WA <sub>0</sub> , WA <sub>1</sub>	Write Address Inputs
$\overline{WE}$	Write Enable Input (Active Low)
RA <sub>0</sub> , RA <sub>1</sub>	Read Address Inputs
$\overline{OE}$	3-State Output Enable Input (Active Low)
O <sub>1</sub> to O <sub>4</sub>	Data Outputs

## Write Function Table

### Write Inputs

$\overline{WE}$	WA <sub>1</sub>	WA <sub>0</sub>	D Inputs to
L	L	L	Word 0
L	L	H	Word 1
L	H	L	Word 2
L	H	H	Word 3
H	X	X	None (hold)

H : High Voltage Level

L : Low Voltage Level

X : Immaterial

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**Read Function Table****Read Inputs**

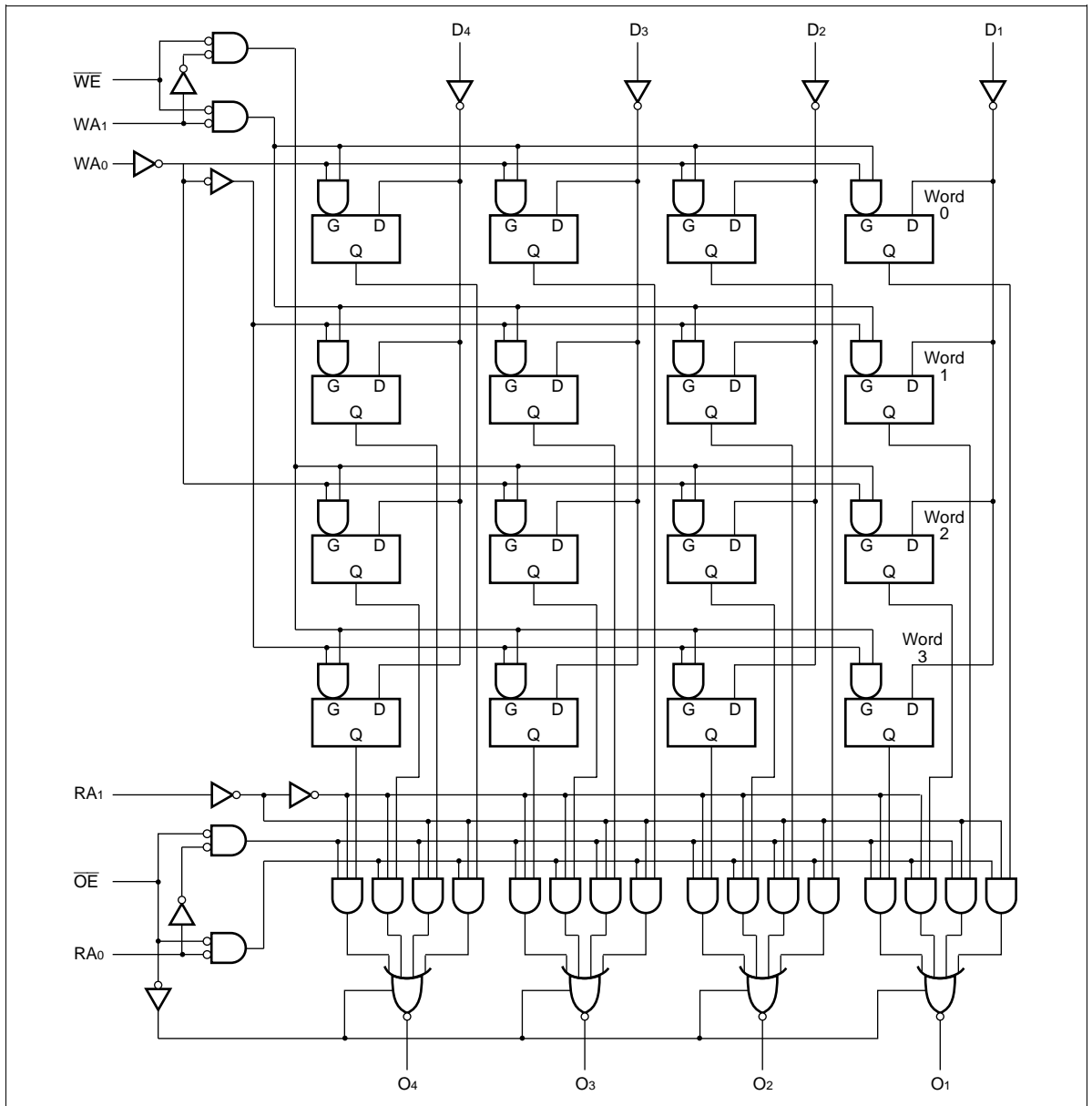
$\overline{OE}$	$RA_1$	$RA_0$	Outputs from
L	L	L	Word 0
L	L	H	Word 1
L	H	L	Word 2
L	H	H	Word 3
H	X	X	None (HIGH Z)

H : High Voltage Level

L : Low Voltage Level

X : Immaterial

## Logic Diagram



## DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	$I_{CC}$	80	$\mu A$	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$ , $T_a = \text{Worst case}$
Maximum quiescent supply current	$I_{CC}$	8.0	$\mu A$	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$ , $T_a = 25^\circ C$

AC Characteristics: HD74AC670

Item	Symbol	V <sub>CC</sub> (V) <sup>*1</sup>	Ta = +25°C C <sub>L</sub> = 50 pF			Ta = -40°C to +85°C C <sub>L</sub> = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Propagation delay	t <sub>PLH</sub>	3.3	1.0	14.0	17.5	1.0	19.0	ns
$\overline{W}_E$ to O <sub>n</sub>		5.0	1.0	11.5	13.5	1.0	15.0	
Propagation delay	t <sub>PHL</sub>	3.3	1.0	13.5	17.0	1.0	18.5	ns
$\overline{W}_E$ to O <sub>n</sub>		5.0	1.0	11.0	13.0	1.0	14.5	
Propagation delay	t <sub>PLH</sub>	3.3	1.0	12.5	15.5	1.0	17.0	ns
R <sub>A1</sub> or R <sub>A0</sub> to O <sub>n</sub>		5.0	1.0	10.0	12.0	1.0	13.0	
Propagation delay	t <sub>PHL</sub>	3.3	1.0	12.5	15.5	1.0	17.0	ns
R <sub>A1</sub> or R <sub>A0</sub> to O <sub>n</sub>		5.0	1.0	10.0	12.0	1.0	13.0	
Propagation delay	t <sub>PLH</sub>	3.3	1.0	12.0	15.0	1.0	16.5	ns
Data to O <sub>n</sub>		5.0	1.0	9.5	11.5	1.0	12.5	
Propagation delay	t <sub>PHL</sub>	3.3	1.0	11.5	14.5	1.0	16.0	ns
Data to O <sub>n</sub>		5.0	1.0	9.0	11.0	1.0	12.0	
Enable time	t <sub>PZH</sub>	3.3	1.0	8.0	11.0	1.0	12.0	ns
$\overline{OE}$ to O <sub>n</sub>		5.0	1.0	6.0	8.5	1.0	9.5	
Enable time	t <sub>PZL</sub>	3.3	1.0	10.0	12.0	1.0	13.0	ns
$\overline{OE}$ to O <sub>n</sub>		5.0	1.0	7.5	9.5	1.0	10.5	
Disable time	t <sub>PHZ</sub>	3.3	1.0	8.0	11.0	1.0	12.0	ns
$\overline{OE}$ to O <sub>n</sub>		5.0	1.0	6.0	8.5	1.0	9.5	
Disable time	t <sub>PLZ</sub>	3.3	1.0	9.0	11.5	1.0	12.5	ns
$\overline{OE}$ to O <sub>n</sub>		5.0	1.0	7.0	9.0	1.0	10.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V  
Voltage Range 5.0 is 5.0 V ± 0.5 V

# HD74AC670

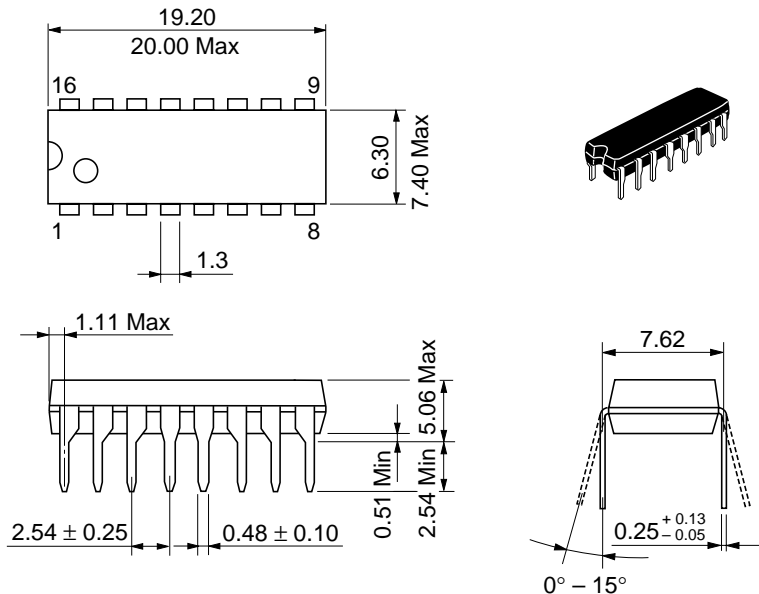
## AC Operating Requirements: HD74AC670

Item	Symbol	$V_{CC}$ (V)*1	$T_a = +25^\circ\text{C}$ $C_L = 50\text{ pF}$		$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $C_L = 50\text{ pF}$	
			Typ	Guaranteed Minimum	Guaranteed Minimum	Unit
Setup time	$t_{su}$	3.3	3.0	5.5	6.0	ns
Data to $\overline{W}_E$		5.0	2.0	4.0	4.5	
Setup time	$W_{A1}$ or $W_{A0}$ to $\overline{W}_E$	3.3	3.0	5.5	6.0	ns
$W_{A1}$ or $W_{A0}$ to $\overline{W}_E$		5.0	2.0	4.5	4.5	
Hold time	$t_h$	3.3	3.0	4.0	4.0	ns
$\overline{W}_E$ to Data		5.0	2.5	4.0	4.0	
Hold time	$\overline{W}_E$ to $W_{A1}$ or $W_{A2}$	3.3	3.0	4.0	4.0	ns
$\overline{W}_E$ to $W_{A1}$ or $W_{A2}$		5.0	2.5	4.0	4.0	
Pulse width	$t_w$	3.3	3.5	5.5	7.0	ns
$\overline{W}_E$		5.0	2.5	4.5	5.0	
Latch width	$t_{latch}$	3.3	0.5	10.0	10.0	ns
$\overline{W}_E$ to 1		5.0	0.5	10.0	10.0	

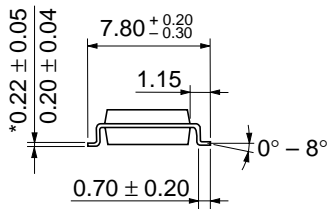
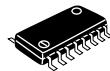
Note: 1. Voltage Range 3.3 is  $3.3\text{ V} \pm 0.3\text{ V}$   
Voltage Range 5.0 is  $5.0\text{ V} \pm 0.5\text{ V}$

## Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	$C_{IN}$	4.5	pF	$V_{CC} = 5.5\text{ V}$
Power dissipation capacitance	$C_{PD}$	60	pF	$V_{CC} = 5.0\text{ V}$



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g





\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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