

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF40195B**

### **MSI**

## **4-bit universal shift register**

Product specification  
File under Integrated Circuits, IC04

January 1995

# 4-bit universal shift register

## HEF40195B MSI

### DESCRIPTION

The HEF40195B is a fully synchronous edge-triggered 4-bit shift register with a clock input (CP), four synchronous parallel data inputs (P<sub>0</sub> to P<sub>3</sub>), two synchronous serial data inputs (J,  $\bar{K}$ ), a synchronous parallel enable input ( $\overline{PE}$ ), buffered parallel outputs from all 4-bit positions (O<sub>0</sub> to O<sub>3</sub>), a buffered inverted output from the last bit position ( $\overline{O_3}$ ) and an overriding asynchronous master reset input ( $\overline{MR}$ ). Each register stage is of a D-type master-slave flip-flop. Operation is synchronous (except for  $\overline{MR}$ ) and is edge-triggered on the LOW to HIGH transition of the CP

input. When  $\overline{PE}$  is LOW, data are loaded into the register from P<sub>0</sub> to P<sub>3</sub> on the LOW to HIGH transition of CP. When  $\overline{PE}$  is HIGH, data are shifted into the first register position from J and  $\bar{K}$  and all the data in the register are shifted one position to the right on the LOW to HIGH transition of CP. D-type entry is obtained by interconnecting J and  $\bar{K}$ . When J is HIGH and  $\bar{K}$  is LOW, the first stage is in the toggle mode. When J is LOW and  $\bar{K}$  is HIGH, the first stage is in the hold mode. A LOW on  $\overline{MR}$  resets all four bit positions (O<sub>0</sub> to O<sub>3</sub> = LOW,  $\overline{O_3}$  = HIGH) independent of all other input conditions.

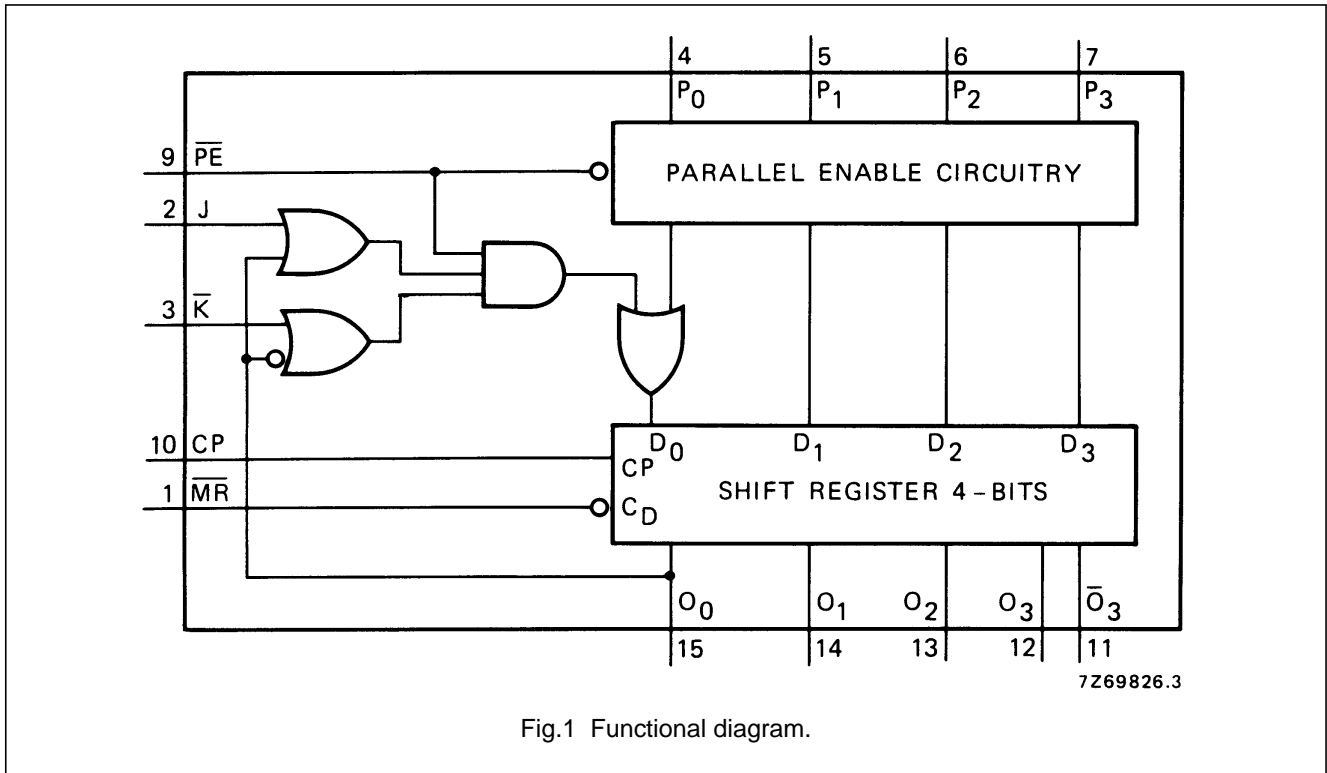


Fig.1 Functional diagram.

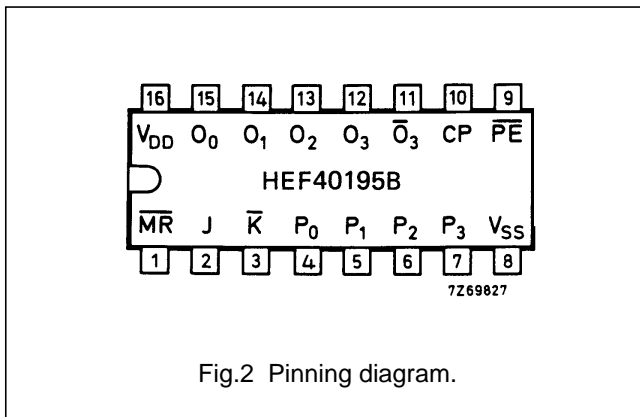


Fig.2 Pinning diagram.

- HEF40195BP(N): 16-lead DIL; plastic (SOT38-1)
  - HEF40195BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
  - HEF40195BT(D): 16-lead SO; plastic (SOT109-1)
- ( ): Package Designator North America

### FAMILY DATA, I<sub>DD</sub> LIMITS category MSI

See Family Specifications

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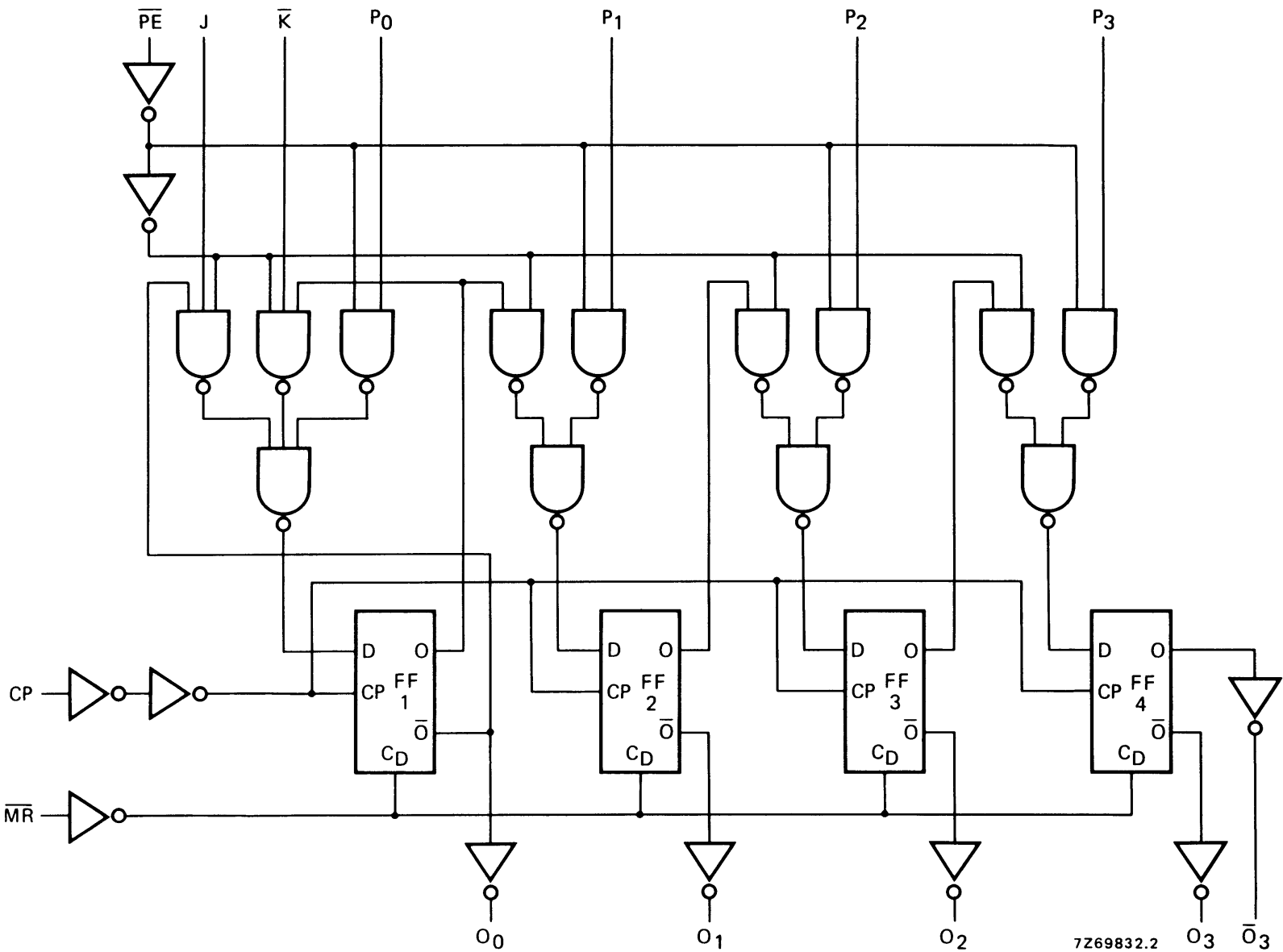


Fig.3 Logic diagram.

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## PINNING

$\overline{PE}$	parallel enable input (active LOW)
$P_0$ to $P_3$	parallel data inputs
J	first stage J-input (active HIGH)
$\overline{K}$	first stage K-input (active LOW)
CP	clock input (LOW to HIGH edge triggered)
$\overline{MR}$	master reset input (active LOW)
$O_0$ to $O_3$	buffered parallel outputs
$\overline{O}_3$	buffered inverted output from last stage

## FUNCTION TABLE

OPERATING MODE	INPUTS ( $\overline{MR} = \text{HIGH}$ )							OUTPUTS AT $t_{n+1}$				
	$\overline{PE}$	J	$\overline{K}$	$P_0$	$P_1$	$P_2$	$P_3$	$O_0$	$O_1$	$O_2$	$O_3$	$\overline{O}_3$
shift mode	H	L	L	X	X	X	X	L	$O_0$	$O_1$	$O_2$	$\overline{O}_2$
	H	L	H	X	X	X	X	$O_0$	$O_0$	$O_1$	$O_2$	$\overline{O}_2$
	H	H	L	X	X	X	X	$\overline{O}_0$	$O_0$	$O_1$	$O_2$	$\overline{O}_2$
	H	H	H	X	X	X	X	H	$O_0$	$O_1$	$O_2$	$\overline{O}_2$
parallel entry mode	L	X	X	L	L	L	L	L	L	L	L	H
	L	X	X	H	H	H	H	H	H	H	H	L

## Notes

1. H = HIGH state (the more positive voltage)
2. L = LOW state (the less positive voltage)
3. X = state is immaterial
4.  $t_{n+1}$  = state after next LOW to HIGH transition of CP

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MSI**AC CHARACTERISTICS** $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$ 

	$V_{DD}$ V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA		
Propagation delays $CP \rightarrow O_n$ HIGH to LOW	5	$t_{PHL}$		105	215	ns	$78\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10			50	95	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15			35	65	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	LOW to HIGH	5	$t_{PLH}$		90	180	ns	$63\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10			45	85	ns	$34\text{ ns} + (0,23\text{ ns/pF}) C_L$
		15			30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
$CP \rightarrow \overline{O}_3$ HIGH to LOW	5	$t_{PHL}$		125	255	ns	$98\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10			50	100	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15			35	70	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	LOW to HIGH	5	$t_{PLH}$		120	240	ns	$93\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10			50	105	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$
		15			35	75	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$
$\overline{MR} \rightarrow O_n$ HIGH to LOW	5	$t_{PHL}$		100	205	ns	$73\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10			45	90	ns	$34\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15			30	65	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	LOW to HIGH	5	$t_{PLH}$		125	235	ns	$98\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10			55	115	ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$
		15			40	85	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times	5	$t_{THL}$		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$	
	10			30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15			20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
	LOW to HIGH	5	$t_{TLH}$		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
		10			30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
		15			20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$

## 4-bit universal shift register

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MSI**AC CHARACTERISTICS** $V_{SS} = 0$  V;  $T_{amb} = 25$  °C;  $C_L = 50$  pF; input transition times  $\leq 20$  ns

	$V_{DD}$ V	SYMBOL	MIN.	TYP.	MAX.	
Set-up times $J, \bar{K} \rightarrow CP$  $P_n \rightarrow CP$  $\bar{PE} \rightarrow CP$	5	$t_{su}$	70	35	ns	see also waveforms Figs 4 and 5
	10		20	10	ns	
	15		10	5	ns	
	5	$t_{su}$	85	40	ns	
	10		25	10	ns	
	15		10	5	ns	
	5	$t_{su}$	115	55	ns	
	10		45	20	ns	
	15		30	15	ns	
Hold times $J, \bar{K} \rightarrow CP$  $P_n \rightarrow CP$  $\bar{PE} \rightarrow CP$	5	$t_{hold}$	15	-20	ns	
	10		5	-5	ns	
	15		0	-5	ns	
	5	$t_{hold}$	20	-25	ns	
	10		10	-5	ns	
	15		0	-5	ns	
	5	$t_{hold}$	10	-50	ns	
	10		5	-20	ns	
	15		5	-10	ns	
Minimum clock pulse width; LOW	5	$t_{WCPL}$	60	30	ns	
	10		25	10	ns	
	15		20	10	ns	
Minimum $\bar{MR}$ pulse width; HIGH	5	$t_{WMRL}$	100	50	ns	
	10		40	20	ns	
	15		30	15	ns	
Recovery time for $\bar{MR}$	5	$t_{RMR}$	30	10	ns	
	10		15	5	ns	
	15		15	5	ns	
Maximum clock pulse frequency	5	$f_{max}$	5	10	MHz	
	10		14	28	MHz	
	15		19	39	MHz	

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	V <sub>DD</sub> V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$1900 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f <sub>i</sub> = input freq. (MHz) f <sub>o</sub> = output freq. (MHz) C <sub>L</sub> = load capacitance (pF) ∑ (f <sub>o</sub> C <sub>L</sub> ) = sum of outputs V <sub>DD</sub> = supply voltage (V)
	10	$8300 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$22\ 800 f_i + \sum (f_o C_L) \times V_{DD}^2$	

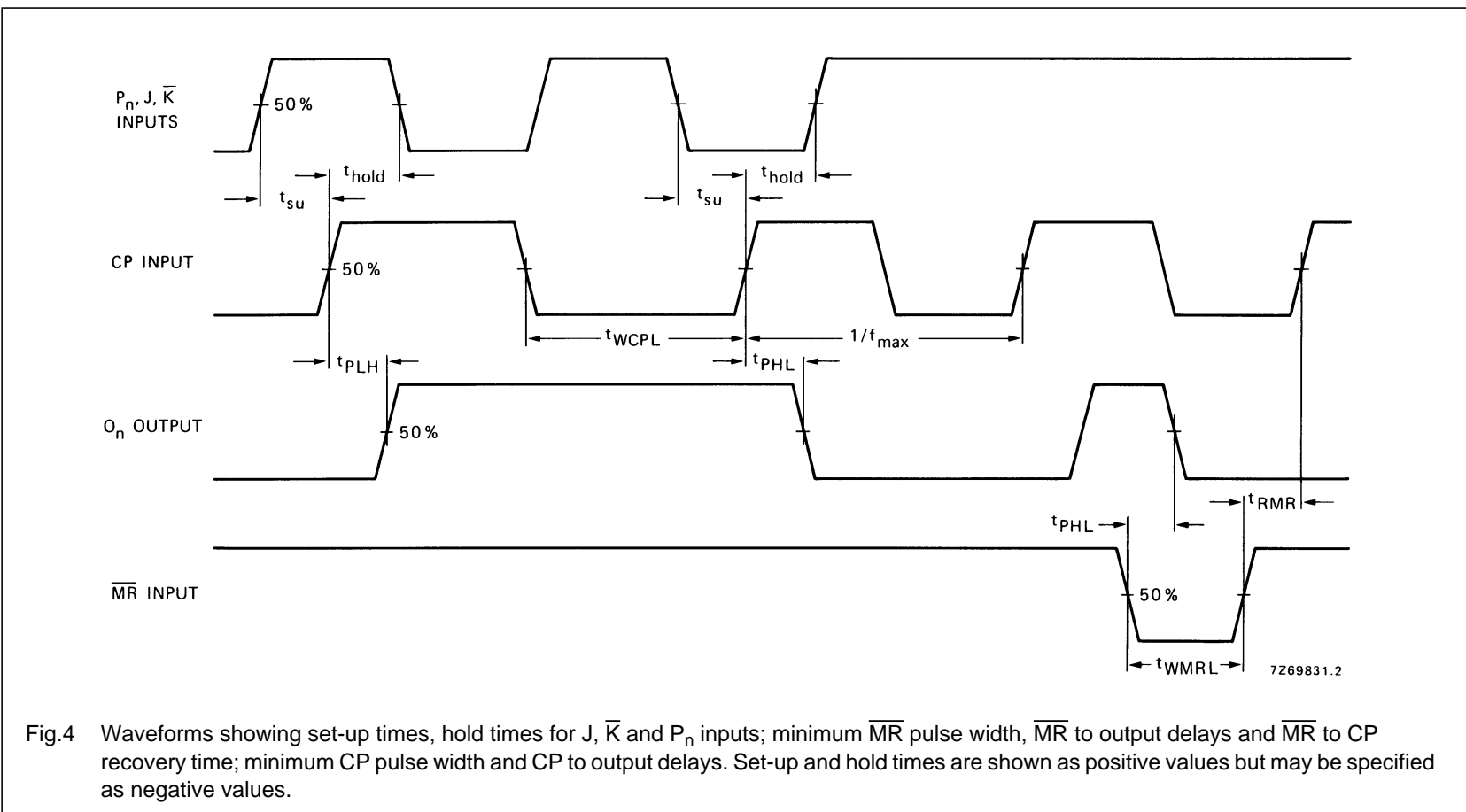


Fig.4 Waveforms showing set-up times, hold times for J, K̄ and P<sub>n</sub> inputs; minimum MR pulse width, MR to output delays and MR to CP recovery time; minimum CP pulse width and CP to output delays. Set-up and hold times are shown as positive values but may be specified as negative values.

## 4-bit universal shift register

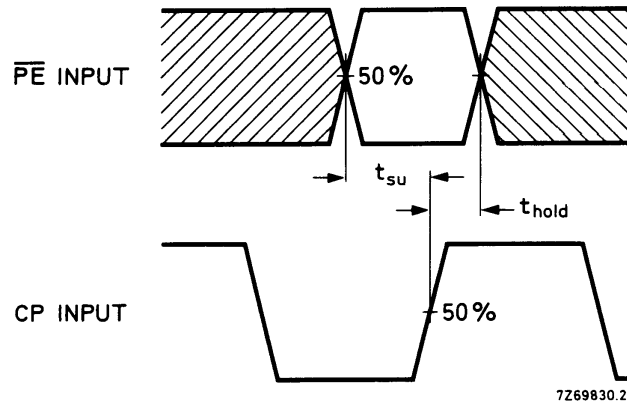
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Fig.5 Waveforms showing set-up and hold times for  $\overline{PE}$  input. Set-up and hold times are shown as positive values but may be specified as negative values.

**APPLICATION INFORMATION**

Some examples of applications for the HEF40195B are:

- Serial data transfer
- Parallel data transfer
- Serial to parallel data transfer
- Parallel to serial data transfer