HGTP3N60B3D, HGT1S3N60B3DS

Data Sheet **January 2000** **File Number 4414.1**

7A, 600V, UFS Series N-Channel IGBT with Anti-Parallel Hyperfast Diode

The HGTP3N60B3D and HGT1S3N60B3DS are MOS gated high voltage switching devices combining the best features of MOSFETs and bipolar transistors. These devices have the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between 25^{o}C and 150^{o}C. The diode used in anti-parallel with the IGBT is the RHRD460. The IGBT used is TA49192.

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

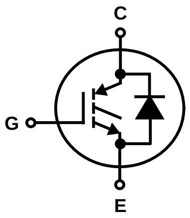
Formerly Developmental Type TA49193.

Ordering Information

PART NUMBER	PACKAGE	BRAND
HGTP3N60B3D	TO-220AB	G3N60B3D
HGT1S3N60B3DS	TO-263AB	G3N60B3D

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in tape and reel, i.e., HGT1S3N60B3DS9A.

Symbol

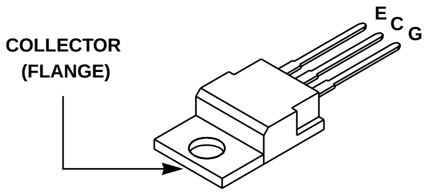


Features

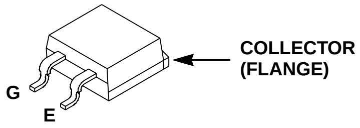
- 7A, 600V $T_C = 25^{o}C$
- 600V Switching SOA Capability
- Typical Fall Time. . . . . 115ns at $T_J = 125^{o}C$
- Short Circuit Rating
- Low Conduction Loss
- Hyperfast Anti-Parallel Diode
- Related Literature
- TB334 “Guidelines for Soldering Surface Mount
  - Components to PC Boards

Packaging

JEDEC TO-220AB



TO-263, TO-263AB



INTERSIL CORPORATION IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,587,713
4,598,461	4,605,948	4,620,211	4,631,564	4,639,754	4,639,762	4,641,162	4,644,637
4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690	4,794,432	4,801,986
4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606	4,860,080	4,883,767
4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951	4,969,027	

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		HGTP3N60B3D, HGT1S3N60B3DS	UNITS
Collector to Emitter Voltage	BV_{CES}	600	V
Collector Current Continuous			
At $T_C = 25^oC$	I_{C25}	7.0	A
At $T_C = 110^oC$	I_{C110}	3.5	A
Average Diode Forward Current	$I_{EC(AVG)}$	4.0	
Collector Current Pulsed (Note 1)	I_{CM}	20	A
Gate to Emitter Voltage Continuous	V_{GES}	±20	V
Gate to Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_J = 150^oC$ (Figure 2)	SSOA	18A at 600V	
Power Dissipation Total at $T_C = 25^oC$	P_D	33.3	W
Power Dissipation Derating $T_C > 25^oC$		0.27	W/^oC
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to 150	^oC
Maximum Lead Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Tech Brief 334	T_{PKG}	260	^oC
Short Circuit Withstand Time (Note 2) at $V_{GE} = 12V$	t_{SC}	5	µs
Short Circuit Withstand Time (Note 2) at $V_{GE} = 10V$	t_{SC}	10	µs

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 360V$, $T_J = 125^oC$, $R_G = 82\Omega$.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Collector to Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Collector to Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = 25^oC$	-	-	250	µA
			$T_C = 150^oC$	-	-	2.0	mA
Collector to Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$, $V_{GE} = 15V$	$T_C = 25^oC$	-	1.8	2.1	V
			$T_C = 150^oC$	-	2.1	2.5	V
Gate to Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$		4.5	5.4	6.0	V
Gate to Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±250	nA
Switching SOA	SSOA	$T_J = 150^oC$, $R_G = 82\Omega$, $V_{GE} = 15V$ $L = 500\mu H$, $V_{CE} = 600V$		18	-	-	A
Gate to Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$		-	7.9	-	V
On-State Gate Charge	$Q_{g(ON)}$	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = 15V$	-	18	22	nC
			$V_{GE} = 20V$	-	21	25	nC
Current Turn-On Delay Time	$t_{d(ON)I}$	IGBT and Diode at $T_J = 25^oC$ $I_{CE} = I_{C110}$ $V_{CE} = 0.8\ BV_{CES}$ $V_{GE} = 15V$ $R_G = 82\Omega$ $L = 1mH$ Test Circuit (Figure 19)		-	18	-	ns
Current Rise Time	t_{rI}			-	16	-	ns
Current Turn-Off Delay Time	$t_{d(OFF)I}$			-	105	-	ns
Current Fall Time	t_{fI}			-	70	-	ns
Turn-On Energy	E_{ON}			-	66	75	µJ
Turn-Off Energy (Note 1)	E_{OFF}			-	88	160	µJ

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Turn-On Delay Time	$t_{d(ON)I}$	IGBT and Diode at $T_J = 150^oC$ $I_{CE} = I_{C110}$ $V_{CE} = 0.8\ BV_{CES}$ $V_{GE} = 15V$ $R_G = 82\Omega$ L = 1mH Test Circuit (Figure 19)	-	16	-	ns
Current Rise Time	t_{rI}		-	18	-	ns
Current Turn-Off Delay Time	$t_{d(OFF)I}$		-	220	295	ns
Current Fall Time	t_{fI}		-	115	175	ns
Turn-On Energy	E_{ON}		-	130	140	µJ
Turn-Off Energy (Note 1)	E_{OFF}		-	210	325	µJ
Diode Forward Voltage	V_{EC}	$I_{EC} = 3A$	-	2.0	2.5	V
Diode Reverse Recovery Time	t_{rr}	$I_{EC} = 1A$, $dI_{EC}/dt = 200A/\mu s$	-	-	22	ns
		$I_{EC} = 3A$, $dI_{EC}/dt = 200A/\mu s$	-	-	28	ns
Thermal Resistance Junction To Case	$R_{\theta JC}$	IGBT	-	-	3.75	$^oC/W$
		Diode			3.0	$^oC/W$

NOTE:

3. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$). All devices were tested per JEDEC Standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss. Turn-On losses include losses due to diode recovery.

Typical Performance Curves Unless Otherwise Specified

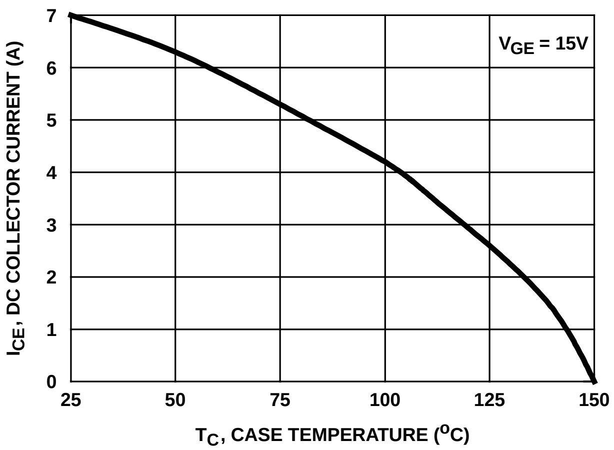


FIGURE 1. DC COLLECTOR CURRENT vs CASE TEMPERATURE

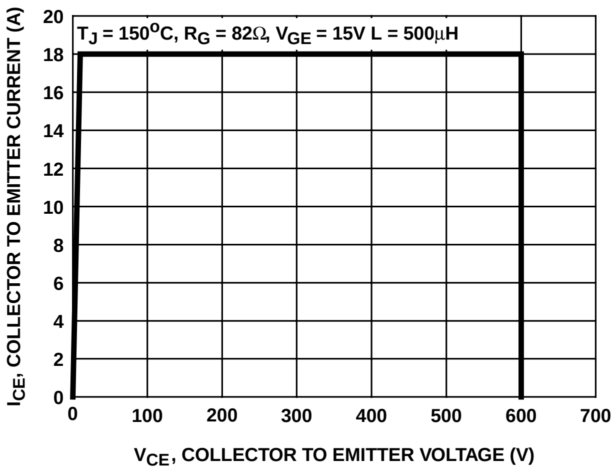


FIGURE 2. MINIMUM SWITCHING SAFE OPERATING AREA

Typical Performance Curves Unless Otherwise Specified **(Continued)**

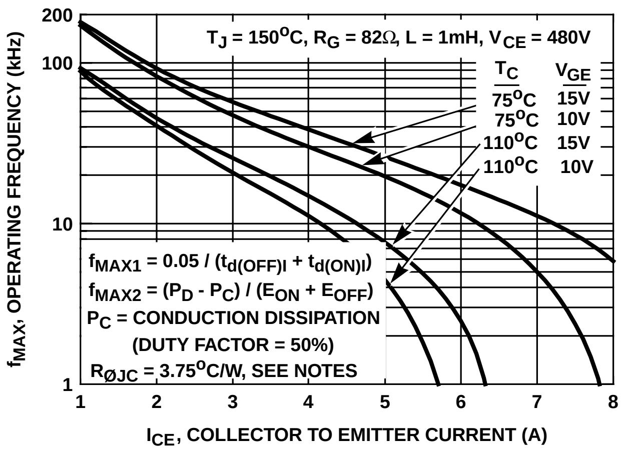


FIGURE 3. OPERATING FREQUENCY vs COLLECTOR TO EMITTER CURRENT

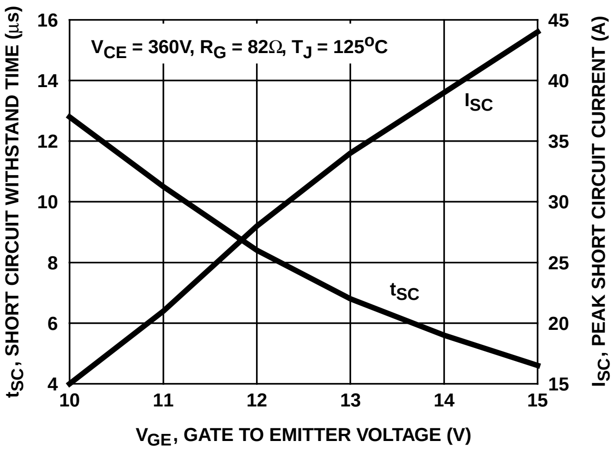


FIGURE 4. SHORT CIRCUIT WITHSTAND TIME

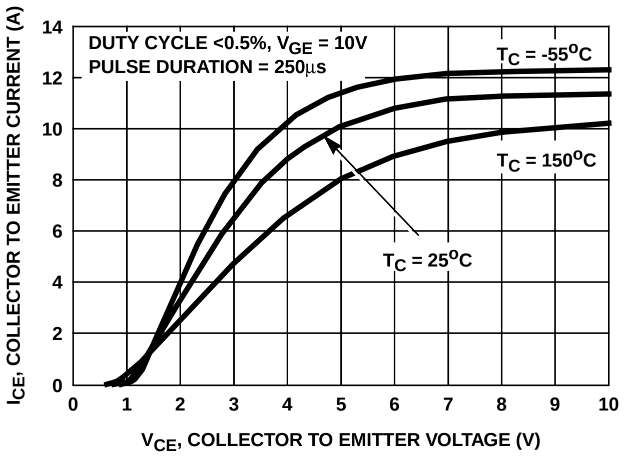


FIGURE 5. COLLECTOR TO EMITTER ON-STATE VOLTAGE

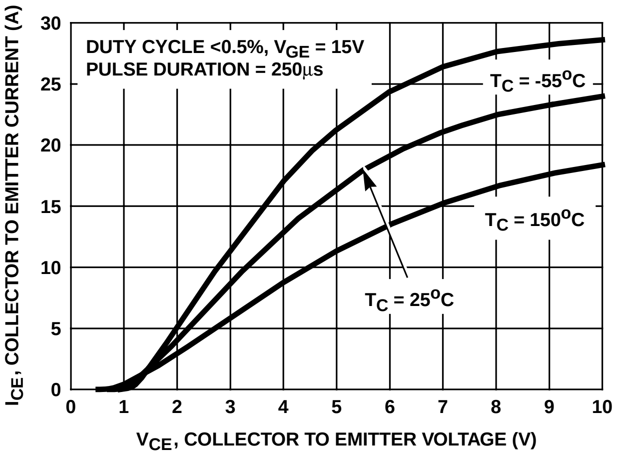


FIGURE 6. COLLECTOR TO EMITTER ON-STATE VOLTAGE

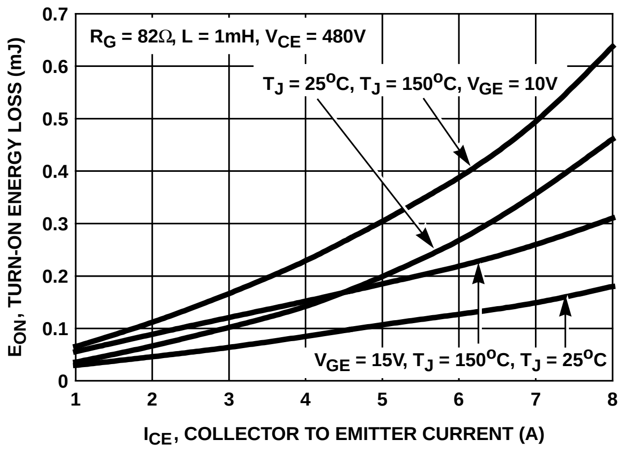


FIGURE 7. TURN-ON ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT

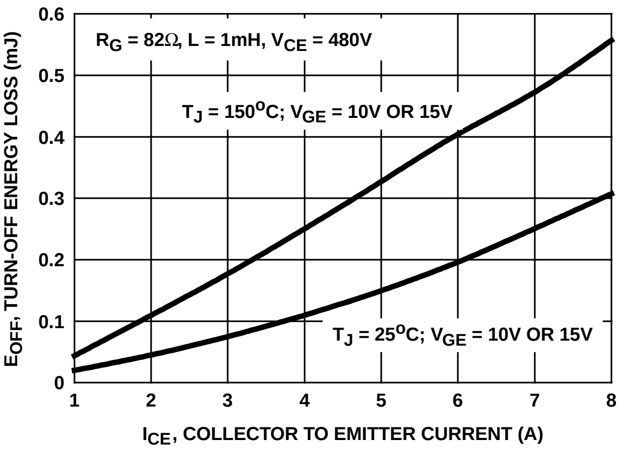


FIGURE 8. TURN-OFF ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT

Typical Performance Curves Unless Otherwise Specified **(Continued)**

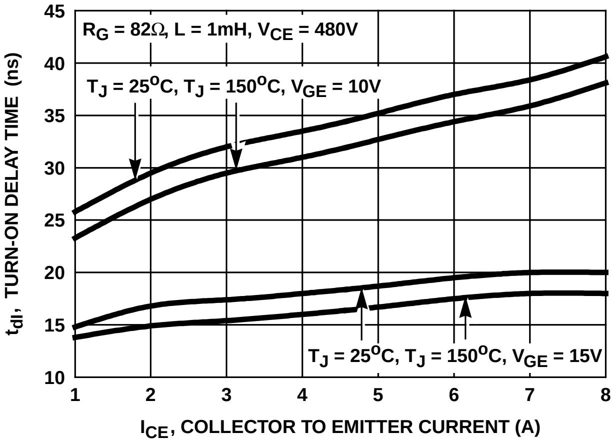


FIGURE 9. TURN-ON DELAY TIME vs COLLECTOR TO EMITTER CURRENT

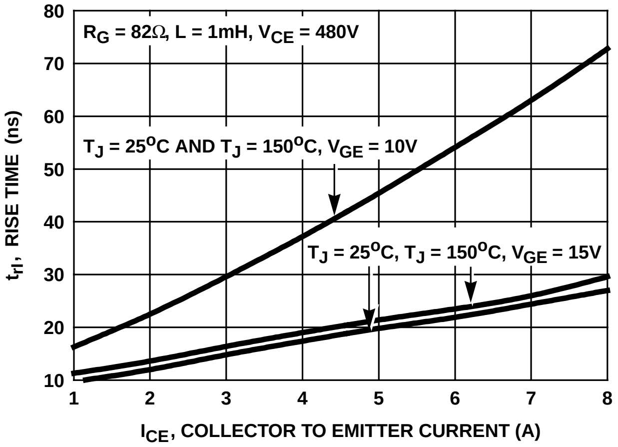


FIGURE 10. TURN-ON RISE TIME vs COLLECTOR TO EMITTER CURRENT

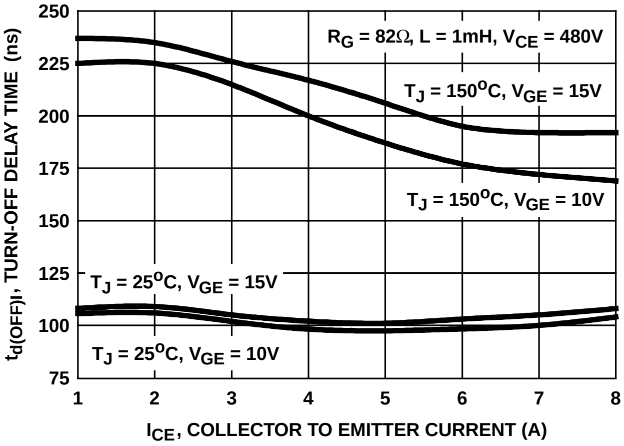


FIGURE 11. TURN-OFF DELAY TIME vs COLLECTOR TO EMITTER CURRENT

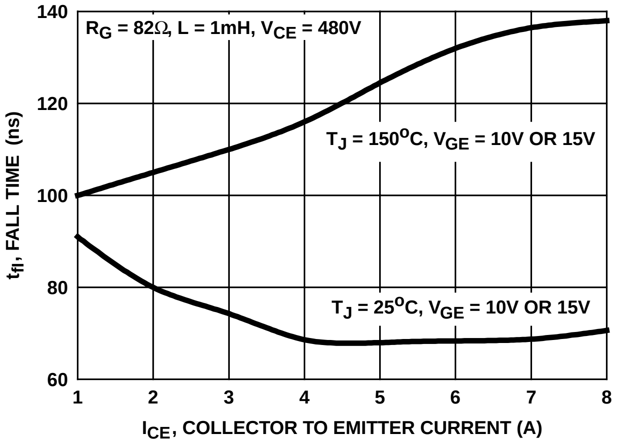


FIGURE 12. FALL TIME vs COLLECTOR TO EMITTER CURRENT

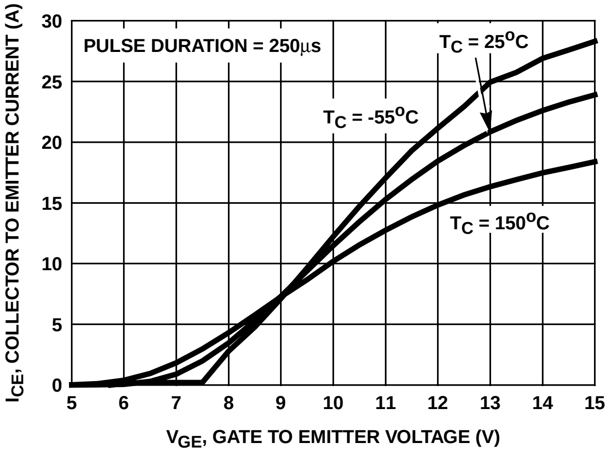


FIGURE 13. TRANSFER CHARACTERISTIC

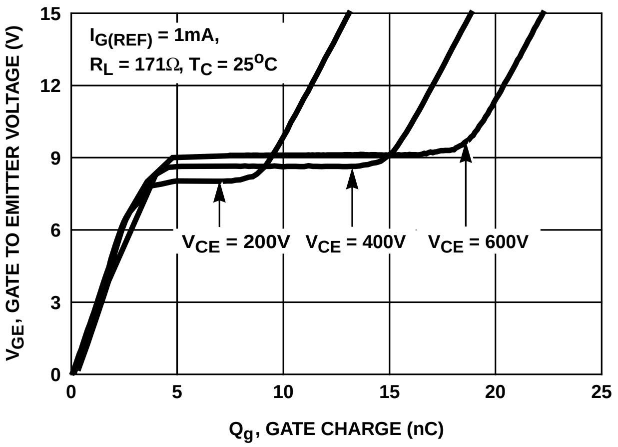


FIGURE 14. GATE CHARGE WAVEFORMS

Typical Performance Curves Unless Otherwise Specified **(Continued)**

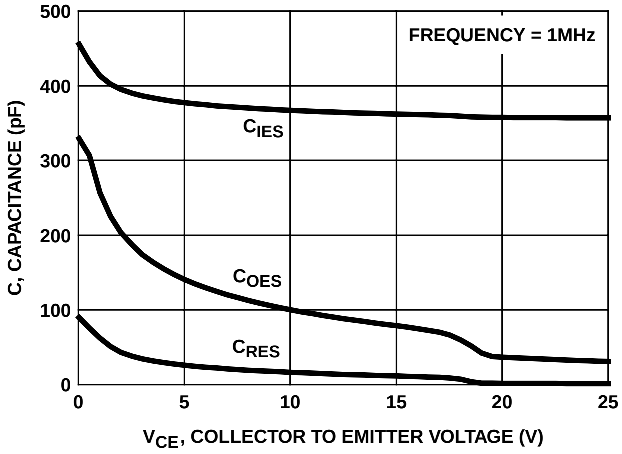


FIGURE 15. CAPACITANCE vs COLLECTOR TO EMITTER VOLTAGE

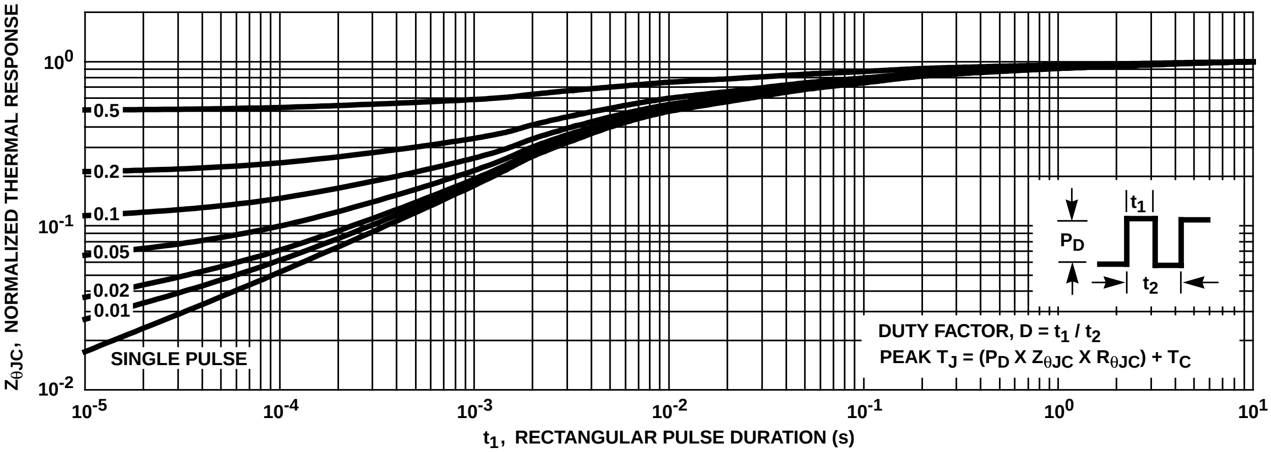
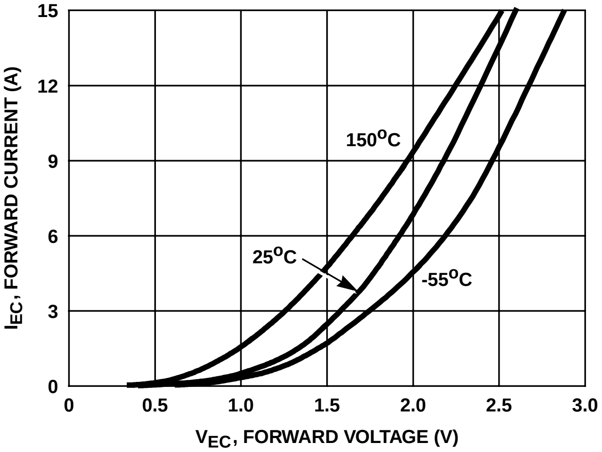


FIGURE 16. NORMALIZED TRANSIENT THERMAL RESPONSE, JUNCTION TO CASE



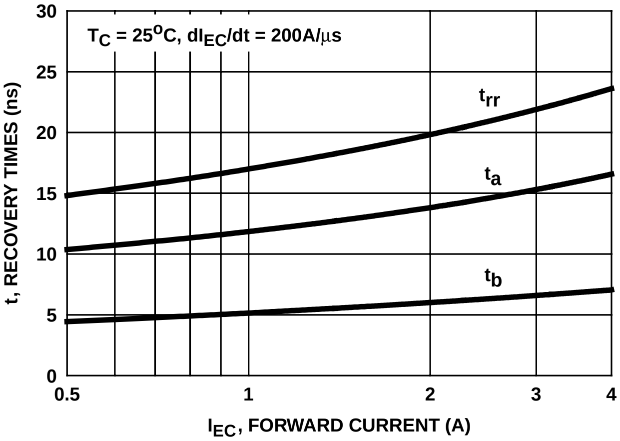


FIGURE 17. DIODE FORWARD CURRENT vs FORWARD VOLTAGE DROP

FIGURE 18. RECOVERY TIME vs FORWARD CURRENT

Test Circuit and Waveforms

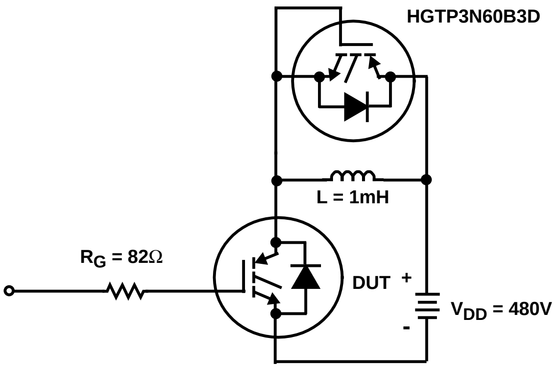


FIGURE 19. INDUCTIVE SWITCHING TEST CIRCUIT

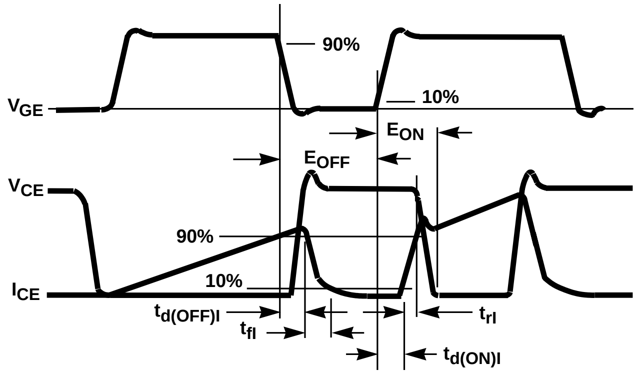


FIGURE 20. SWITCHING TEST WAVEFORMS

Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD LD26™" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic Zener diode from gate to emitter. If gate protection is required an external Zener is recommended.

Operating Frequency Information

Operating frequency information for a typical device (Figure 3) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 5, 6, 7, 8, 9 and 11. The operating frequency plot (Figure 3) of a typical device shows f_{MAX1} or f_{MAX2}; whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{d(OFF)I} + t_{d(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{d(OFF)I}$ and $t_{d(ON)I}$ are defined in Figure 20. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JM}. $t_{d(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JM} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 3) and the conduction losses (P_C) are approximated by $P_C = V_{CE} \times I_{CE})/2$.

E_{ON} and E_{OFF} are defined in the switching waveforms shown in Figure 20. E_{ON} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e., the collector current equals zero ($I_{CE} = 0$).

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