HOLT INTEGRATED CIRCUITS INC.

HI-8683, HI-8684

ARINC INTERFACE DEVICE

ARINC 429 & 561 Serial Data to 8-Bit Parallel Data

September 2006

DESCRIPTION

The HI-8683 and HI-8684 are system components for interfacing incoming ARINC 429 signals to 8-bit parallel data using proven +5V analog/digital CMOS technology. The HI-8683 is a digital device that requires an external analog line receiver such as the HI-8482 or HI-8588 between the ARINC bus and the device inputs. The HI-8684 incorporates the digital logic and analog line receiver circuitry in a single device.

The HI-8683 is also available as a second source to the DLS-112 with the original 18 pin DIP and 28 pin PLCC package pinouts.

The receivers on the HI-8684 connect directly to the ARINC 429 Bus and translate the incoming signals to normal CMOS levels. Internal comparator levels are set just below the standard 6.5 volt minimum data threshold and just above the standard 2.5 volt maximum null threshold. The -10 version of the HI-8684 allows the incorporation of an external 10KΩ resistance in series with each ARINC input for lightning protection without affecting ARINC level detection.

Both products offer high speed 8-bit parallel bus interface, a 32-bit buffer, and error detection for word length and parity. A reset pin is also provided for power-on initialization.

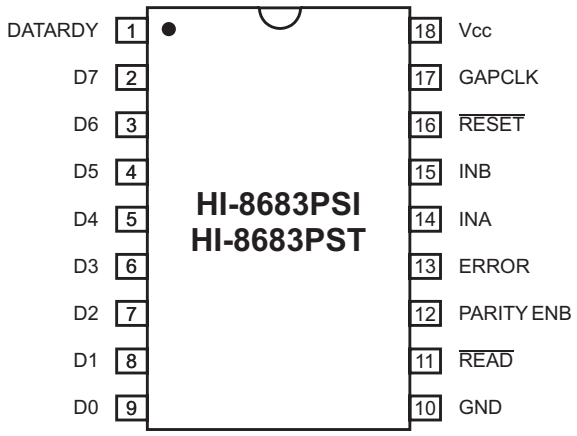
FEATURES

- Automatic conversion of serial ARINC 429, 575 & 561 data to 8-bit parallel data
- High speed parallel 8-bit data bus
- Error detection - word length and parity
- Reset input for power-on initialization
- On-chip line receiver option (HI-8684)
- Input hysteresis of at least 2 volts (HI-8684)
- Test inputs bypass analog inputs (HI-8684)
- Simplified lightning protection with the ability to add 10 Kohm external series resistors (HI-8684-10)
- Plastic package options - surface mount (SOIC), PLCC and DIP
- Military processing available

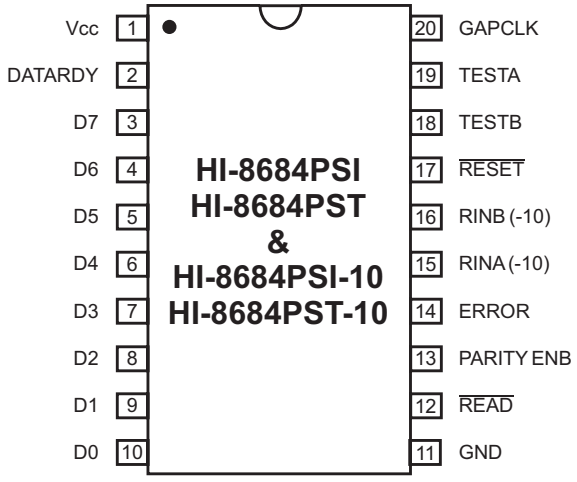
APPLICATIONS

- Avionics data communication
- Serial to parallel conversion
- Parallel to serial conversion

PIN CONFIGURATIONS (Top View)



HI-8683
18-Pin Plastic SOIC - WB Package



HI-8684
20-Pin Plastic SOIC - WB Package

(See page 8 for additional pin configurations)

PIN DESCRIPTIONS

SIGNAL	FUNCTION	DESCRIPTION
DATA RDY	OUTPUT	Receiver data ready flag. A high level indicates data is available in the receive buffer. Flag goes low when the first 8-bit byte is read.
D0 to D7	OUTPUT	8-bit parallel data bus (tri-state)
GND	POWER	0V
$\overline{\text{READ}}$	INPUT	Read strobe. A low level transfers receive buffer data to the data bus
PARITY ENB	INPUT	Parity Enable - A high level activates odd parity checking which replaces the 32nd ARINC bit with an error bit. Otherwise, the 32nd ARINC bit is unchanged
ERROR	OUTPUT	Error Flag. A high level indicates a bit count error (number of ARINC bits was less than or greater than 32) and/or a parity error if parity detection was enabled (PARITY ENB high)
INA	INPUT	Positive digital serial data input (HI-8683 only)
INB	INPUT	Negative digital serial data input (HI-8683 only)
RINA/RINA-10	INPUT	Positive direct ARINC serial data input (HI-8684 & HI-8684-10 only)
RINB/RINB-10	INPUT	Negative direct ARINC serial data input (HI-8684 & HI-8684-10 only)
$\overline{\text{RESET}}$	INPUT	Internal logic states are initialized with a low level
TESTA	INPUT	Used in conjunction with the TESTB input to bypass the built-in analog line receiver circuitry (HI-8684 & HI-8684-10 only)
TESTB	INPUT	Used in conjunction with the TESTA input to bypass the built-in analog line receiver circuitry (HI-8684 & HI-8684-10 only)
GAPCLK	INPUT	Gap Clock. Determines the minimum time required between ARINC words for detection. The minimum word gap time is between 16 and 17 clock cycles of this signal.
Vcc	POWER	+5V ±5% supply

FUNCTIONAL DESCRIPTION

The HI-8683 and HI-8684 are serial to 8-bit parallel converters. The incoming data stream is serially shifted into an input register, checked for errors, and then transferred in parallel to a 32-bit receive buffer. The receive data can be accessed using four 8-bit parallel read operations while the next serial data steam is being received.

RECEIVER INPUTS

Figure 1 is a block diagram of both the HI-8683 and HI-8684. The difference between the two products is the HI-8684 has a built-in line receiver whereas the HI-8683 is strictly a digital device and requires an external ARINC line receiver such as the Holt HI-8444, HI-8445, HI-8448 , HI-8482 or HI-8588 to interface to the ARINC 429 bus.

HI-8684 Line Receiver

Internal 35KΩ resistors are in series with both the RINA and RINB ARINC 429 inputs. They connect to level translators whose resistance to GND is typically 10KΩ. After level translation, the buffered inputs drive a differential amplifier. The differential signal is compared to levels derived from a divider between VCC and GND. The nominal settings correspond to a One/Zero amplitude of 6.0V and a Null amplitude of 3.3V. A valid ARINC One/Zero input sets a latch and a Null input resets the latch.

Since any added external series resistance will affect the voltage translation, the HI-8684-10 is available with 25KΩ of the 35KΩ series resistance required for proper ARINC 429 level detection. The remaining 10KΩ required that must be added can be incorporated in other external circuitry such as lightning protection. Except for the different input series resistance, the HI-8684 and HI-8684-10 are identical.

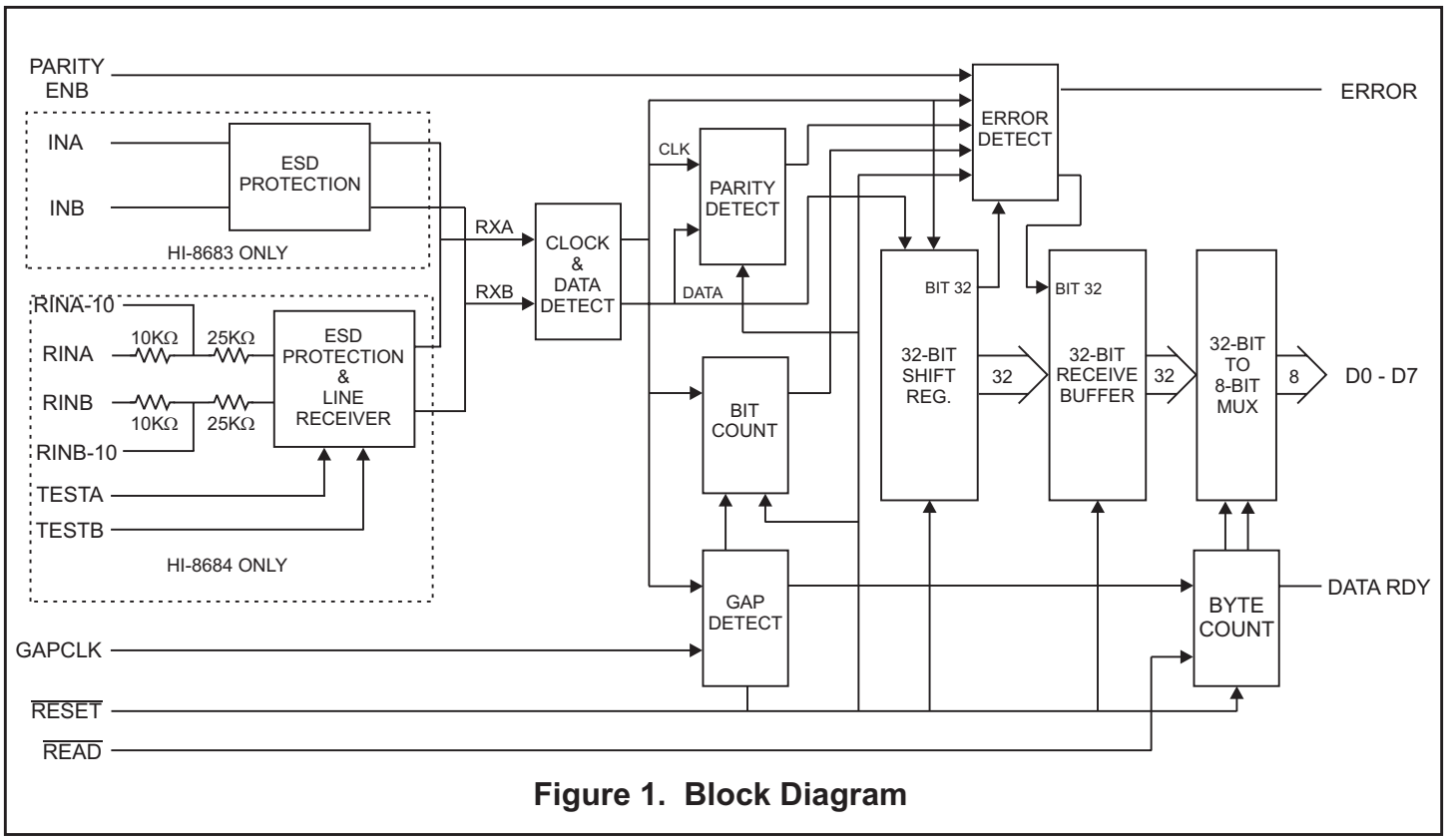


Figure 1. Block Diagram

FUNCTIONAL DESCRIPTION (cont.)

PROTOCOL DETECTION

ARINC clock and data in the HI-8683 are derived from the two streams of digital data at the INA and INB inputs and the resulting One/Zero data is shifted into a 32-bit input register as illustrated in Figure 3.

In the HI-8684, the One/Zero data shifted into the input register is created from either the two digital outputs of the built-in line receiver (Figure 3) or the TESTA and TESTB inputs (Figure 4).

For ARINC 561 operation, the INA and INB data streams inputs must be derived from the ARINC 561 data, clock and sync with external logic.

GAP DETECTION

The end of a data word is detected by an internal counter that times out when a data One or Zero is not received for a period equal to 16 cycles of the GAPCLK signal. The gap detection time may vary between 16 and 17 cycles of the GAPCLK signal since the incoming data and GAPCLK are not usually synchronous inputs. The required frequency of GAPCLK is a function of the mininum gap time specified for the type of ARINC data being received. Table 1 indicates typical frequencies that may be used for the various data rates normally encountered.

DATABUS TYPE	BIT PERIOD (µs)	MINIMUM GAP (µs)	GAP CLOCK MHz	GAP DETECTION TIME (µs)
429	10	45	0.75 1.0 1.5	21.3 - 22.7 16 - 17 10.7 - 11.3
429	69 - 133	310 - 599	0.1	160 - 170
575	69 - 133	310 - 599	0.1	160 - 170
561	69 - 133	103 - 200	0.2	80 - 85

Table 1 - Typical Gap Detection Times

FUNCTIONAL DESCRIPTION (cont.)

ERROR CHECKING

Once a word gap is detected, the data word in the input register is transferred to the receive buffer and checked for errors.

When parity detection is enabled (PARITY ENB high), the received word is checked for odd parity. If there is a parity error, the 32nd bit of the received data word is set high.

If parity checking is disabled (PARITY ENB low) the 32nd bit of the data word is always the 32nd ARINC bit received.

The ERROR flag output is set high upon receipt of a word gap and the number of bits received since the previous word gap is less than or greater than 32. The ERROR flag is reset low when the next valid ARINC word is written into the receive buffer or when $\overline{\text{RESET}}$ is pulsed low.

READING RECEIVE BUFFER

When the data word is transferred to the receive buffer, the DATA RDY pin goes high. The data word can then be read in four 8-bit bytes by pulsing the $\overline{\text{READ}}$ input low as indicated in Figure 5. The first read cycle resets DATA RDY low and increments an internal counter to the next 8-bit byte. The counter continues to increment on each read cycle until all four bytes are read. The relationship between each bit of an ARINC word received and each bit of the four 8-bit data bus bytes is specified in Figure 2.

When a new ARINC word is received it always overwrites the receive buffer. If the first byte of the previous word has not been read, then previous data is lost and the receive buffer will contain the new ARINC word. However, if the DATA RDY pin goes high between the reading of the first and fourth bytes, the previous read bytes are no longer valid because the unread bytes have been overwritten by the new ARINC word. Also, the next read will be of the first byte of the new ARINC word since the internal byte counter is always reset to the first byte when new data is transferred to the receive buffer.

Read	Byte	Data Bus Bits	ARINC Bits
1st	Byte 1	D0 - D7	ARINC 1 - ARINC 8
2nd	Byte 2	D0 - D7	ARINC 9 - ARINC 16
3rd	Byte 3	D0 - D7	ARINC 17 - ARINC 24
4th	Byte 4	D0 - D7	ARINC 25 - ARINC 32

FIGURE 2. ORDER OF RECEIVED DATA

RESET

A low on the $\overline{\text{RESET}}$ input sets a flip-flop which initializes the internal logic. When $\overline{\text{RESET}}$ goes high, the internal logic remains in the initialized state until the first word gap is detected preventing reception of a partial word.

TEST MODE (HI-8684 only)

The built-in differential line receiver on the HI-8684 can be disabled allowing the data and clock detection circuitry to be driven directly with digital signals. The logical OR function of the TESTA and TESTB is defined in Truth Table 1. The two inputs can be used for testing the receiver logic and for inputting ARINC 429 type data derived from another source / protocol. See Figure 4 for typical test input timing.

The device should always be initialized with $\overline{\text{RESET}}$ immediately after entering the test mode to clear a partial word that may have been received since the last word gap. Otherwise, an ERROR condition may occur and the first 32 bits of data on the test inputs may not be properly received.

Also, when entering the test mode, both TESTA and TESTB should be set high and held in that state for at least one word gap period (17 gap clocks) after $\overline{\text{RESET}}$ goes high.

When exiting the test mode, both test inputs should be held low and the device initialized with $\overline{\text{RESET}}$.

TRUTH TABLE 1.

RINA	RINB	TESTA	TESTB	RXA	RXB
-1.50 to +1.50V	-1.50V to +1.50V	0	0	0	0
-3.25V to -6.50V	+3.25V to +6.50V	0	0	0	1
+3.25V to +6.50V	-3.25V to -6.50V	0	0	1	0
X	X	0	1	0	1
X	X	1	0	1	0
X	X	1	1	0	0

X = don't care

TIMING DIAGRAMS

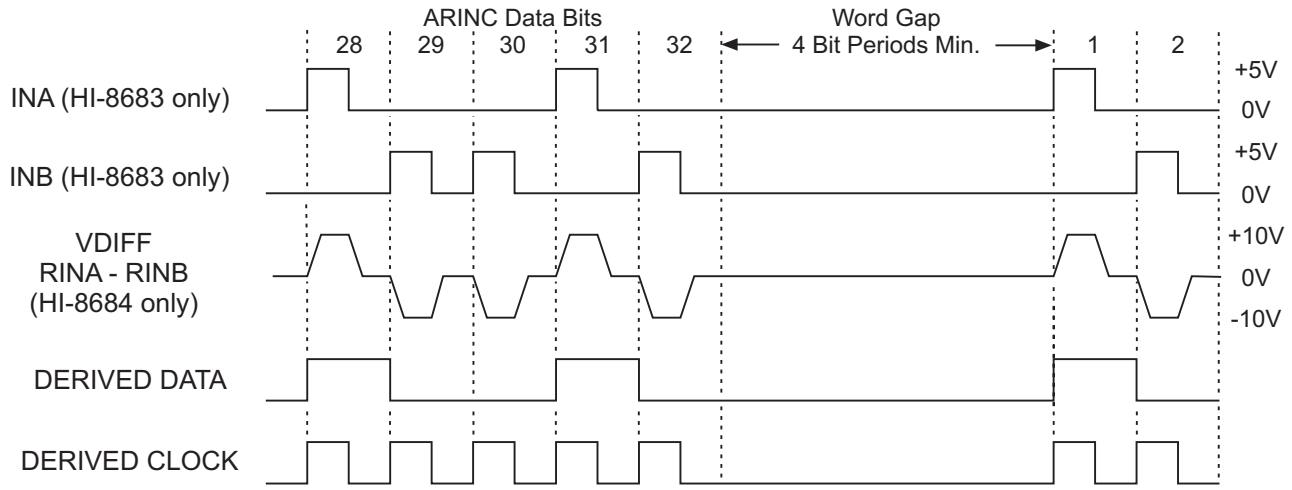


FIGURE 3 - RECEIVER INPUT TIMING FOR ARINC 429

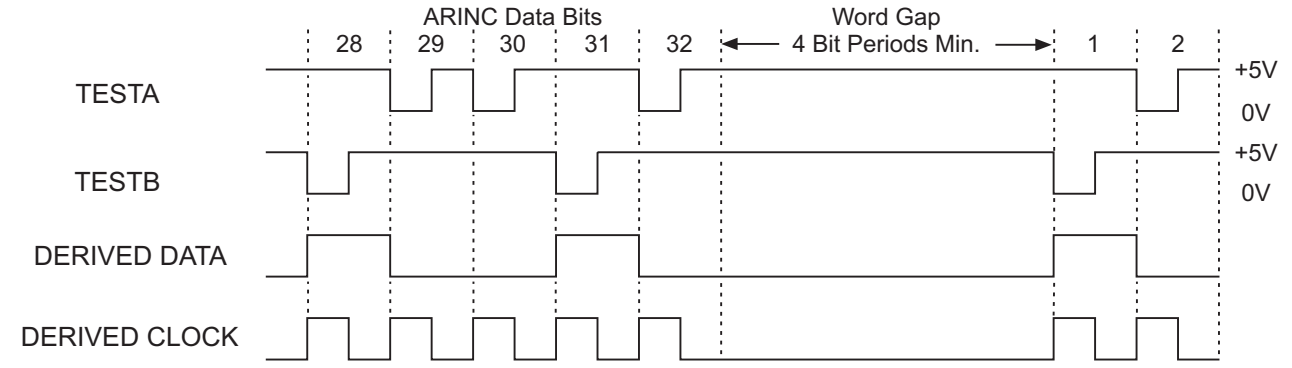


FIGURE 4 - TEST INPUT TIMING FOR ARINC 429

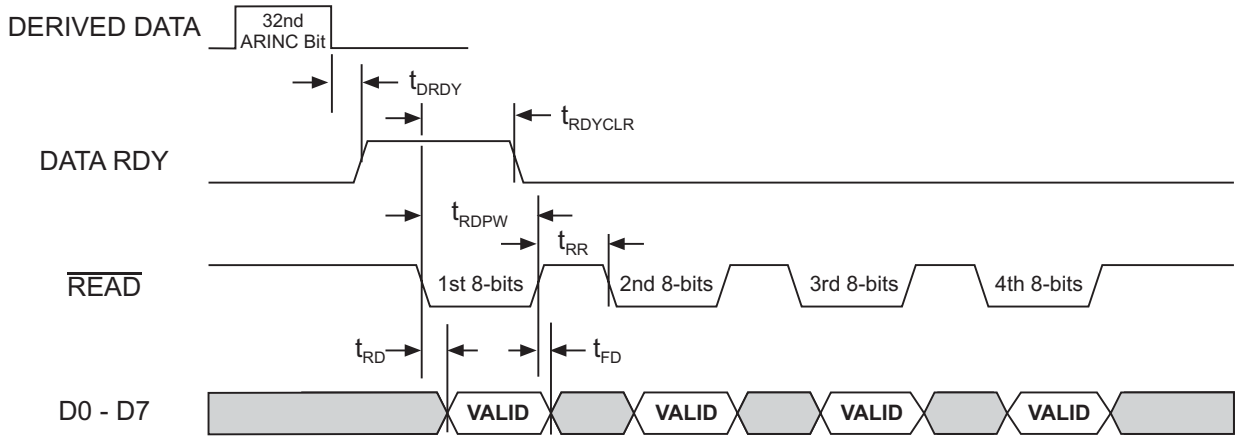


FIGURE 5 - RECEIVER PARALLEL DATABUS TIMING

ABSOLUTE MAXIMUM RATINGS

All voltages referenced to GND

Supply voltages
V_{CC} ..... +7.0V

Voltage on inputs
RINA (-10) to RINB (-10) ..... +29V to - 29V
All other input pins.....-0.3 to Vcc +0.3

DC current per input pin ..... +10mA

Power dissipation at 25°C
plastic 18-pin SO..... 1.9W, derate 15.4mW/°C
plastic 18-pin DIP.....1.6W, derate 13.3mW/°C
plastic 20-pin SO.....1.4W, derate 11.5mW/°C
plastic 20-pin PLCC .2.0W, derate 17.2mW/°C

Solder Temperature
Leads ..... +280°C for 10 sec
Package body .....+220°C

Storage Temperature ..... -65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltages
V_{CC}.....+5V ± 5%

Temperature Range
Industrial Screening ..... -40°C to +85°C
Hi-Temp Screening ..... -55°C to +125°C
Military Screening.....-55°C to +125°C

Junction Temperature, Tj ..... ≤+175°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

DC ELECTRICAL CHARACTERISTICS

Vcc = 5V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ARINC Bus Inputs (RINA & RINB, HI-8684 only)						
Differential input voltage						
one or zero	V_{DIN}	differential voltage	6.5	10.0	13.0	volts
null	V_{NIN}	" " " "	-	-	2.75	volts
common mode	V_{COM}	with respect to GND	-	-	5.0	volts
Input resistance						
RINA (-10) to RINB (-10)	R_{DIFF}	supplies floating	30	75	-	Kohm
RINA (-10) or RINB (-10) to GND or V_{CC}	R_{SUP}	" " " '	19	40	-	Kohm
Input capacitance (Guaranteed but not tested)						
differential	C_{DIFF}	RINA to RINB	-	-	20	pF
to GND	C_G		-	-	20	pF
to V_{CC}	C_H		-	-	20	pF
Digital Inputs (INA, INB, $\overline{\text{RESET}}$, GAPCLK, $\overline{\text{READ}}$ & PARITY ENB)						
Input voltage						
high	V_{IH}		2.0	-	V_{CC}	volts
low	V_{IL}		0.0	-	0.8	volts
Input current						
source	I_{IH}	V_{IN} = 5.0V	-	-	1.0	µA
sink	I_{IL}	V_{IN} = 0.0V	-1.0	-	-	µA
Input capacitance	C_I		-	-	8.0	pF

DC ELECTRICAL CHARACTERISTICS (cont.)

Vcc = 5V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Digital Inputs (TESTA & TESTB)						
Input voltage high low	 V_{IH} V_{IL}		 2.4 0.0	 - -	 V_{CC} 0.8	 volts volts
Input current source sink	 I_{IH} I_{IL}	 V_{IN} = 5.0V V_{IN} = 0.0V	 - -1.0	 110 -	 - -	 µA µA
Input capacitance	C_I		-	-	8.0	pF
Outputs (D0 to D7, ERROR & DATA RDY)						
Output voltage high low	 V_{OH} V_{OL}	 I_{OH} = -1.0 mA I_{OL} = 1.6 mA	 2.7 -	 - -	 - 0.4	 volts volts
Output tri-state current (D0 - D7 only)	 I_{IH} I_{IL}	 V_{OH} = 5.0V V_{OL} = 0.0V	 - -1.0	 - -	 1.0 -	 µA µA
Output capacitance	C_O		-	-	15	pF
Operating Supply Current						
V_{CC} (HI-8683 only)	I_{CC1}	V_{IN} = 0.0V, outputs open	-	-	1.0	mA
V_{CC} (HI-8684 only)	I_{CC2}	V_{IN} = 0.0V, outputs open	-	-	6.5	mA

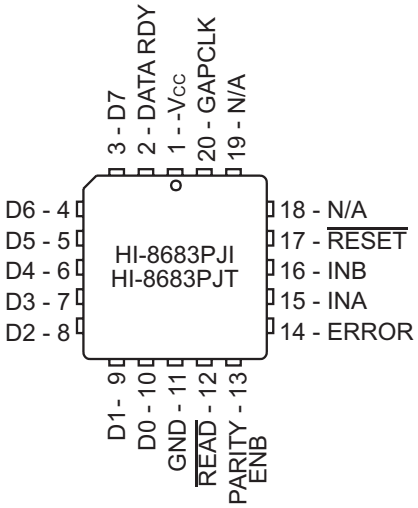
AC ELECTRICAL CHARACTERISTICS

Vcc = 5V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

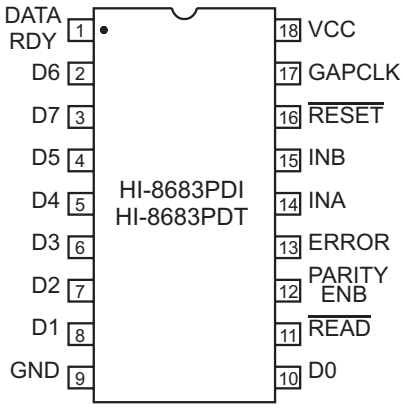
PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{READ}}$ pulse width	t_{RDPW}		50			ns
Data delay from $\overline{\text{READ}}$	t_{RD}				40	ns
$\overline{\text{READ}}$ to data floating	t_{FD}				20	ns
$\overline{\text{READ}}$ to DATA RDY clear	t_{RDYCLR}				35	ns
$\overline{\text{READ}}$ pulse to next $\overline{\text{READ}}$ pulse	t_{RR}		25			ns
GAPCLK frequency	f_{GC}			1		MHz
32 ARINC bit to DATA RDY	t_{DRDY}		16		17	clocks

HI-8683 & HI-8684 PIN CONFIGURATIONS

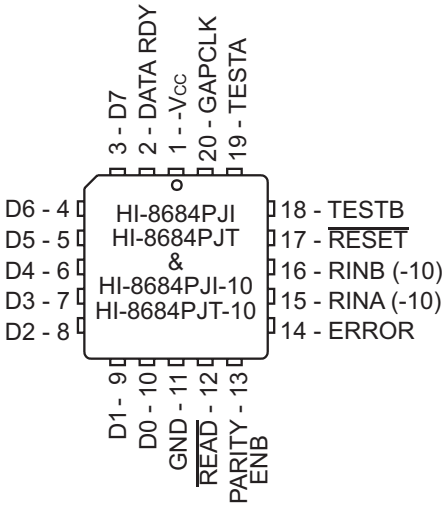
(See page 1 for additional pin configurations)



HI-8683
20-Pin Plastic PLCC



HI-8683
18-Pin Plastic DIP



HI-8684
20-Pin Plastic PLCC

ORDERING INFORMATION

HI - 868xxx x x - xx

PART NUMBER (1)	INPUT SERIES RESISTANCE	
	BUILT-IN	REQUIRED EXTERNALLY
No dash number	35 Kohm	0
-10	25 Kohm	10 Kohm

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

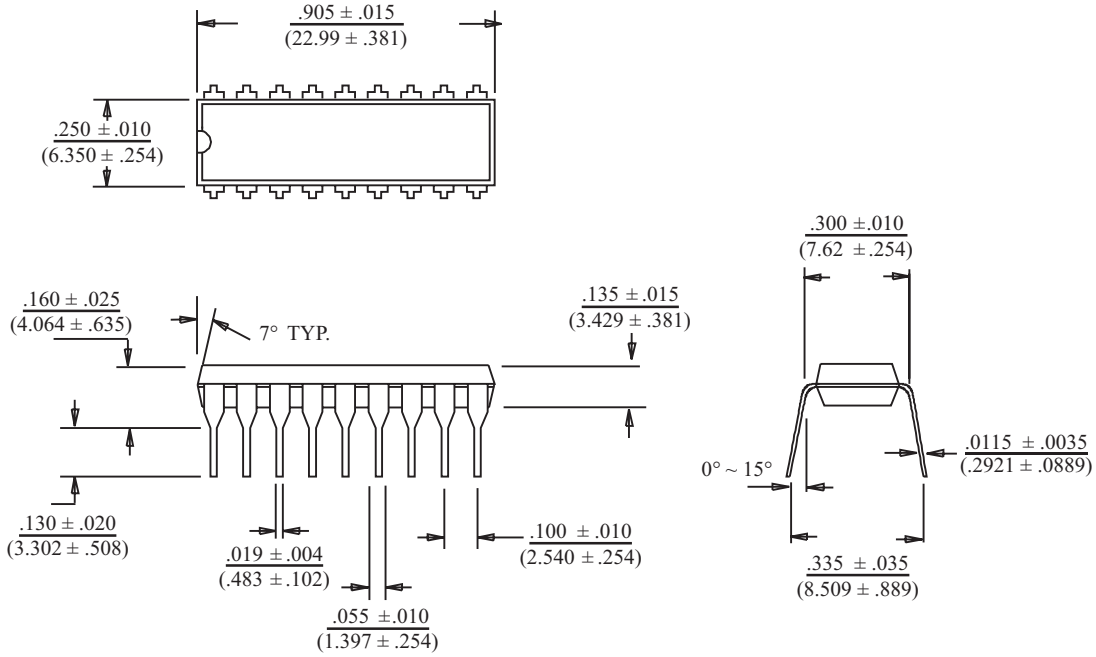
PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	NO
T	-55°C TO +125°C	T	NO

PART NUMBER	PACKAGE DESCRIPTION	BUILT-IN LINE RECV'R
8683PD	18 PIN PLASTIC DIP	NO
8683PJ	20 PIN PLASTIC PLCC	NO
8683PS	18 PIN PLASTIC SOIC - WB	NO
8684PJ	20 PIN PLASTIC PLCC	YES
8684PS	20 PIN PLASTIC SOIC - WB	YES

Legend: WB - Wide Body
(1): Only available with 'HI-8684'

18-PIN PLASTIC DIP

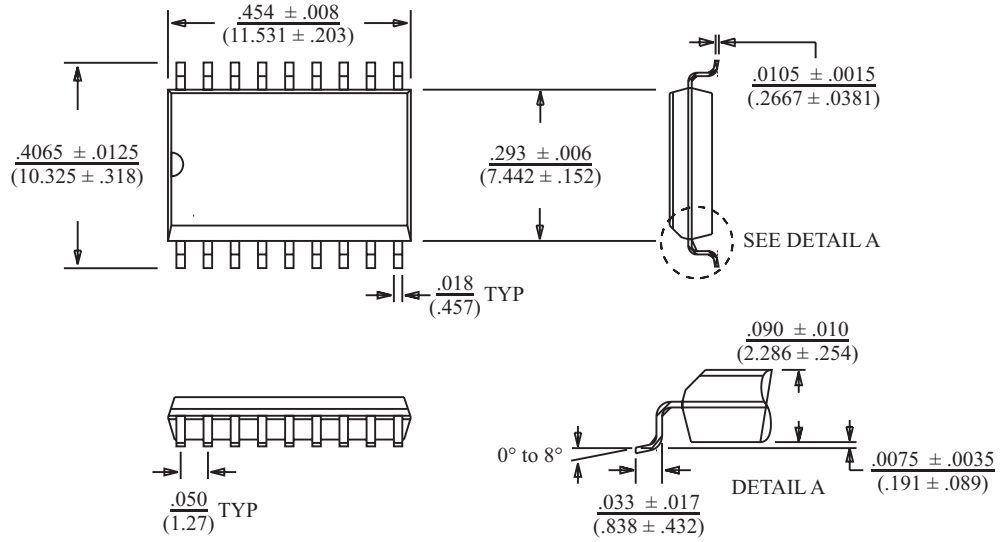
Package Type: 18P



18-PIN PLASTIC SMALL OUTLINE (SOIC) - WB

(Wide Body)

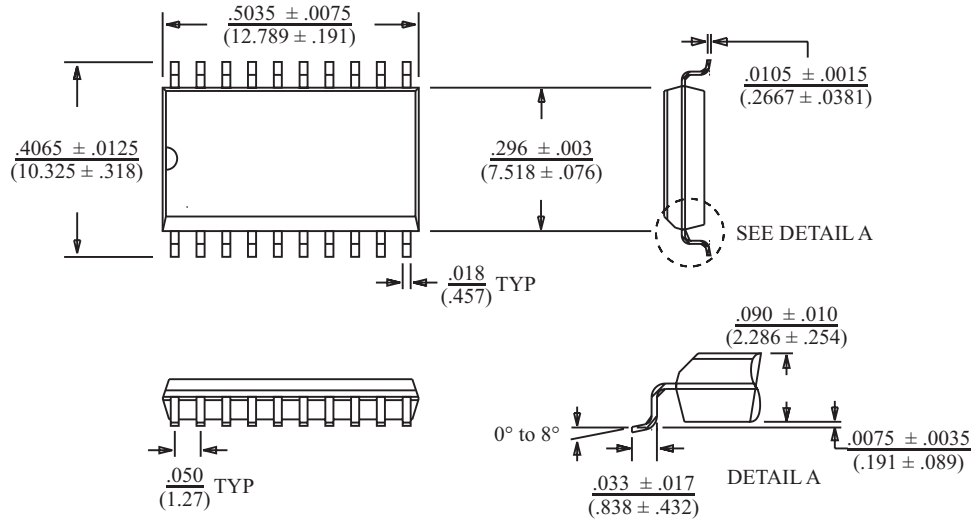
Package Type: 18HW



20-PIN PLASTIC SMALL OUTLINE (SOIC) - WB

(Wide Body)

Package Type: 20HW



20-PIN PLASTIC PLCC

Package Type: 20J