Data Sheet June 1999 File Number 2937.8

6-Bit, 30MSPS, Flash A/D Converter

The HI-5701 is a monolithic, 6-bit, CMOS flash Analog-to-Digital Converter. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 30MSPS speed is made possible by a parallel architecture which also eliminates the need for an external sample and hold circuit. The HI-5701 delivers ±0.7 LSB differential nonlinearity while consuming only 250mW (Typ) at 30MSPS. Microprocessor compatible data output latches are provided which present valid data to the output bus 1.5 clock cycles after the convert command is received. An overflow bit is provided to allow the series connection of two converters to achieve 7-bit resolution.

The HI-5701 is available in Commercial and Industrial temperature ranges and is supplied in 18 lead Plastic DIP and SOIC packages

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI3-5701K-5	0 to 70	18 Ld PDIP	E18.3
HI9P5701K-5	0 to 70	18 Ld SOIC	M18.3
HI3-5701B-9	-40 to 85	18 Ld PDIP	E18.3
HI9P5701B-9	-40 to 85	18 Ld SOIC	M18.3
HI5701-EV	25	Evaluation Board	

Features

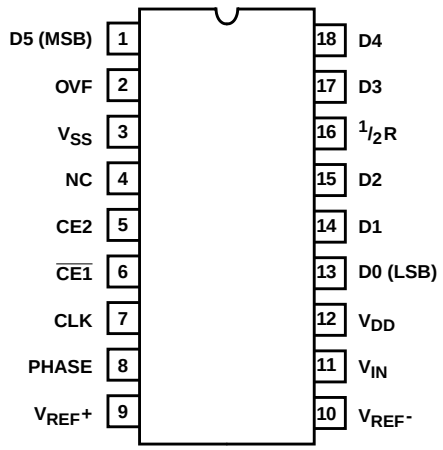
- 30MSPS with No Missing Codes
- Full Power Input Bandwidth 20MHz
- No Missing Codes Over Temperature
- Sample and Hold Not Required
- Single Supply Voltage. . . . . +5V
- Power Dissipation (Max). 300mW
- CMOS/TTL Compatible
- Overflow Bit
- /883 Version Available

Applications

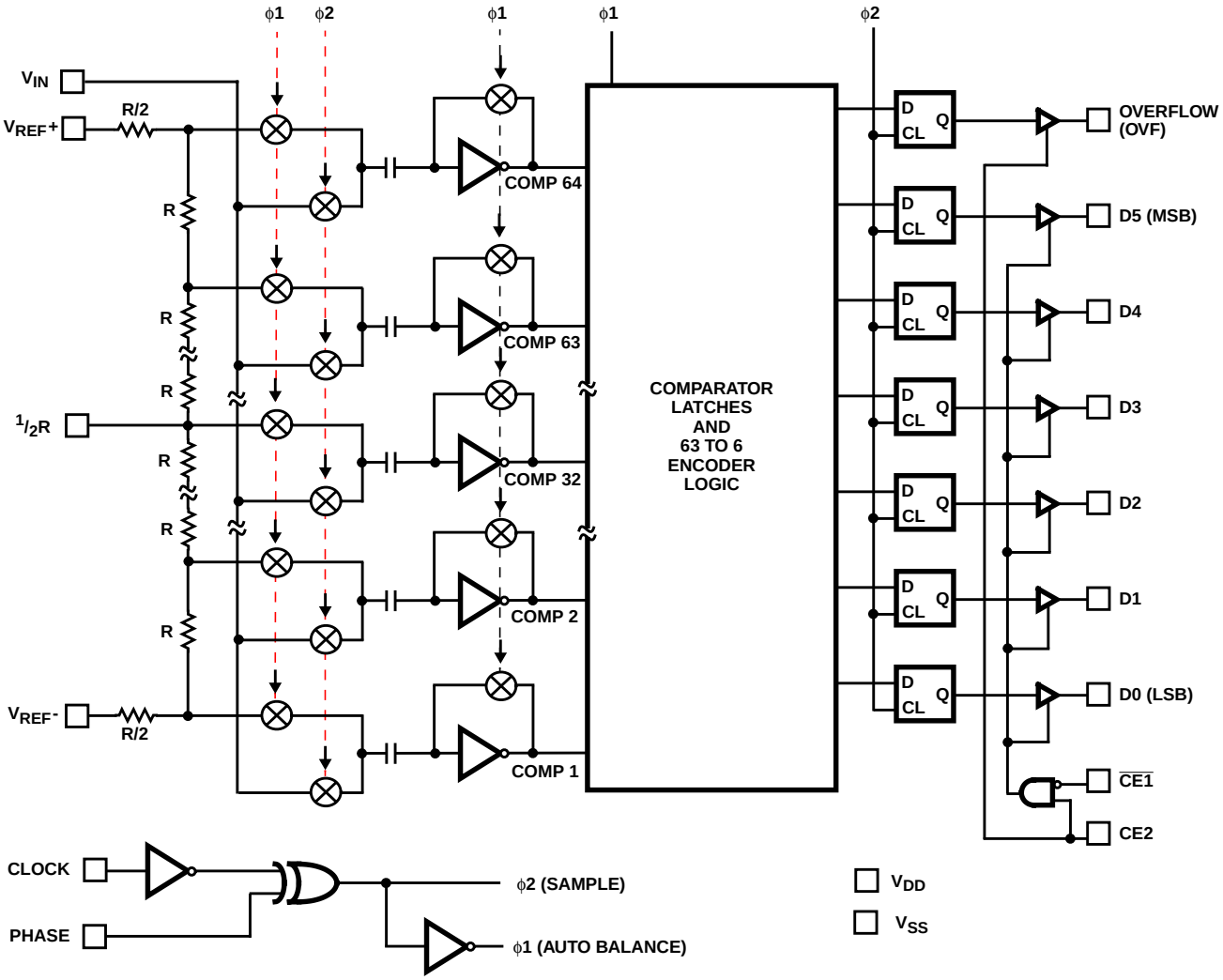
- Video Digitizing
- Radar Systems
- Communication Systems
- High Speed Data Acquisition Systems

Pinout

HI-5701
(PDIP, SOIC)
TOP VIEW



Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage, V_{DD} to V_{SS} . . . . . (V_{SS} - 0.5) < V_{DD} < +7V
Analog and Reference Input Pins (V_{SS} - 0.5) < V_{INA} < (V_{DD} +0.5V)
Digital I/O Pins . . . . . .(V_{SS} - 0.5) < $V_{I/O}$ < (V_{DD} +0.5V)

Operating Conditions

Temperature Range
HI3-5701-5 . . . . . 0°C to 70°C
HI9P5701-9 . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	75
SOIC Package	105

Maximum Power Dissipation at 70°C (Note 2) 635mW
Maximum Junction Temperature . . . . . .150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . .300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Electrical Specifications

V_{DD} = +5.0V; V_{REF}+ = +4.0V; V_{REF-} = V_{SS} = GND; f_S = Specified Clock Frequency at 50% Duty Cycle; C_L = 30pF; Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	25°C			(NOTE 3) 0°C TO 70°C -40°C TO 85°C		UNITS
		MIN	TYP	MAX	MIN	MAX	
SYSTEM PERFORMANCE							
Resolution		6	-	-	6	-	Bits
Integral Linearity Error, INL (Best Fit Line)	f_S = 20MHz	-	±0.5	±1.25	-	±2.0	LSB
	f_S = 30MHz	-	±1.5	-	-	-	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	f_S = 20MHz	-	±0.3	±0.6	-	±0.75	LSB
	f_S = 30MHz	-	±0.7	-	-		LSB
Offset Error, V_{OS} (Adjustable to Zero)	f_S = 20MHz (Note 3)	-	±0.5	±2.0	-	±2.5	LSB
	f_S = 30MHz	-	±0.5	-	-	-	LSB
Full Scale Error, FSE (Adjustable to Zero)	f_S = 20MHz (Note 3)	-	±0.25	±2.0	-	±2.5	LSB
	f_S = 30MHz	-	±0.25	-	-	-	LSB
DYNAMIC CHARACTERISTICS							
Maximum Conversion Rate	No Missing Codes	30	40	-	30	-	MSPS
Minimum Conversion Rate	No Missing Codes (Note 3)	-	-	0.125	-	0.125	MSPS
Full Power Input Bandwidth	f_S = 30MHz	-	20	-	-	-	MHz
Signal to Noise Ratio, SNR	f_S = 1MHz, f_{IN} = 100kHz	-	36	-	-	-	dB
$= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	f_S = 30MHz, f_{IN} = 4MHz	-	31	-	-	-	dB
Signal to Noise Ratio, SINAD	f_S = 1MHz, f_{IN} = 100kHz	-	35	-	-	-	dB
$= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_S = 30MHz, f_{IN} = 4MHz	-	30	-	-	-	dB
Total Harmonic Distortion	f_S = 1MHz, f_{IN} = 100kHz	-	-44	-	-	-	dBc
	f_S = 30MHz, f_{IN} = 4MHz	-	-38	-	-	-	dBc
Differential Gain	f_S = 14.32MHz, f_{IN} = 3.58MHz	-	2	-	-	-	%
Differential Phase	f_S = 14.32MHz, f_{IN} = 3.58MHz	-	2	-	-	-	Degree

Electrical Specifications V_{DD} = +5.0V; V_{REF}+ = +4.0V; V_{REF-} = V_{SS} = GND; f_S = Specified Clock Frequency at 50% Duty Cycle; C_L = 30pF; Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	25°C			(NOTE 3) 0°C TO 70°C -40°C TO 85°C		UNITS
		MIN	TYP	MAX	MIN	MAX	
ANALOG INPUTS							
Analog Input Resistance, R_{IN}	V_{IN} = 4V	-	30	-	-	-	MΩ
Analog Input Capacitance, C_{IN}	V_{IN} = 0V	-	20	-	-	-	pF
Analog Input Bias Current, IB	V_{IN} = 0V, 4V	-	0.01	±1.0	-	±1.0	µA
REFERENCE INPUTS							
Total Reference Resistance, R_L		250	370	-	235	-	Ω
Reference Resistance Tempco, T_C		-	+0.266	-	-	-	Ω/°C
DIGITAL INPUTS							
Input Logic High Voltage, V_{IH}		2.0	-	-	2.0	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	-	0.8	V
Input Logic High Current, I_{IH}	V_{IN} = 5V	-	-	1.0	-	1.0	µA
Input Logic Low Current, I_{IL}	V_{IN} = 0V	-	-	1.0	-	1.0	µA
Input Capacitance, C_{IN}		-	7	-	-	-	pF
DIGITAL OUTPUTS							
Output Logic Sink Current, I_{OL}	V_O = 0.4V	3.2	-	-	3.2	-	mA
Output Logic Source Current, I_{OH}	V_O = 4.5V	-3.2	-	-	-3.2	-	mA
Output Leakage, I_{OFF}	CE2 = 0V	-	-	±1.0	-	±1.0	µA
Output Capacitance, C_{OUT}	CE2 = 0V	-	5.0	-	-	-	pF
TIMING CHARACTERISTICS							
Aperture Delay, t_{AP}		-	6	-	-	-	ns
Aperture Jitter, t_{AJ}		-	30	-	-	-	ps
Data Output Enable Time, t_{EN}	(Note 3)	-	12	20	-	20	ns
Data Output Disable Time, t_{DIS}	(Note 3)	-	11	20	-	20	ns
Data Output Delay, t_{OD}	(Note 3)	-	14	20	-	20	ns
Data Output Hold, t_H	(Note 3)	5	10	-	5	-	ns
POWER SUPPLY REJECTION							
Offset Error PSRR, ΔV_{OS}	V_{DD} = 5V ±10%	-	±0.1	±1.0	-	±1.5	LSB
Gain Error PSRR, ΔFSE	V_{DD} = 5V ±10%	-	±0.1	±1.0	-	±1.5	LSB
POWER SUPPLY CURRENT							
Supply Current, I_{DD}	f_S = 20MHz	-	50	60	-	75	mA

NOTE:

3. Parameter guaranteed by design or characterization and not production tested.

Timing Waveforms

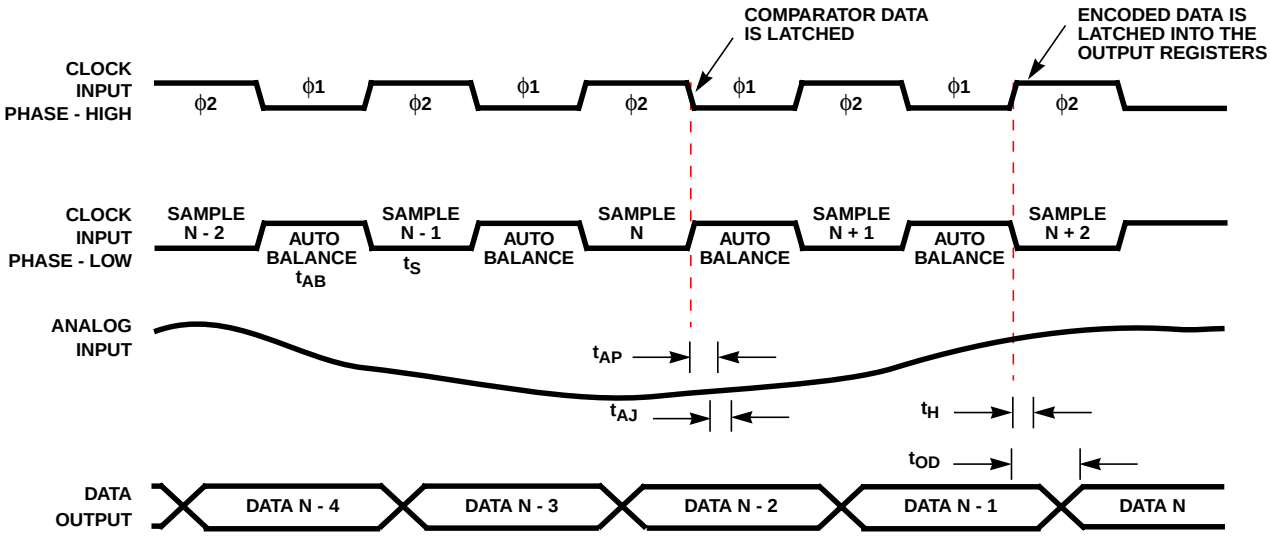


FIGURE 1. INPUT-TO-OUTPUT TIMING

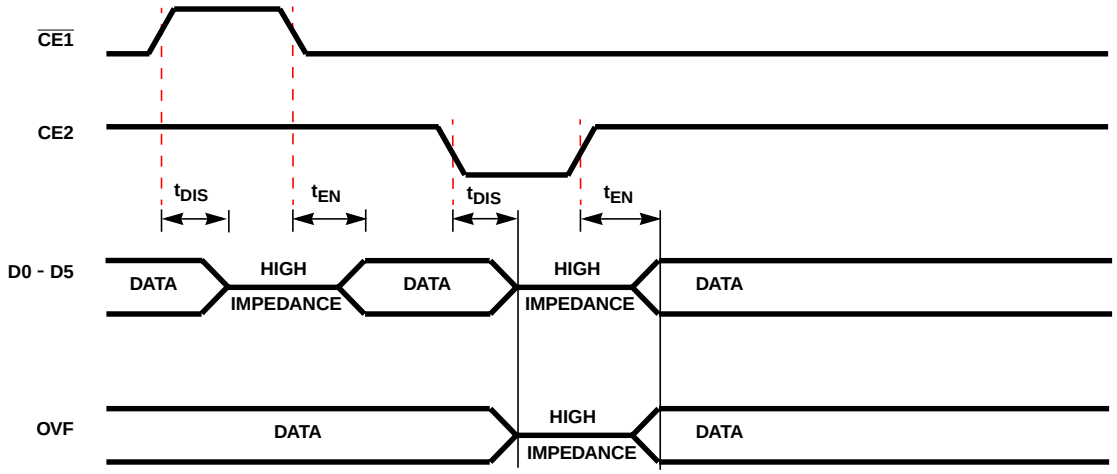


FIGURE 2. OUTPUT ENABLE TIMING

Typical Performance Curves

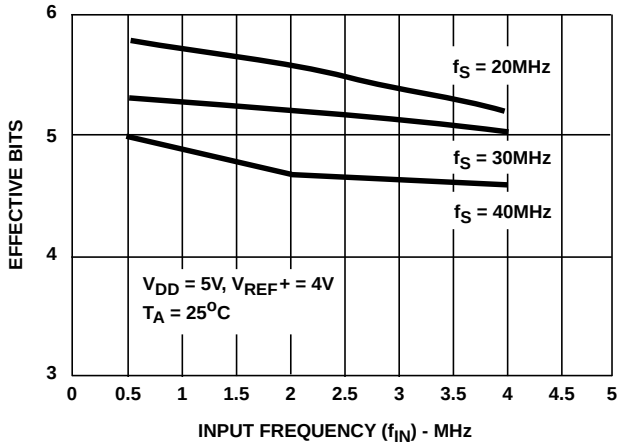


FIGURE 3. EFFECTIVE NUMBER OF BITS vs f_{IN}

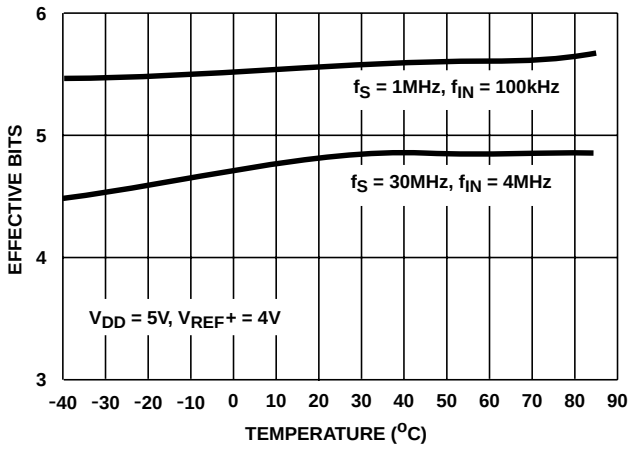


FIGURE 4. ENOB vs TEMPERATURE

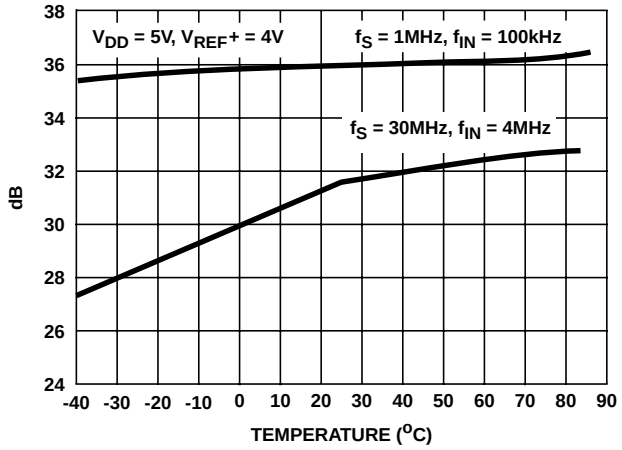


FIGURE 5. SNR vs TEMPERATURE

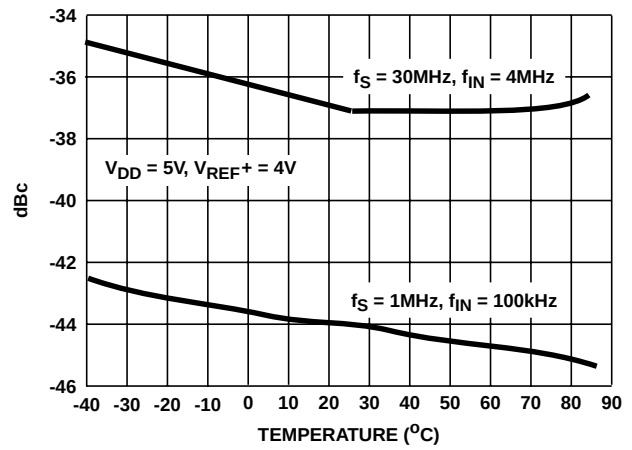


FIGURE 6. TOTAL HARMONIC DISTORTION vs TEMPERATURE

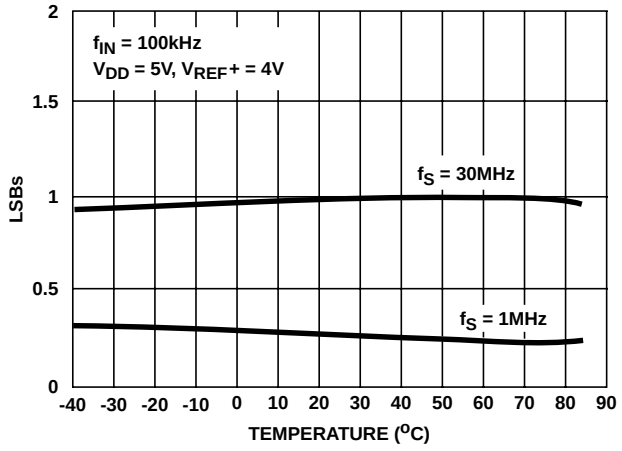


FIGURE 7. INL vs TEMPERATURE

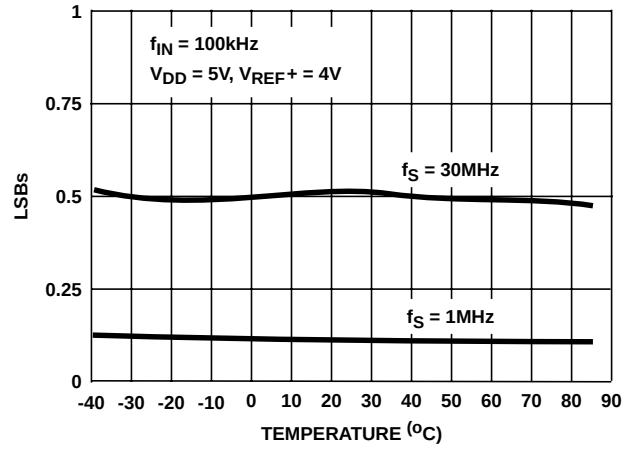


FIGURE 8. DNL vs TEMPERATURE

Typical Performance Curves (Continued)

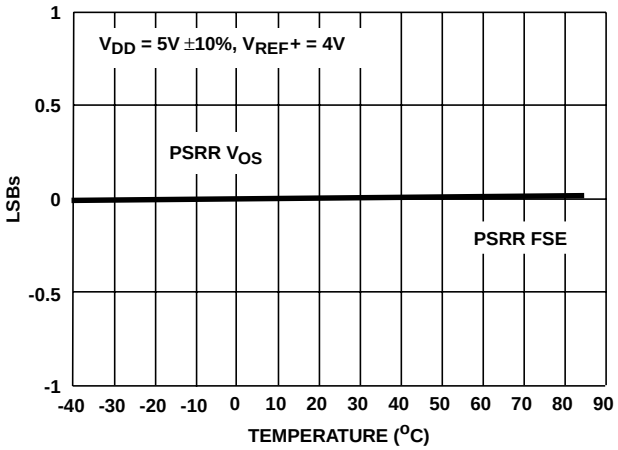


FIGURE 9. POWER SUPPLY REJECTION vs TEMPERATURE

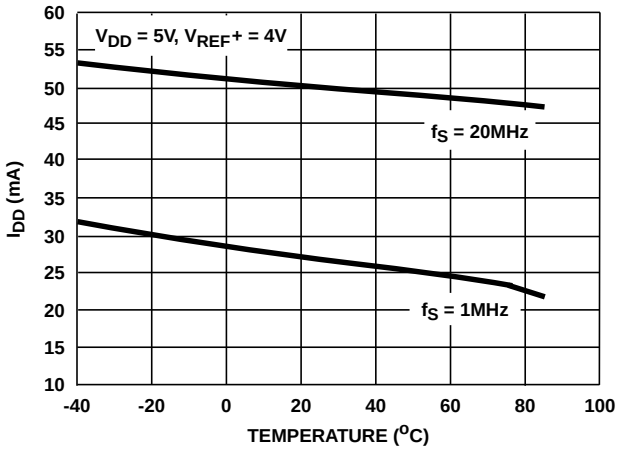


FIGURE 10. SUPPLY CURRENT vs TEMPERATURE

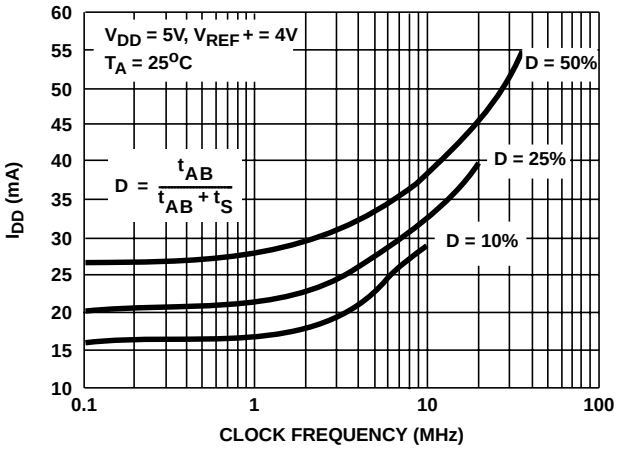


FIGURE 11. SUPPLY CURRENT vs CLOCK AND DUTY CYCLE

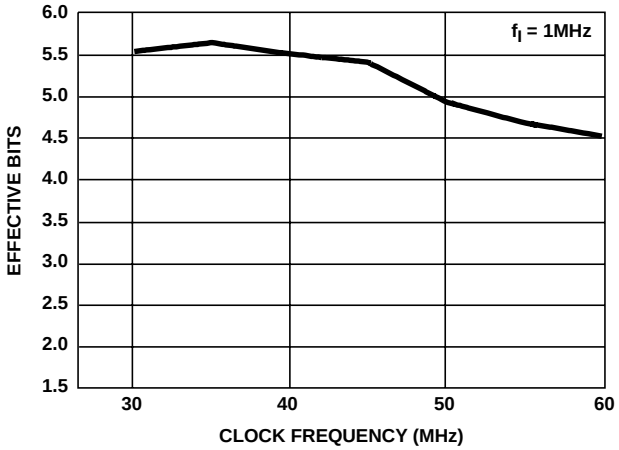


FIGURE 12. EFFECTIVE NUMBER OF BITS vs CLOCK FREQUENCY

TABLE 1. PIN DESCRIPTIONS

PIN #	NAME	DESCRIPTION
1	D5	Bit 6, Output (MSB).
2	OVF	Overflow, Output.
3	V_{SS}	Digital Ground.
4	NC	No Connection.
5	CE2	Three-State Output Enable Input, Active High (See Table 2).
6	$\overline{CE1}$	Three-State Output Enable Input, Active Low (See Table 2).
7	CLK	Clock Input.
8	PHASE	Sample Clock Phase Control Input. When Phase is Low, Sample Unknown (ϕ1) Occurs When the Clock is Low and Auto Balance (ϕ2) Occurs When the Clock is High (See Text).
9	$V_{REF}+$	Reference Voltage Positive Input.
10	$V_{REF}-$	Reference Voltage Negative Input.
11	V_{IN}	Analog Signal Input.
12	V_{DD}	Power Supply, +5V.
13	D0	Bit 1, Output (LSB).
14	D1	Bit 2, Output.
15	D2	Bit 3, Output.
16	$^1/_2$ R2	Reference Ladder Midpoint.
17	D3	Bit 4, Output.
18	D4	Bit 5, Output.

TABLE 2. CHIP ENABLE TRUTH TABLE

$\overline{CE1}$	CE2	D0 - D5	OVF
0	1	Valid	Valid
1	1	Three-State	Valid
X	0	Three-State	Three-State

X = Don't Care

Theory of Operation

The HI-5701 is a 6-bit analog-to-digital converter based on a parallel CMOS "flash" architecture. This flash technique is an extremely fast method of A/D conversion because all bit decisions are made simultaneously. In all, 64 comparators are used in the HI-5701; 63 comparators to encode the output word, plus an additional comparator to detect an overflow condition.

The CMOS HI-5701 works by alternately switching between a "Sample" mode and an "Auto Balance" mode. Splitting up the comparison process in this CMOS technique offers a number of significant advantages. The offset voltage of each CMOS comparator is dynamically canceled with each conversion cycle such that offset voltage drift is virtually eliminated during operation. The block diagram and timing diagram illustrate how the HI-5701 CMOS flash converter operates.

The input clock which controls the operation of the HI-5701 is first split into a non-inverting ϕ1 clock and an inverting ϕ2 clock. These two clocks, in turn, synchronize all internal timing of analog switches and control logic within the converter.

In the "Auto Balance" mode (ϕ1), all ϕ1 switches close and ϕ2 switches open. The output of each comparator is momentarily tied to its own input, self-biasing the comparator midway between V_{SS} and V_{DD} and presenting a low impedance to a small input capacitor. Each capacitor, in turn, is connected to a reference voltage tap from the resistor ladder. The Auto Balance mode quickly precharges all 64 input capacitors between the self-bias voltage and each respective tap voltage.

In the "Sample" mode (ϕ2), all ϕ1 switches open and ϕ2 switches close. This places each comparator in a sensitive high gain amplifier configuration. In this open loop state, the input impedance is very high and any small voltage shift at the input will drive the output either high or low. The ϕ2 state also switches each input capacitor from its reference tap to the input signal. This instantly transfers any voltage difference between the reference tap and input voltage to the comparator input. All 64 comparators are thus driven simultaneously to a defined logic state. For example, if the input voltage is at mid-scale, capacitors precharged near zero during ϕ1 will push comparator inputs higher than the self bias voltage at ϕ2; capacitors precharged near the reference voltage push the respective comparator inputs lower than the bias point. In general, all capacitors precharged by taps above the input voltage force a "low" voltage at comparator inputs; those precharged below the input voltage force "high" inputs at the comparators.

During the next ϕ1 state, comparator output data is latched into the encoder logic block and the first stage of encoding takes place. The following ϕ2 state completes the encoding process. The 6 data bits (plus overflow bit) are latched into the output flip-flops at the next falling clock edge. The Overflow bit is set if the input voltage exceeds $V_{REF}+ - {}^1/_2$ LSB. The output bus may be either enabled or disabled according to the state of $\overline{CE1}$ and CE2 (See Table 2). When disabled, output bits assume a high impedance state.

As shown in the timing diagram, the digital output word becomes valid after the second ϕ1 state. There is thus a one and a half cycle pipeline delay between input sample and digital output. "Data Output Delay" time indicates the slight time delay for data to become valid at the end of the ϕ1 state. Refer to the Glossary of Terms for other definitions.

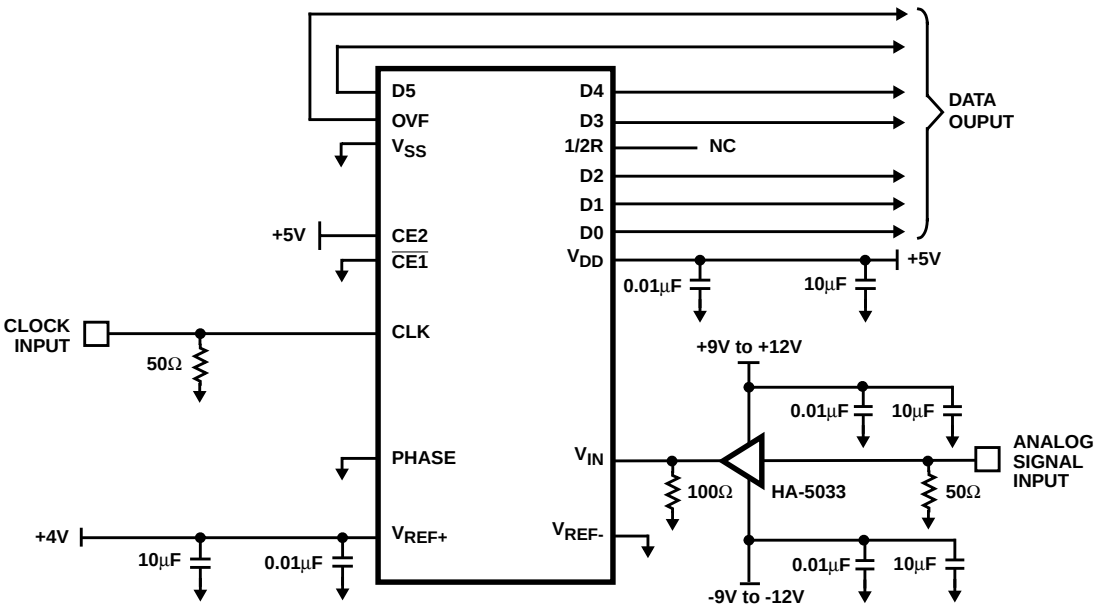


FIGURE 13. TEST CIRCUIT

Application Information

Voltage Reference

The reference voltage is applied across the resistor ladder at the input of the converter, between $V_{REF}+$ and $V_{REF}-$. In most applications, $V_{REF}-$ is simply tied to analog ground such that the reference source drives $V_{REF}+$. The reference must be capable of supplying enough current to drive the minimum ladder resistance of 235Ω over temperature.

The HI-5701 is specified for a reference voltage of 4.0V, but will operate with voltages as high as the V_{DD} supply. In the case of 4.0V reference operation, the converter encodes the analog input into a binary output in LSB increments of $(V_{REF}+ - V_{REF}-)/64$, or 62.5mV. Reducing the reference voltage reduces the LSB size proportionately and thus increases linearity errors. The minimum practical reference voltage is about 2V. Because the reference voltage terminals are subjected to internal transient currents during conversion, it is important to drive the reference pins from a low impedance source and to decouple thoroughly. Again, ceramic and tantalum (0.01μF and 10μF) capacitors near the package pin are recommended. It is not necessary to decouple the $^1/_2$R tap point pin for most applications.

It is possible to elevate $V_{REF}-$ from ground if necessary. In this case, the $V_{REF}-$ pin must be driven from a low impedance reference capable of sinking the current through the resistor ladder. Careful decoupling is again recommended.

Digital Control and Interface

The HI-5701 provides a standard high speed interface to external CMOS and TTL logic families. Four digital inputs are provided to control the function of the converter. The clock and phase inputs control the sample and auto balance modes. The digital outputs change state on the clock phase which begins the sample mode. Two chip enable inputs control the three-state outputs of output bits D0 through D5 and the Overflow OVF bit. As indicated in Table 2, all output bits are high impedance when CE2 is low, and output bits D0 through D5 are independently controlled by $\overline{CE1}$.

Although the Digital Outputs are capable of handling typical data bus loading, the bus capacitance charge/discharge currents will produce supply and local ground disturbances. Therefore, an external bus driver is recommended.

Clock

The clock should be properly terminated to digital ground near the clock input pin. Clock frequency defines the conversion frequency and controls the converter as described in the “Theory of Operation” section. The Auto Balance ϕ1 half cycle of the clock may be reduced to 16ns; the Sample ϕ2 half cycle may be varied from a minimum of 16ns to a maximum of 8μs.

TABLE 3. PHASE CONTROL

CLOCK	PHASE	INTERNAL GENERATION
0	0	Sample Unknown (ϕ2)
0	1	Auto Balance (ϕ1)
1	0	Auto Balance (ϕ1)
1	1	Sample Unknown (ϕ2)

Gain and Offset Adjustment

In applications where accuracy is of utmost importance, three adjustments can be made; i.e., offset, gain, and

midpoint trim. In general, offset and gain correction can be done in the preamp circuitry.

Offset Adjustment

The preferred offset correction method is to introduce a DC component to V_{IN} of the converter. An alternate method is to adjust the V_{REF}- input to produce the desired offset adjustment. The theoretical input voltage to produce the first transition is $^1/_2$ LSB.

V_{IN} (0 to 1 transition) = $^1/_2$ LSB = $^1/_2(V_{REF}/64) = V_{REF}/128$.

Gain Adjustment

In general, full scale error correction can be done in the preamp circuitry by adjusting the gain of the op amp. An alternate method is to adjust the V_{REF}+ input voltage. This adjustment is performed by setting V_{IN} to the 63 to overflow transition. The theoretical input voltage to produce the transition is $^1/_2$ LSB less than V_{REF}+ and is calculated as follows:

V_{IN} (63 to 64 transition) = $V_{REF} - (V_{REF}/128)$
$= V_{REF}(127/128)$.

To perform the gain trim, first do the offset trim and then apply the required V_{IN} for the 63 to overflow transition. Now adjust V_{REF}+ until that transition occurs on the outputs.

Midpoint Trim

The reference center ($^1/_2$R) is available to the user as the midpoint of the resistor ladder. The $^1/_2$R point can be used to improve linearity or create unique transfer functions. The offset and gain trims should be done prior to adjusting the midpoint. The theoretical transition from count 31 to 32 occurs at 31.5 LSBs. That voltage is calculated as follows:

V_{IN} (31 to 32 transition) = $31.5(V_{REF}/64) = V_{REF}(63/128)$.

An adjustable voltage follower can be used to drive the $^1/_2$R pin. Set V_{IN} to the 31 to 32 transition voltage, then adjust the voltage follower until the transition occurs on the output bits.

Signal Source

A current pulse is present at the analog input (V_{IN}) at the beginning of every sample and auto balance period. The transient current is due to comparator charging and switch feed through in the capacitor array. It varies with the amplitude of the analog input and the sampling rate.

The signal source must be capable of recovering from the transient prior to the end of the sample period to ensure a valid signal for conversion. Suitable broad band amplifiers or buffers which exhibit low output impedance and high output drive include the HFA-0005, HA-5004, HA-5002, and HA-5033.

The signal source may drive above or below the power supply rails, but should not exceed 0.5V beyond the rails or damage may occur. Input voltages of -0.5V to +$^1/_2$ LSB are converted to all zeros; input voltages of V_{REF}+ - $^1/_2$ LSB to V_{DD} + 0.5 are converted to all ones with the Overflow bit set.

Power Supply

The HI-5701 operates nominally from a 5V supply, but will function from 3V to 6V. The supply should be well regulated and “clean” of significant noise, especially high frequency noise. It is recommended that power supply decoupling capacitors be placed as close to the supply pin as possible. A combination of 0.01µF ceramic and 10µF tantalum capacitors is recommended for this purpose as shown in the test circuit Figure 13.

Reducing Power Consumption

Power dissipation in the HI-5701 is related to clock frequency and clock duty cycle. For a fixed 50% clock duty cycle, power may be reduced by lowering the clock frequency. For a given conversion frequency, power may be reduced by shortening the Auto Balance ϕ1 portion of the clock duty cycle.

TABLE 4. OUTPUT CODE TABLE

CODE DESCRIPTION	INPUT VOLTAGE† V_{REF}+ = 4V V_{REF}- = 0V (V)	DECIMAL COUNT	BINARY OUTPUT CODE						
				MSB					LSB
			OVF	D5	D4	D3	D2	D1	D0
Overflow (OVF)	4.000	127	1	1	1	1	1	1	1
Full Scale (FS)	3.9063	63	0	1	1	1	1	1	1
FS - 1 LSB	3.8438 • •	62	0	1	1	1 • • •	1	1	0
$^3/_4$ FS	2.9688 • • •	48	0	1	1	0 • • •	0	0	0

TABLE 4. OUTPUT CODE TABLE (Continued)

CODE DESCRIPTION	INPUT VOLTAGE† $V_{REF}+ = 4V$ $V_{REF}- = 0V$ (V)	DECIMAL COUNT	BINARY OUTPUT CODE						
				MSB					LSB
			OVF	D5	D4	D3	D2	D1	D0
$^1/_2$ FS	1.9688 • • •	32	0	1	0	0 • • •	0	0	0
$^1/_4$ FS	0.9688 • • •	16	0	0	1	0 • • •	0	0	0
1 LSB	0.0313	1	0	0	0	0	0	0	1
Zero	0	0	0	0	0	0	0	0	0

† The voltages listed above represent the ideal transition of each output code shown as a function of the reference voltage.

Glossary of Terms

Aperture Delay - is The time delay between the external sample command (the rising edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter, t_{AJ} - This is the RMS variation in the aperture delay due to variation of internal ϕ1 and ϕ2 clock path delays and variation between the individual comparator switching times.

Differential Linearity Error, DNL - The differential linearity error is the difference in LSBs between the spacing of the measured midpoint of adjacent codes and the spacing of ideal midpoints of adjacent codes. The ideal spacing of each midpoint is 1 LSB. The range of values possible is from -1 LSB (which implies a missing code) to greater than +1 LSB.

Full Power Input Bandwidth - Full power bandwidth is the frequency at which the amplitude of the fundamental of the digital output word has decreased 3dB below the amplitude of an input sine wave. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The bandwidth given is measured at the specified sampling frequency.

Full Scale Error, FSE - is The difference between the actual input voltage of the 63 to 64 code transition and the ideal value of $V_{REF}+ - 1.5$ LSB. This error is expressed in LSBs.

Integral Linearity Error, INL - The integral linearity error is the difference in LSBs between the measured code centers and the ideal code centers. The ideal code centers are calculated using a best fit line through the converter's transfer function.

LSB - Least Significant Bit = $(V_{REF}+ - V_{REF}-)/64$. All HI-5701 specifications are given for a 62.5mV LSB size $V_{REF}+ = 4V$, $V_{REF}- = 0V$.

Offset Error, V_{OS} - Offset error is the difference between the actual input voltage of the 0 to 1 code transition and the ideal value of $V_{REF}- + 0.5$ LSB. V_{OS} error is expressed in LSBs.

Power Supply Rejection Ratio, PSRR - Is expressed in LSBs and is the maximum shift in code transition points due to a power supply voltage shift. This is measured at the 0 to 1 code transition point and the 62 to 63 code transition point with a power supply voltage shift from the nominal value of 5.0V.

Signal to Noise Ratio, SNR - SNR is the ratio in dB of the RMS signal to RMS noise at specified input and sampling frequencies.

Signal to Noise and Distortion Ratio, SINAD - Is the ratio in dB of the RMS signal to the RMS sum of the noise and harmonic distortion at specified input and sampling frequencies.

Total Harmonic Distortion, THD - Is the ratio in dBc of the RMS sum of the first five harmonic components to the RMS signal for a specified input and sampling frequency

Die Characteristics

DIE DIMENSIONS:

86.6 mils x 130.7 mils x 19 mils ±1 mil

METALLIZATION:

Type: SiAl
Thickness: 11kÅ ±1kÅ

PASSIVATION:

Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

$<2.0 \times 10^5$ A/cm^2

TRANSISTOR COUNT:

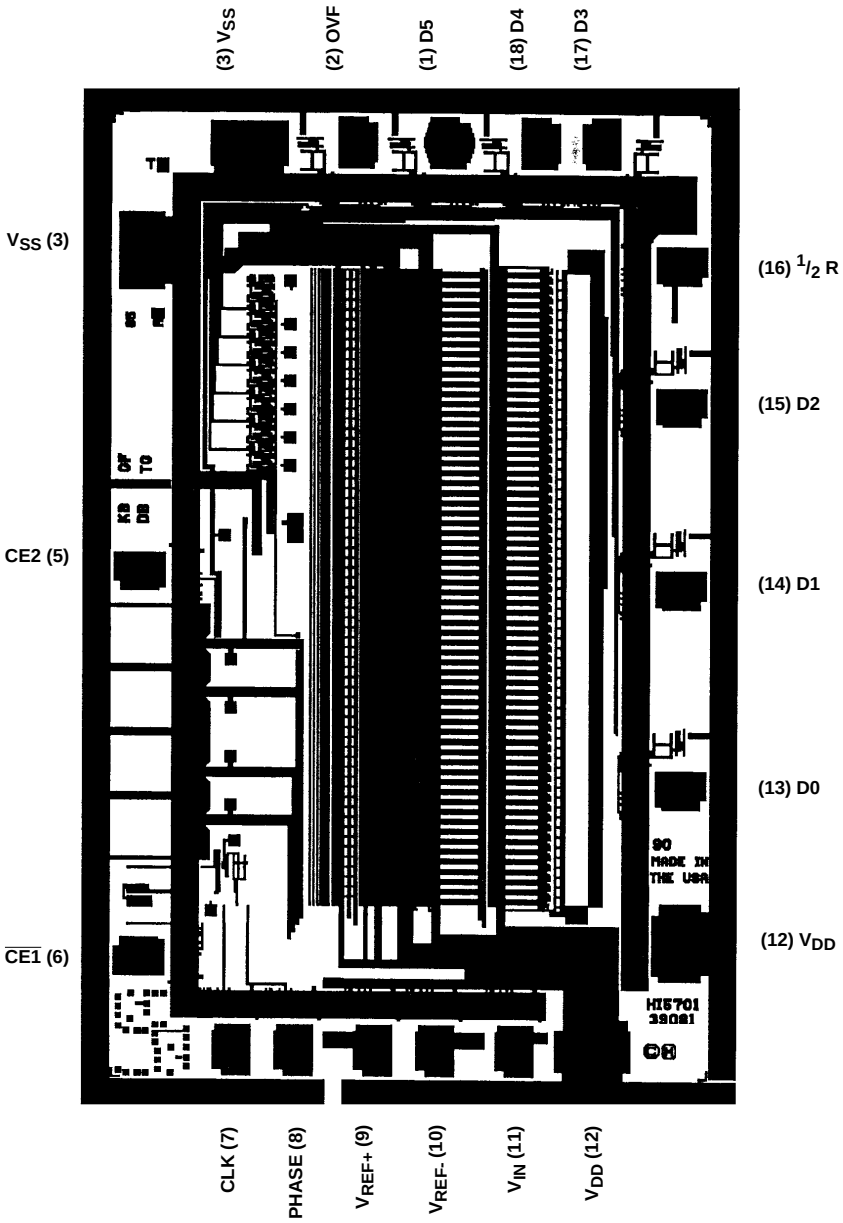
4000

SUBSTRATE POTENTIAL (POWERED UP):

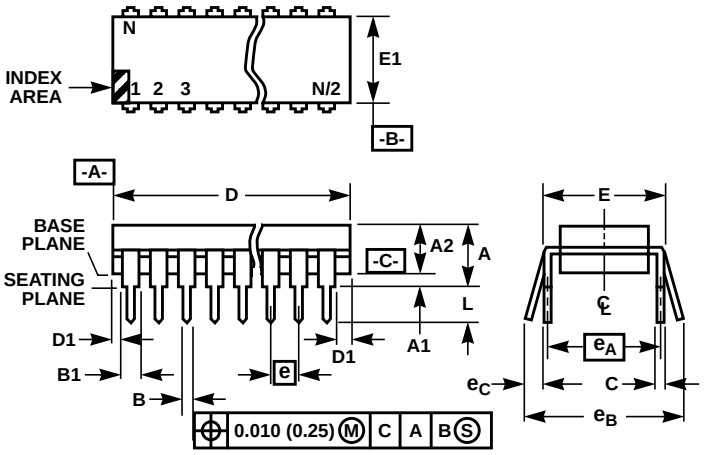
V+

Metallization Mask Layout

HI-5701



Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E18.3 (JEDEC MS-001-BC ISSUE D)
18 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.845	0.880	21.47	22.35	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	18		18		9

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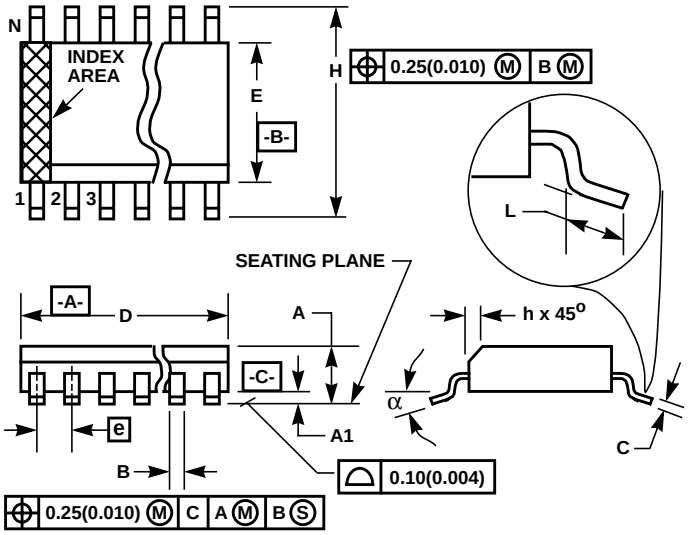
Small Outline Plastic Packages (SOIC)



M18.3 (JEDEC MS-013-AB ISSUE C)
18 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4469	0.4625	11.35	11.75	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	18		18		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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