

## 2 K × 8 GENERAL PURPOSE CMOS SRAM

### FEATURES

- **ACCESS TIME**
  - COMMERCIAL : 120 NS (MAX)
  - INDUSTRIAL : 120 NS (MAX)
  - MILITARY : 120 NS (MAX)
- **VERY LOW POWER CONSUMPTION**
  - ACTIVE : 240 mW (TYP)
  - STANDBY : 2.0 μW (TYP)
  - DATA RETENTION : 4 μW (TYP)
- **600 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **SINGLE 5 VOLT SUPPLY**
- **EQUAL CYCLE AND ACCESS TIME**
- **NO CLOCK AND STROBES REQUIRED**
- **GATED INPUTS**
- **WIDE TEMPERATURE RANGE : - 55 TO + 125°C**

### INTRODUCTION

The HM 6116 is a very low power CMOS static RAM organized as 2048 × 8 bits. It is manufactured using the MHS high performance CMOS technology.

120 ns access time for commercial temperature range is available with a maximum power consumption of only 385 mW.

The HM 6116 features fully static operation requiring no external clocks or timing strobes. Thanks to the special input buffer "gated inputs", the circuit remains in stand by mode when the  $\overline{CS}$  goes to an intermediate level

(VIH). Easy memory expansion is provided by an active low chip select ( $\overline{CS}$ ), an active low output enable ( $\overline{OE}$ ) and three state drivers.

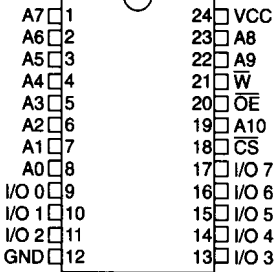
The HM 6116 are TTL compatible and operate from single 5 V supply thus simplifying system design.

The HM 6116 is 100 % processed following the test methods of MIL STD 883C and/or ESA/SCC 9000, making it ideally suitable for military/space applications that demand superior levels of performance and reliability.

# INTERFACE

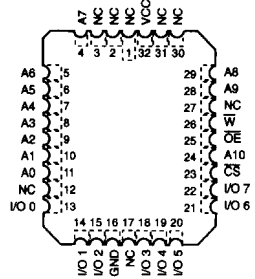
## PIN CONFIGURATION

Plastic 600 mils, 24 pins, DIL.  
Ceramic 600 mils, 24 pins, DIL.



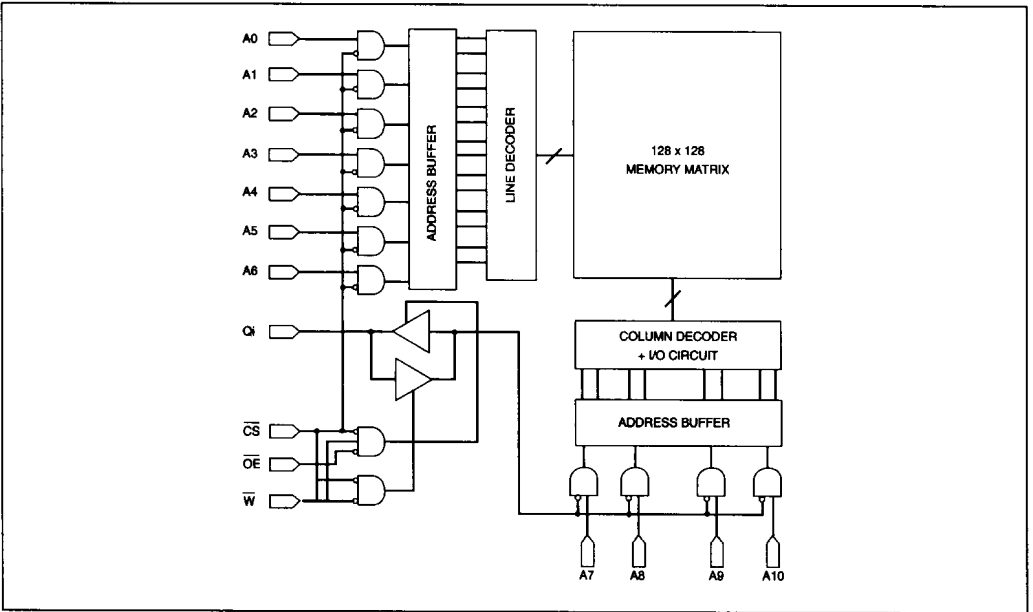
Pinout DIL 24 pins (top view)

LCC, 32 pins.



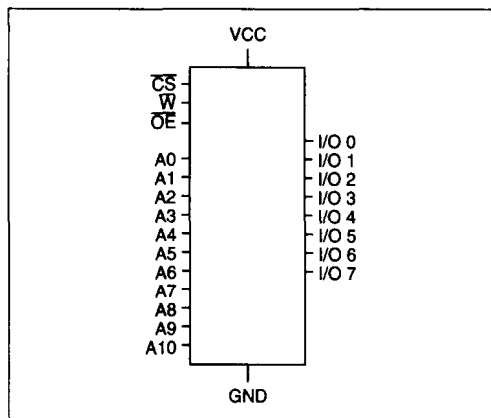
Pinout LCC 32 pins (top view)

## BLOCK DIAGRAM



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## LOGIC SYMBOL



## PIN NAMES

A0-A10 : Address inputs	$\overline{\text{CS}}$ : Chip Select
I/O0-I/O7 : Input/Output	$\overline{\text{OE}}$ : Output enable
VCC : Power	$\overline{\text{W}}$ : Write Enable
GND : Ground	

## TRUTH TABLE

CS	$\overline{\text{OE}}$	W	DATA-IN	DATA-OUT	MODE
H	X	X	Z	Z	Deselect
L	L	H	Z	Valid	Read
L	H	L	Valid	Z	Write
L	L	L	Valid	Z	Write

L = low, H = high, X = H or L, Z = high impedance.

## ELECTRICAL CHARACTERISTICS

## ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : - 0.3 V to + 7.0 V  
 Input or Output voltage applied : (Gnd - 0.3 V) to (Vcc + 0.3 V)

Storage temperature : - 65°C to + 150°C

## OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(-2)	$V_{cc} \pm 10\%$	- 55°C to + 125°C
Industrial	(-9)	$V_{cc} \pm 10\%$	- 40°C to + 85°C
Commercial	(-5)	$V_{cc} \pm 10\%$	0°C to 70°C

## RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
VCC	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL (1)	Input low voltage	- 0.3	0.0	0.8	V
VIH	Input high voltage	2.2	-	$V_{cc} + 0.3\text{ V}$	V

Note : 1. VIL min = - 0.3 V or - 1.0 V pulse width 50 ns.

## CAPACITANCE

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin (2)	Input capacitance	-	-	8	pF
Cout (2)	Output capacitance	-	-	10	pF

Note : 2. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not 100 % tested.

**DC PARAMETERS**

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(3)	Input leakage current	- 5.0	-	5.0	μA
IOZ	(3)	Output leakage current	- 5.0	-	5.0	μA
VOL	(4)	Output low voltage	-	-	0.4	V
VOH	(4)	Output high voltage	2.4	-	-	V

Notes : 3. Gnd < Vin < Vcc, Gnd < Vout < Vcc output disabled specified to ± 10 μA for the HM61162.  
 4. Vcc min, IOL = 3.2 mA, IOH = - 1.0 mA.

**CONSUMPTION FOR COMMERCIAL (- 5) SPECIFICATION**

SYMBOL		PARAMETER	6116 -5	6116 L-5	6116 B-5	UNIT	VALUE
ICCSB	(5)	Standby supply current	3.0	2.0	2.0	mA	max
ICCSB1	(6)	Standby supply current	2000.0	100.0	1.0	μA	max
ICC	(7)	Operating supply current	70.0	70.0	70.0	mA	max
ICCOP	(8)	Operating supply current	70.0	70.0	70.0	mA	max

**CONSUMPTION FOR INDUSTRIAL (- 9) SPECIFICATION**

SYMBOL		PARAMETER	6116 -9	6116 L-9	6116 B-9	UNIT	VALUE
ICCSB	(5)	Standby supply current	4.5	4.0	4.0	mA	max
ICCSB1	(6)	Standby supply current	2000.0	500.0	5.0	μA	max
ICC	(7)	Operating supply current	80.0	80.0	80.0	mA	max
ICCOP	(8)	Operating supply current	80.0	80.0	80.0	mA	max

**CONSUMPTION FOR MILITARY (- 2) SPECIFICATION**

SYMBOL		PARAMETER	6116 -2	6116 L-2	UNIT	VALUE
ICCSB	(5)	Standby supply current	5.0	4.5	mA	max
ICCSB1	(6)	Standby supply current	3000.0	1500.0	μA	max
ICC	(7)	Operating supply current	85.0	85.0	mA	max
ICCOP	(8)	Operating supply current	85.0	85.0	mA	max

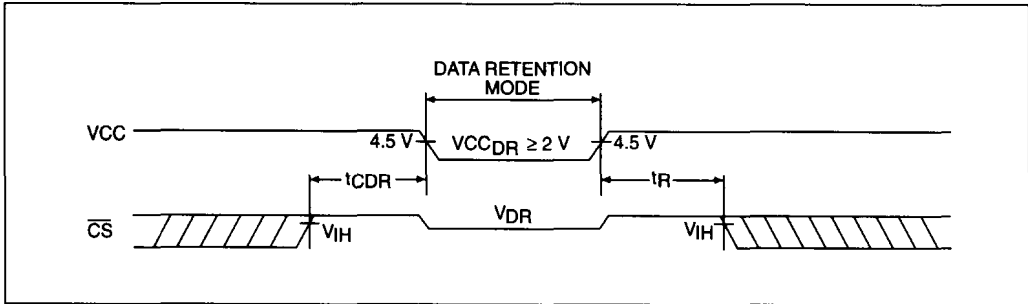
Notes : 5. CS ≤ VIH.  
 6. CS ≤ Vcc - 0.3 V, Iout = 0 mA.  
 7. CS ≤ VIL, Iout = 0 mA, Vin = Gnd/Vcc.  
 8. Vcc max, Iout = 0 mA, f = 1 MHz and 5 mA/MHz, Vin = Gnd/Vcc.

**DATA RETENTION MODE**

MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip select ( $\overline{CS}$ ) must be held high during data retention; within  $V_{CC}$  to  $V_{CC} - 0.2$  V.
2. Output Enable ( $\overline{OE}$ ) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3.  $\overline{CS}$  and  $\overline{OE}$  must be kept between  $V_{CC} + 0.3$  V and 70 % of  $V_{CC}$  during the power up and power down transitions.

**TIMING**



**DATA RETENTION CHARACTERISTICS**

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL (9)	MAXIMUM	UNIT
VCCDR	Vcc for data retention	2.0	-	-	V
TCDR	Chip deselect to data retention time	0.0	-	-	ns
TR	Operation recovery time	TAVAV (10)	-	-	-
ICCDR1 (11)	Data retention current @2.0 V : HM-6116B-5 HM-6116B-9 HM-6116L-5 HM-6116L-9 HM-6116L-2	- - - - -	0.1 0.1 2.0 2.0 2.0	1.0 5.0 30.0 200.0 600.0	$\mu$ A $\mu$ A $\mu$ A $\mu$ A $\mu$ A
ICCDR2 (11)	Data retention current @3.0 V : HM-6116B-5 HM-6116B-9 HM-6116L-5 HM-6116L-9 HM-6116L-2	- - - - -	0.3 0.3 3.0 3.0 3.0	1.0 7.0 45.0 300.0 900.0	$\mu$ A $\mu$ A $\mu$ A $\mu$ A $\mu$ A

Notes : 9. TA = 25°C.  
 10. TAVAV = Read cycle time.  
 11. CS = Vcc, Vin = Gnd/Vcc, this parameter is only tested to Vcc = 2 V.

**AC PARAMETERS**

**AC CONDITIONS :**

Input pulse levels : Gnd to 3.0 V  
 Input rise : 10 ns

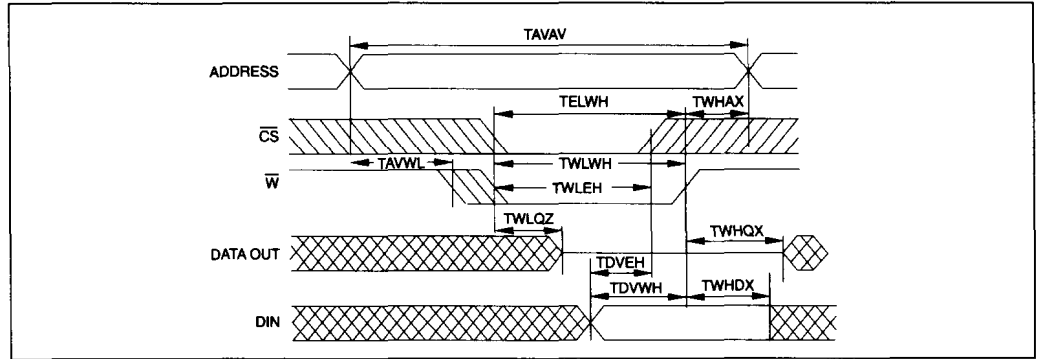
Input timing reference levels : 1.5 V  
 Output load : 1 TTL gate + 100 pF

**WRITE CYCLE : COMMERCIAL (- 5), INDUSTRIAL (- 9) AND MILITARY (- 2) SPECIFICATION**

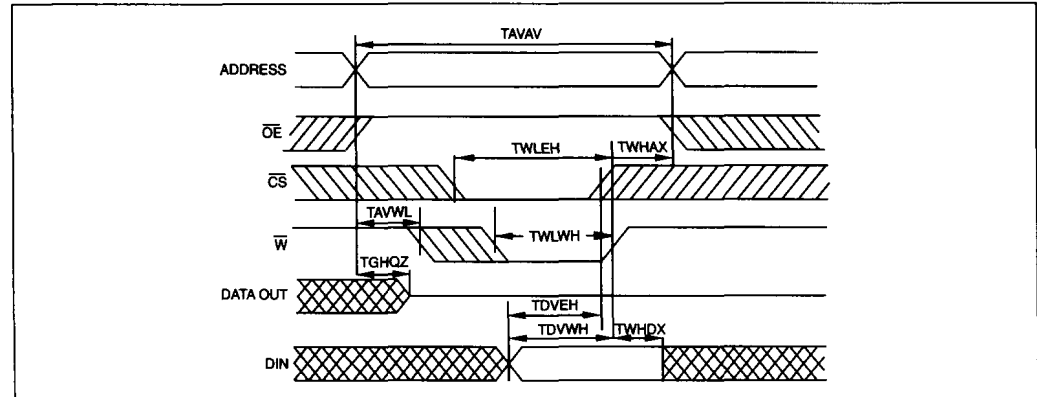
SYMBOL	PARAMETER	6116	
		(B)(L)	-5/-9/-2
TAVAV	Write cycle time	120	ns min
TAVWL	Address set-up time	0	ns min
TAVWH	Address valid to end of write	105	ns min
TDVWH	Data set-up time	35	ns min
TELWH	CS low to write end	70	ns min
TWLQZ (12)	Write low to high Z	50	ns max
TWLWH	Write pulse width	70	ns min
TWHAX	Address hold to end of write	10	ns min
TWHDX	Data hold time	10	ns min
TWHQX (12)	Write high to low Z	5	ns min

Note : 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

**WRITE CYCLE 1**



**WRITE CYCLE 2**

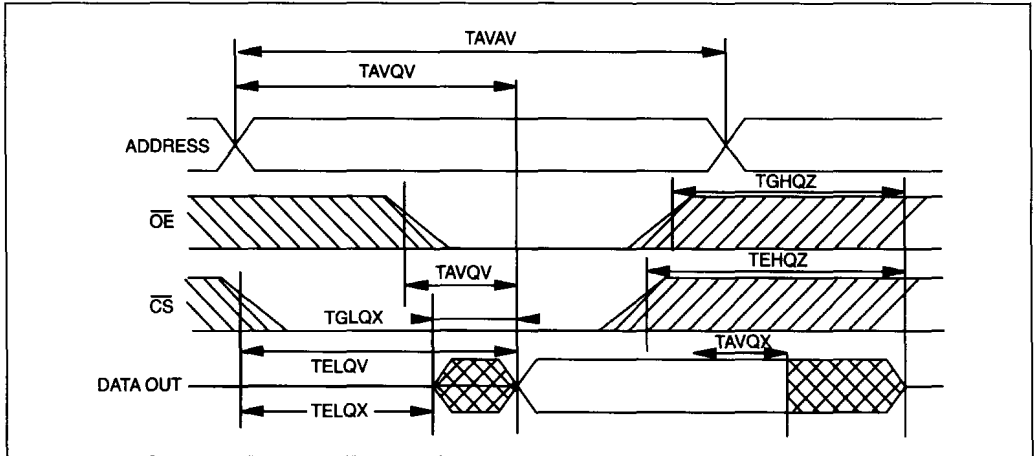


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READ CYCLE : COMMERCIAL (- 5), INDUSTRIAL (- 9) AND MILITARY (- 2) SPECIFICATION

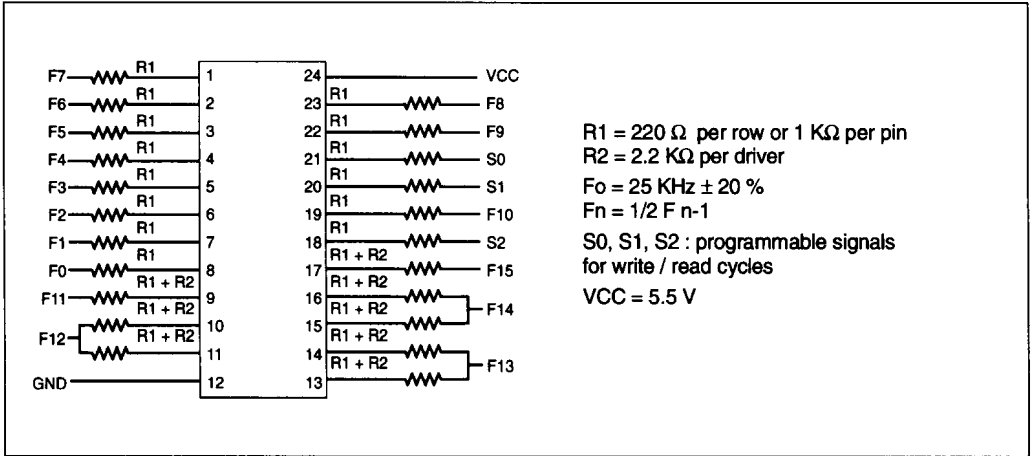
SYMBOL	PARAMETER	6116 (B)(L) -5/ -9/ -2	UNIT	VALUE
TAVAV	Write cycle time	120	ns	min
TAVQV	Address access time	120	ns	max
TAVQX	Address valid to low Z	10	ns	min
TELQV	Chip-select access time	120	ns	max
TELQX	CS low to low Z	10	ns	min
TEHQZ	CS high to high Z	40	ns	max
TGLQV	Output Enable access time	80	ns	max
TGLQX	OE low to low Z	10	ns	min
TGHQZ	OE high to high Z	40	ns	max

READ CYCLE



Note :  $\bar{W}$  high for a read cycle.

**BURN-IN SCHEMATICS**



**ORDERING INFORMATION**

