

---

# HM514170D, HM514270D Series HM51S4170D, HM51S4270D Series

262,144-word × 16-bit Dynamic RAM

# HITACHI

ADE-203-672 (Z)

Preliminary

Rev. 0.0

Oct. 18, 1996

---

## Description

The Hitachi HM51(S)4170D, HM51(S)4270D Series are CMOS dynamic RAM organized as 262,144-word × 16-bit. HM51(S)4170D, HM51(S)4270D Series have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM51(S)4170D, HM51(S)4270D Series offer fast page mode as a high speed access mode. They have the package variations of standard 400-mil 40-pin plastic SOJ and standard 400-mil 44-pin plastic TSOPII. Internal refresh timer enables HM51S4170D, HM51S4270D Series self refresh operation.

## Features

- Single 5 V supply: 5 V ± 10%
- Access time: 60 ns/70 ns/80 ns (max)
- Low power dissipation
  - Active mode: 825 mW/660 mW/578 mW (max) (HM51(S)4170D Series)  
825 mW/770 mW/688 mW (max) (HM51(S)4270D Series)
  - Standby mode: 11 mW (max)  
1.1 mW (max) (L-version)
- Fast page mode capability
- Refresh cycles
  - 1024 refresh cycles: 16 ms (HM51(S)4170D Series)  
128 ms (L-version) (HM51(S)4170DL Series)
  - 512 refresh cycles: 8 ms (HM51(S)4270D Series)  
128 ms (L-version) (HM51(S)4270DL Series)
- 2 variations of refresh
  - $\overline{\text{RAS}}$ -only refresh
  - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

## HM51(S)4170D Series, HM51(S)4270D Series

- 2  $\overline{WE}$ -byte control
- Self refresh operation (HM51S4170D, HM51S4270D)
- Battery backup operation (L-version)

### Ordering Information

Type No.	Access time	Package
HM514170DJ-6	60 ns	400-mil 40-pin plastic SOJ (CP-40D)
HM514170DJ-7	70 ns	
HM514170DJ-8	80 ns	
HM514170DLJ-6	60 ns	
HM514170DLJ-7	70 ns	
HM514170DLJ-8	80 ns	
HM514270DJ-6	60 ns	
HM514270DJ-7	70 ns	
HM514270DJ-8	80 ns	
HM514270DLJ-6	60 ns	
HM514270DLJ-7	70 ns	
HM514270DLJ-8	80 ns	
HM51S4170DJ-6	60 ns	
HM51S4170DJ-7	70 ns	
HM51S4170DJ-8	80 ns	
HM51S4170DLJ-6	60 ns	
HM51S4170DLJ-7	70 ns	
HM51S4170DLJ-8	80 ns	
HM51S4270DJ-6	60 ns	
HM51S4270DJ-7	70 ns	
HM51S4270DJ-8	80 ns	
HM51S4270DLJ-6	60 ns	
HM51S4270DLJ-7	70 ns	
HM51S4270DLJ-8	80 ns	
HM514170DTT-6	60 ns	400 mil 44-pin plastic TSOP II (TTP-44/40DB)
HM514170DTT-7	70 ns	
HM514170DTT-8	80 ns	
HM514170DLTT-6	60 ns	
HM514170DLTT-7	70 ns	
HM514170DLTT-8	80 ns	
HM514270DTT-6	60 ns	
HM514270DTT-7	70 ns	
HM514270DTT-8	80 ns	
HM514270DLTT-6	60 ns	
HM514270DLTT-7	70 ns	
HM514270DLTT-8	80 ns	

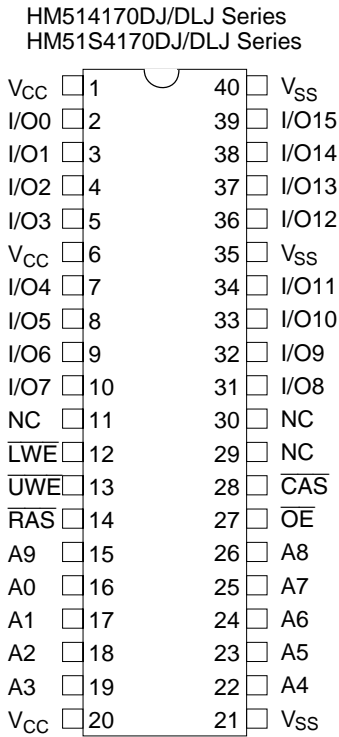
**Ordering Information (cont)**

<b>Type No.</b>	<b>Access time</b>	<b>Package</b>
HM51S4170DTT-6	60 ns	400 mil 44-pin plastic TSOP II (TTP-44/40DB)
HM51S4170DTT-7	70 ns	
HM51S4170DTT-8	80 ns	
HM51S4170DLTT-6	60 ns	
HM51S4170DLTT-7	70 ns	
HM51S4170DLTT-8	80 ns	
HM51S4270DTT-6	60 ns	
HM51S4270DTT-7	70 ns	
HM51S4270DTT-8	80 ns	
HM51S4270DLTT-6	60 ns	
HM51S4270DLTT-7	70 ns	
HM51S4270DLTT-8	80 ns	

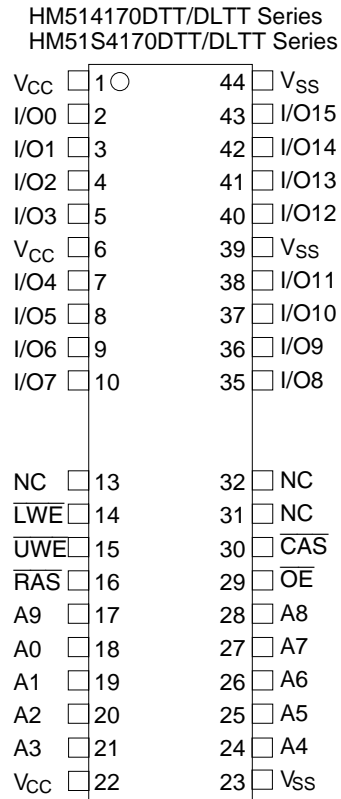
---

# HM51(S)4170D Series, HM51(S)4270D Series

## Pin Arrangement



(Top view)



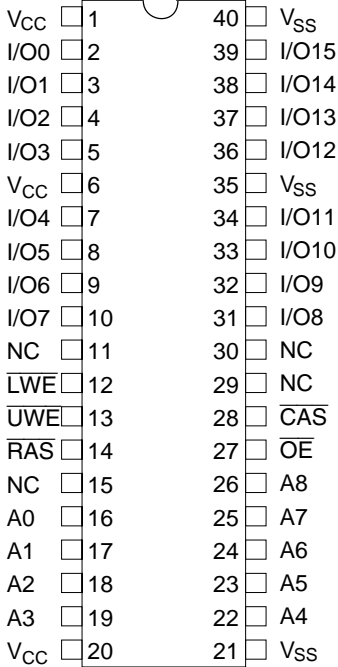
(Top view)

## Pin Description

Pin name	Function
A0 to A9	Address input — Refresh address A0 to A9 — Row address A0 to A9 — Column address A0 to A7
I/O0 to I/O15	Data input/output
RAS	Row address strobe
CAS	Column address strobe
UWE / LWE	Read/write enable
OE	Output enable
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground
NC	No connection

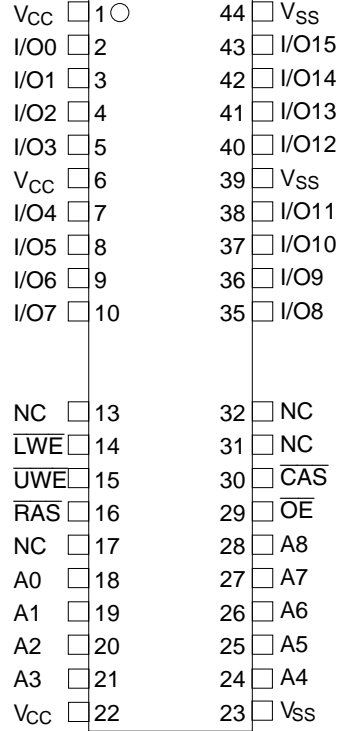
## Pin Arrangement

HM514270DJ/DLJ Series  
HM51S4270DJ/DLJ Series



(Top view)

HM514270DTT/DLTT Series  
HM51S4270DTT/DLTT Series



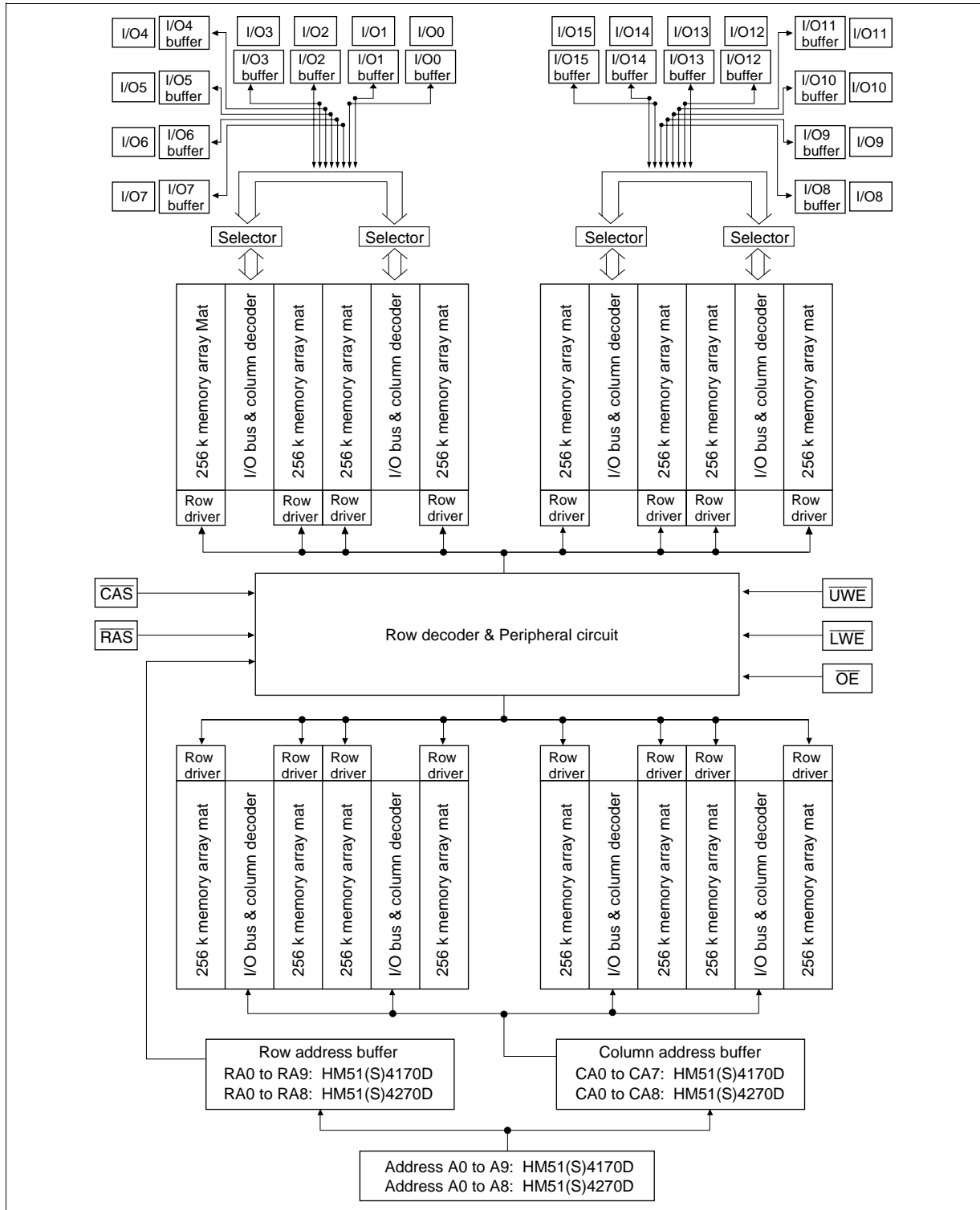
(Top view)

## Pin Description

Pin name	Function
A0 to A8	Address input — Refresh address A0 to A8 — Row address A0 to A8 — Column address A0 to A8
I/O0 to I/O15	Data input/output
RAS	Row address strobe
CAS	Column address strobe
UWE / LWE	Read/write enable
OE	Output enable
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground
NC	No connection

# HM51(S)4170D Series, HM51(S)4270D Series

## Block Diagram



## Operation Mode

The HM51(S)4170D, HM51(S)4270D series has the following 11 operation modes.

1. Read cycle
2. Early write cycle
3. Delayed write cycle
4. Read-modify-write cycle
5.  $\overline{\text{RAS}}$ -only refresh cycle
6.  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycle
7. Self refresh cycle (HM51S4170D, HM51S4270D)
8. Fast page mode read cycle
9. Fast page mode early write cycle
10. Fast page mode delayed write cycle
11. Fast page mode read-modify-write cycle

### Inputs

$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{UWE}}$	$\overline{\text{LWE}}$	Output	Operation
H	H	D	D	Open	Standby
H	L	H	H	Valid	Standby
L	L	H	H	Valid	Read cycle
L	L	L* <sup>2</sup>	L* <sup>2</sup>	Open	Early write cycle
L	L	L* <sup>2</sup>	L* <sup>2</sup>	Undefined	Delayed write cycle
L	L	H to L	H to L	Valid	Read-modify-write cycle
L	H	D	D	Open	$\overline{\text{RAS}}$ -only refresh cycle
H to L	L	D	D	Open	$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle Self refresh cycle
L	H to L	H	H	Valid	Fast page mode read cycle
L	H to L	L* <sup>2</sup>	L* <sup>2</sup>	Open	Fast page mode early write cycle
L	H to L	L* <sup>2</sup>	L* <sup>2</sup>	Undefined	Fast page mode delayed write cycle
L	H to L	H to L	H to L	Valid	Fast page mode read modify-write cycle

Notes: 1. H: High (inactive) L: Low (active) D: H or L

2.  $t_{\text{wcs}} \geq 0$  ns Early write cycle

$t_{\text{wcs}} < 0$  ns Delay write cycle

3. Mode is determined by the OR function of the  $\overline{\text{UWE}}$  and  $\overline{\text{LWE}}$ . (Mode is set by the earliest of  $\overline{\text{UWE}}$  and  $\overline{\text{LWE}}$  active edge and reset by the latest of  $\overline{\text{UWE}}$  and  $\overline{\text{LWE}}$  inactive edge.) However write OPERATION and output High-Z control are done independently by each  $\overline{\text{UWE}}$ ,  $\overline{\text{LWE}}$ .

## HM51(S)4170D Series, HM51(S)4270D Series

### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to $V_{SS}$	$V_T$	-1.0 to +7.0	V
Supply voltage relative to $V_{SS}$	$V_{CC}$	-1.0 to +7.0	V
Short circuit output current	$I_{out}$	50	mA
Power dissipation	$P_T$	1.0	W
Operating temperature range	$T_{opr}$	0 to +70	°C
Storage temperature range	$T_{stg}$	-55 to +125	°C

### Recommended DC Operating Conditions ( $T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	$V_{SS}$	0	0	0	V	2
	$V_{CC}$	4.5	5.0	5.5	V	1, 2
Input high voltage	$V_{IH}$	2.4	—	6.5	V	1
Input low voltage	$V_{IL}$	-1.0	—	0.8	V	1

Notes: 1. All voltage referred to  $V_{SS}$ .

2. The supply voltage with all  $V_{CC}$  pins must be on the same level.

The supply voltage with all  $V_{SS}$  pins must be on the same level.



## DC Characteristics

( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ )\*<sup>5</sup> (HM51(S)4170D Series)

Parameter	Symbol	HM514170D, HM51S4170D						Unit	Test conditions
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
Operating current* <sup>1, *2</sup>	$I_{CC1}$	—	135	—	120	—	105	mA	$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ cycling, $t_{RC} = \text{min}$
Standby current	$I_{CC2}$	—	2	—	2	—	2	mA	TTL interface, $\overline{\text{RAS}}$ , $\overline{\text{CAS}} = V_{IH}$ Dout = High-Z
		—	1	—	1	—	1	mA	CMOS interface $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{UWE}}$ , $\overline{\text{LWE}}$ , $\overline{\text{OE}}$ $\geq V_{CC} - 0.2\text{ V}$ Dout = High-Z
Standby current (L-version)	$I_{CC2}$	—	200	—	200	—	200	$\mu\text{A}$	CMOS interface $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{OE}}$ , $\overline{\text{UWE}}$ , $\overline{\text{LWE}} \geq V_{CC} - 0.2\text{ V}$ Dout = High-Z
$\overline{\text{RAS}}$ -only refresh current* <sup>2</sup>	$I_{CC3}$	—	135	—	120	—	100	mA	$t_{RC} = \text{min}$
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh current* <sup>2</sup>	$I_{CC6}$	—	135	—	120	—	100	mA	$t_{RC} = \text{min}$
Fast page mode current* <sup>1, *3</sup>	$I_{CC7}$	—	150	—	120	—	100	mA	$t_{PC} = \text{min}$
Battery backup current* <sup>4</sup> (Standby with CBR refresh) (L-version)	$I_{CC10}$	—	300	—	300	—	300	$\mu\text{A}$	Standby: CMOS interface Dout = High-Z CBR refresh: $t_{RC} = 125\ \mu\text{s}$ $t_{\text{RAS}} \leq 1\ \mu\text{s}$ , $\overline{\text{CAS}} = V_{IL}$ $\overline{\text{LWE}}$ , $\overline{\text{UWE}}$ , $\overline{\text{OE}} = V_{IH}$
Self-refresh mode current (HM51S4170D)	$I_{CC11}$	—	1	—	1	—	1	mA	CMOS interface $\overline{\text{RAS}}$ , $\overline{\text{CAS}} \leq 0.2\text{ V}$ , Dout = High-Z
Self-refresh mode current (HM51S4170DL)	$I_{CC11}$	—	200	—	200	—	200	$\mu\text{A}$	CMOS interface $\overline{\text{RAS}}$ , $\overline{\text{CAS}} \leq 0.2\text{ V}$ Dout = High-Z
Input leakage current	$I_{LI}$	-10	10	-10	10	-10	10	$\mu\text{A}$	$0\text{ V} \leq V_{in} \leq 6.5\text{ V}$
Output leakage current	$I_{LO}$	-10	10	-10	10	-10	10	$\mu\text{A}$	$0\text{ V} \leq V_{out} \leq 6.5\text{ V}$ Dout = disable
Output high voltage	$V_{OH}$	2.4	$V_{CC}$	2.4	$V_{CC}$	2.4	$V_{CC}$	V	High Iout = -5.0 mA
Output low voltage	$V_{OL}$	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA

Notes: 1.  $I_{CC}$  depends on output load condition when the device is selected.  $I_{CC}$  max is specified at the output open condition.

2. Address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$ .

3. Address can be changed once or less while  $\overline{\text{CAS}} = V_{IH}$ .

4.  $V_{IH} \geq V_{CC} - 0.2\text{ V}$ ,  $0 \leq V_{IL} \leq 0.2\text{ V}$ , Address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$ .

5. All the  $V_{CC}$  pins shall be supplied with the same voltage. And all the  $V_{SS}$  pins shall be supplied with the same voltage.

# HM51(S)4170D Series, HM51(S)4270D Series

## DC Characteristics

( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ )\*<sup>5</sup> (HM51(S)4270D Series)

Parameter	Symbol	HM514270D, HM51S4270D						Unit	Test conditions
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
Operating current* <sup>1, *2</sup>	$I_{CC1}$	—	150	—	140	—	125	mA	$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ cycling, $t_{RC} = \text{min}$
Standby current	$I_{CC2}$	—	2	—	2	—	2	mA	TTL interface, $\overline{\text{RAS}}$ , $\overline{\text{CAS}} = V_{IH}$ Dout = High-Z
		—	1	—	1	—	1	mA	CMOS interface $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{UWE}}$ , $\overline{\text{LWE}}$ , $\overline{\text{OE}}$ $\geq V_{CC} - 0.2\text{ V}$ Dout = High-Z
Standby current (L-version)	$I_{CC2}$	—	200	—	200	—	200	$\mu\text{A}$	CMOS interface $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{OE}}$ , $\overline{\text{UWE}}$ , $\overline{\text{LWE}} \geq V_{CC} - 0.2\text{ V}$ Dout = High-Z
$\overline{\text{RAS}}$ -only refresh current* <sup>2</sup>	$I_{CC3}$	—	140	—	130	—	110	mA	$t_{RC} = \text{min}$
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh current* <sup>2</sup>	$I_{CC6}$	—	140	—	130	—	110	mA	$t_{RC} = \text{min}$
Fast page mode current* <sup>1, *3</sup>	$I_{CC7}$	—	150	—	130	—	120	mA	$t_{PC} = \text{min}$
Battery backup current* <sup>4</sup> (Standby with CBR refresh) (L-version)	$I_{CC10}$	—	300	—	300	—	300	$\mu\text{A}$	Standby: CMOS interface Dout = High-Z CBR refresh: $t_{RC} = 250\ \mu\text{s}$ $t_{RAS} \leq 1\ \mu\text{s}$ , $\overline{\text{CAS}} = V_{IL}$ $\overline{\text{LWE}}$ , $\overline{\text{UWE}}$ , $\overline{\text{OE}} = V_{IH}$
Self-refresh mode current (HM51S4270D)	$I_{CC11}$	—	1	—	1	—	1	mA	CMOS interface $\overline{\text{RAS}}$ , $\overline{\text{CAS}} \leq 0.2\text{ V}$ , Dout = High-Z
Self-refresh mode current (HM51S4270DL)	$I_{CC11}$	—	200	—	200	—	200	$\mu\text{A}$	CMOS interface $\overline{\text{RAS}}$ , $\overline{\text{CAS}} \leq 0.2\text{ V}$ Dout = High-Z
Input leakage current	$I_{LI}$	-10	10	-10	10	-10	10	$\mu\text{A}$	$0\text{ V} \leq V_{in} \leq 6.5\text{ V}$
Output leakage current	$I_{LO}$	-10	10	-10	10	-10	10	$\mu\text{A}$	$0\text{ V} \leq V_{out} \leq 6.5\text{ V}$ Dout = disable
Output high voltage	$V_{OH}$	2.4	$V_{CC}$	2.4	$V_{CC}$	2.4	$V_{CC}$	V	High Iout = -5.0 mA
Output low voltage	$V_{OL}$	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA

Notes: 1.  $I_{CC}$  depends on output load condition when the device is selected.  $I_{CC}$  max is specified at the output open condition.

2. Address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$ .

3. Address can be changed once or less while  $\overline{\text{CAS}} = V_{IH}$ .

4.  $V_{IH} \geq V_{CC} - 0.2\text{ V}$ ,  $0 \leq V_{IL} \leq 0.2\text{ V}$ , Address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$ .

5. All the  $V_{CC}$  pins shall be supplied with the same voltage. And all the  $V_{SS}$  pins shall be supplied with the same voltage.

**Capacitance** ( $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ )

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	$C_{I1}$	—	5	pF	1
Input capacitance (Clocks)	$C_{I2}$	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.  
2.  $\overline{\text{CAS}} = V_{IH}$  to disable Dout.

**AC Characteristics** ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ )\*<sup>1, \*14, \*15, \*17, \*18</sup>**Test Conditions**

- Input rise and fall time: 5 ns
- Input timing reference levels: 0.8 V, 2.4 V
- Input levels: 0 V, 3 V
- Output load: 2 TTL gate +  $C_L$  (100 pF) (Including scope and jig)

# HM51(S)4170D Series, HM51(S)4270D Series

## Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514170D, HM51S4170D HM514270D, HM51S4270D						Unit	Notes
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	$t_{RC}$	110	—	130	—	150	—	ns	
RAS precharge time	$t_{RP}$	40	—	50	—	60	—	ns	
$\overline{RAS}$ pulse width	$t_{RAS}$	60	10000	70	10000	80	10000	ns	
$\overline{CAS}$ pulse width	$t_{CAS}$	15	10000	20	10000	20	10000	ns	22
Row address setup time	$t_{ASR}$	0	—	0	—	0	—	ns	
Row address hold time	$t_{RAH}$	10	—	10	—	10	—	ns	
Column address setup time	$t_{ASC}$	0	—	0	—	0	—	ns	
Column address hold time	$t_{CAH}$	15	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	$t_{RCD}$	20	45	20	50	20	60	ns	8
$\overline{RAS}$ to column address delay time	$t_{RAD}$	15	30	15	35	15	40	ns	9
$\overline{RAS}$ hold time	$t_{RSH}$	15	—	20	—	20	—	ns	
$\overline{CAS}$ hold time	$t_{CSH}$	60	—	70	—	80	—	ns	
$\overline{CAS}$ to RAS precharge time	$t_{CRP}$	10	—	15	—	15	—	ns	
$\overline{OE}$ to Din delay time	$t_{ODD}$	15	—	20	—	20	—	ns	
$\overline{OE}$ delay time from Din	$t_{DZO}$	0	—	0	—	0	—	ns	
$\overline{CAS}$ setup time from Din	$t_{DZC}$	0	—	0	—	0	—	ns	
Transition time (rise and fall)	$t_T$	3	50	3	50	3	50	ns	7

# HM51(S)4170D Series, HM51(S)4270D Series

## Read Cycle

		HM514170D, HM51S4170D HM514270D, HM51S4270D							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{\text{RAS}}$	$t_{\text{RAC}}$	—	60	—	70	—	80	ns	2, 3
Access time from $\overline{\text{CAS}}$	$t_{\text{CAC}}$	—	15	—	20	—	20	ns	3, 4, 13
Access time from address	$t_{\text{AA}}$	—	30	—	35	—	40	ns	3, 5, 13
Access time from $\overline{\text{OE}}$	$t_{\text{OAC}}$	—	15	—	20	—	20	ns	3, 22
Read command setup time	$t_{\text{RCS}}$	0	—	0	—	0	—	ns	20
Read command hold time to $\overline{\text{CAS}}$	$t_{\text{RCH}}$	0	—	0	—	0	—	ns	16, 19
Read command hold time to $\overline{\text{RAS}}$	$t_{\text{RRH}}$	0	—	0	—	0	—	ns	16, 19
Column address to $\overline{\text{RAS}}$ lead time	$t_{\text{RAL}}$	30	—	35	—	40	—	ns	
Output buffer turn-off time	$t_{\text{OFF1}}$	0	15	0	15	0	15	ns	6
Output buffer turn-off to $\overline{\text{OE}}$	$t_{\text{OFF2}}$	0	15	0	15	0	15	ns	6
$\overline{\text{CAS}}$ to Din delay time	$t_{\text{CDD}}$	15	—	15	—	15	—	ns	

## Write Cycle

		HM514170D, HM51S4170D HM514270D, HM51S4270D							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	$t_{\text{WCS}}$	0	—	0	—	0	—	ns	10, 19
Write command hold time	$t_{\text{WCH}}$	15	—	15	—	15	—	ns	20
Write command pulse width	$t_{\text{WP}}$	10	—	10	—	10	—	ns	21
Write command to $\overline{\text{RAS}}$ lead time	$t_{\text{RWL}}$	15	—	20	—	20	—	ns	21
Write command to $\overline{\text{CAS}}$ lead time	$t_{\text{CWL}}$	15	—	20	—	20	—	ns	21
Data-in setup time	$t_{\text{DS}}$	0	—	0	—	0	—	ns	11, 21
Data-in hold time	$t_{\text{DH}}$	15	—	15	—	15	—	ns	11, 21
$\overline{\text{CAS}}$ to $\overline{\text{OE}}$ delay time	$t_{\text{COD}}$	—	0	—	0	—	0	ns	22

# HM51(S)4170D Series, HM51(S)4270D Series

## Read-Modify-Write Cycle

		HM514170D, HM51S4170D HM514270D, HM51S4270D							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	$t_{RWC}$	150	—	180	—	200	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	$t_{RWD}$	80	—	95	—	105	—	ns	10, 19
$\overline{CAS}$ to $\overline{WE}$ delay time	$t_{CWD}$	35	—	45	—	45	—	ns	10, 19
Column address to $\overline{WE}$ delay time	$t_{AWD}$	50	—	60	—	65	—	ns	10, 19
$\overline{OE}$ hold time from $\overline{WE}$	$t_{OEH}$	15	—	20	—	20	—	ns	21

## Refresh Cycle

		HM514170D, HM51S4170D HM514270D, HM51S4270D							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time (CBR refresh cycle)	$t_{CSR}$	10	—	10	—	10	—	ns	19
$\overline{CAS}$ hold time (CBR refresh cycle)	$t_{CHR}$	10	—	10	—	10	—	ns	20
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	$t_{RPC}$	10	—	10	—	10	—	ns	19
$\overline{CAS}$ precharge time in normal mode	$t_{CPN}$	10	—	10	—	10	—	ns	

## Fast Page Mode Cycle

		HM514170D, HM51S4170D HM514270D, HM51S4270D							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode cycle time	$t_{PC}$	40	—	45	—	50	—	ns	
Fast page mode $\overline{CAS}$ precharge time	$t_{CP}$	10	—	10	—	10	—	ns	
Fast page mode $\overline{RAS}$ pulse width	$t_{RASC}$	—	100000	—	100000	—	100000	ns	12
Access time from $\overline{CAS}$ precharge	$t_{ACP}$	—	35	—	40	—	45	ns	3, 13
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	$t_{RHCP}$	35	—	40	—	45	—	ns	

# HM51(S)4170D Series, HM51(S)4270D Series

## Fast Page Mode Read-Modify-Write Cycle

		HM514170D, HM51S4170D HM514270D, HM51S4270D							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
CAS precharge to $\overline{UWE}$ , $\overline{LWE}$ delay time	$t_{CPW}$	55	—	65	—	70	—	ns	21
Fast page mode read-modify-write cycle time	$t_{PCM}$	80	—	95	—	100	—	ns	

## Refresh (HM51(S)4170D Series)

Parameter	Symbol	Max	Unit	Notes
Refresh period	$t_{REF}$	16	ms	1024 cycles
Refresh period (L-version)	$t_{REF}$	128	ms	1024 cycles

## Refresh (HM51(S)4270D Series)

Parameter	Symbol	Max	Unit	Notes
Refresh period	$t_{REF}$	8	ms	512 cycles
Refresh period (L-version)	$t_{REF}$	128	ms	512 cycles

## Self Refresh Mode

		HM51S4170D, HM51S4270D							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{RAS}$ pulse width (self refresh)	$t_{RASS}$	100	—	100	—	100	—	$\mu$ s	23, 24, 25, 26
$\overline{RAS}$ precharge time (self refresh)	$t_{RPS}$	110	—	130	—	150	—	ns	
$\overline{CAS}$ hold time (self refresh)	$t_{CHS}$	-50	—	-50	—	-50	—	ns	

## HM51(S)4170D Series, HM51(S)4270D Series

- Notes:
1. AC measurements assume  $t_r = 5$  ns.  $V_{IH} = 3.0$  V,  $V_{IL} = 0.0$  V.
  2. Assumes that  $t_{RCD} \leq t_{RCD}(\text{max})$  and  $t_{RAD} \leq t_{RAD}(\text{max})$ . If  $t_{RCD}$  or  $t_{RAD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  exceeds the value shown.
  3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
  4. Assumes that  $t_{RCD} \geq t_{RCD}(\text{max})$  and  $t_{RAD} \leq t_{RAD}(\text{max})$ .
  5. Assumes that  $t_{RCD} \leq t_{RCD}(\text{max})$  and  $t_{RAD} \geq t_{RAD}(\text{max})$ .
  6.  $t_{OFF}(\text{max})$  defines the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
  7.  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
  8. Operation with the  $t_{RCD}(\text{max})$  limit insures that  $t_{RAC}(\text{max})$  can be met,  $t_{RCD}(\text{max})$  is specified as a reference point only, if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max})$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
  9. Operation with the  $t_{RAD}(\text{max})$  limit insures that  $t_{RAC}(\text{max})$  can be met,  $t_{RAD}(\text{max})$  is specified as a reference point only, if  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max})$  limit, then access time is controlled exclusively by  $t_{AA}$ .
  10.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if  $t_{WCS} \geq t_{WCS}(\text{min})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{RWD} \geq t_{RWD}(\text{min})$ ,  $t_{CWD} \geq t_{CWD}(\text{min})$ ,  $t_{AWD} \geq t_{AWD}(\text{min})$  and  $t_{CPW} \geq t_{CPW}(\text{min})$ , the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
  11. These parameters are referred to  $\overline{\text{CAS}}$  leading edge in an early write cycle and to  $\overline{\text{WE}}$  leading edge in a delayed write or a read-modify-write cycle.
  12.  $t_{RASC}$  defines  $\overline{\text{RAS}}$  pulse width in fast page mode cycles.
  13. Access time is determined by the longest among  $t_{AA}$ ,  $t_{CAC}$  and  $t_{ACP}$ .
  14. After power up pause for 100  $\mu\text{s}$ , then DRAM initialization requires a minimum of eight  $\overline{\text{RAS}}$ -only refresh or eight  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles. If the user will implement  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  timing in their system, then the eight initialization cycles MUST be  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  cycles.
  15. In delayed write or read-modify-write cycles,  $\overline{\text{OE}}$  must disable output buffer prior to applying data to the device.
  16. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
  17. The supply voltage with all  $V_{CC}$  pins must be on the same level.  
The supply voltage with all  $V_{SS}$  pins must be on the same level.
  18. A word of data can be written only when  $\overline{\text{UWE}}$  and  $\overline{\text{LWE}}$  go low at the same time. This implies that early write cycles cannot be combined with delayed write cycles in the same cycles because all data is latched at the fall of the first  $\overline{\text{WE}}$ . In other words, staggering the  $\overline{\text{WE}}$  signals in one cycle is not permitted.
  19.  $t_{RCH}$ ,  $t_{RRH}$ ,  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are determined by the earlier falling edge of  $\overline{\text{UWE}}$  and  $\overline{\text{LWE}}$ .
  20.  $t_{WCH}$  and  $t_{RCS}$  are determined by the later rising edge of  $\overline{\text{UWE}}$  or  $\overline{\text{LWE}}$ .
  21.  $t_{WP}$ ,  $t_{RWL}$ ,  $t_{CWL}$ ,  $t_{OEHL}$ ,  $t_{DS}$ ,  $t_{DH}$  and  $t_{CPW}$  should be satisfied by both  $\overline{\text{UWE}}$  and  $\overline{\text{LWE}}$ .
  22. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large  $V_{CC}/V_{SS}$  line noise, which causes to degrade  $V_{IH}(\text{min})/V_{IL}(\text{max})$  level.
  23. Please do not use  $t_{RASS}$  timing,  $10 \mu\text{s} \leq t_{RASS} \leq 100 \mu\text{s}$ . During this period, the device is in transition state from normal operation mode to self refresh mode. If  $t_{RASS} > 100 \mu\text{s}$ , then  $\overline{\text{RAS}}$  precharge time should use  $t_{RPS}$  instead of  $t_{RP}$ .
  24. If you use distributed CBR refresh mode with 15.6  $\mu\text{s}$  interval in normal read/write cycle, CBR refresh should be executed within 15.6  $\mu\text{s}$  immediately after exiting from and before entering into self refresh mode.

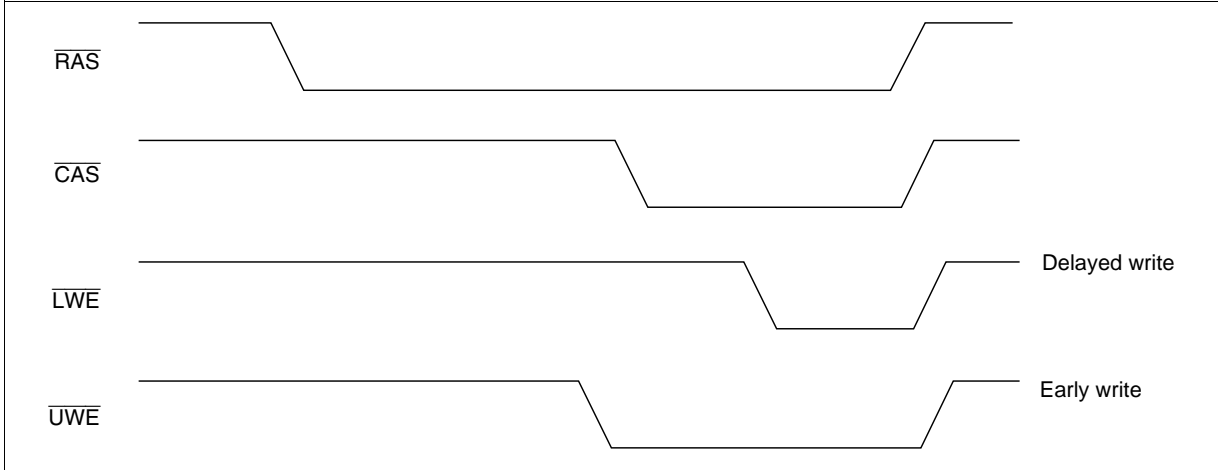


25. If you use  $\overline{\text{RAS}}$  only refresh or CBR burst refresh mode in normal read/write cycle, 1024 or 512 cycles (1024 cycles: HM51S4170D Series, 512 cycles: HM51S4270D Series) of distributed CBR refresh with 15.6  $\mu\text{s}$  interval should be executed within 16 or 8 ms (16 ms: HM51S4270D Series, 8 ms: HM51S4270D Series) immediately after exiting from and before entering into the self refresh mode.
26. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
27. XXX: H or L (H:  $V_{\text{IH}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IH}}(\text{max})$ , L:  $V_{\text{IL}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IL}}(\text{max})$ )  
/////: Invalid Dout
- When the address, clock and input pins are not described on timing waveforms, their pins must be applied  $V_{\text{IH}}$  or  $V_{\text{IL}}$ .

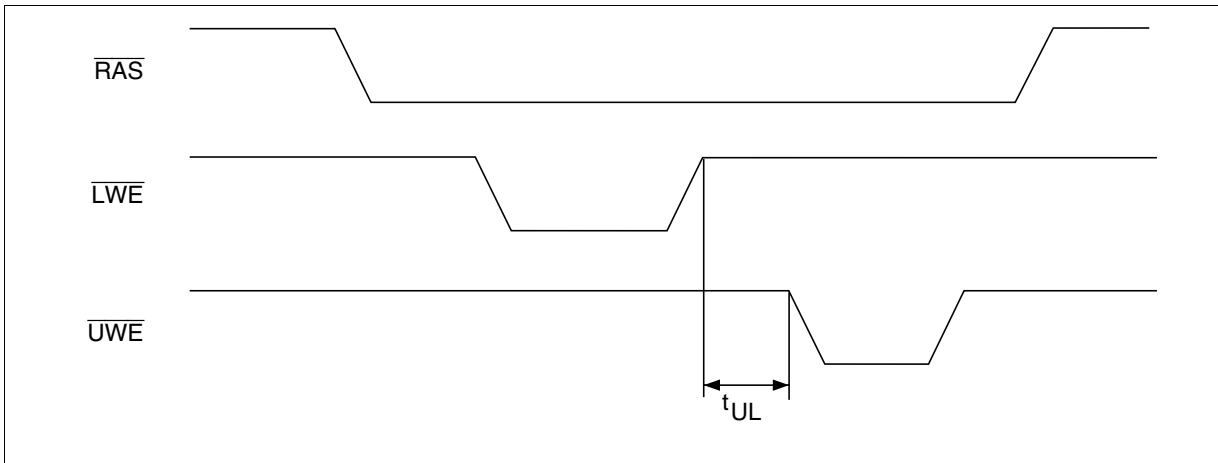
## Notes concerning $\overline{2WE}$ control

Please do not separate the  $\overline{UWE/LWE}$  operation timing intentionally. However skew between  $\overline{UWE/LWE}$  are allowed under the following conditions.

- (1) Each of the  $\overline{UWE/LWE}$  should satisfy the timing specifications individually.
- (2) Different operation mode for upper/lower byte is not allowed; such as following.

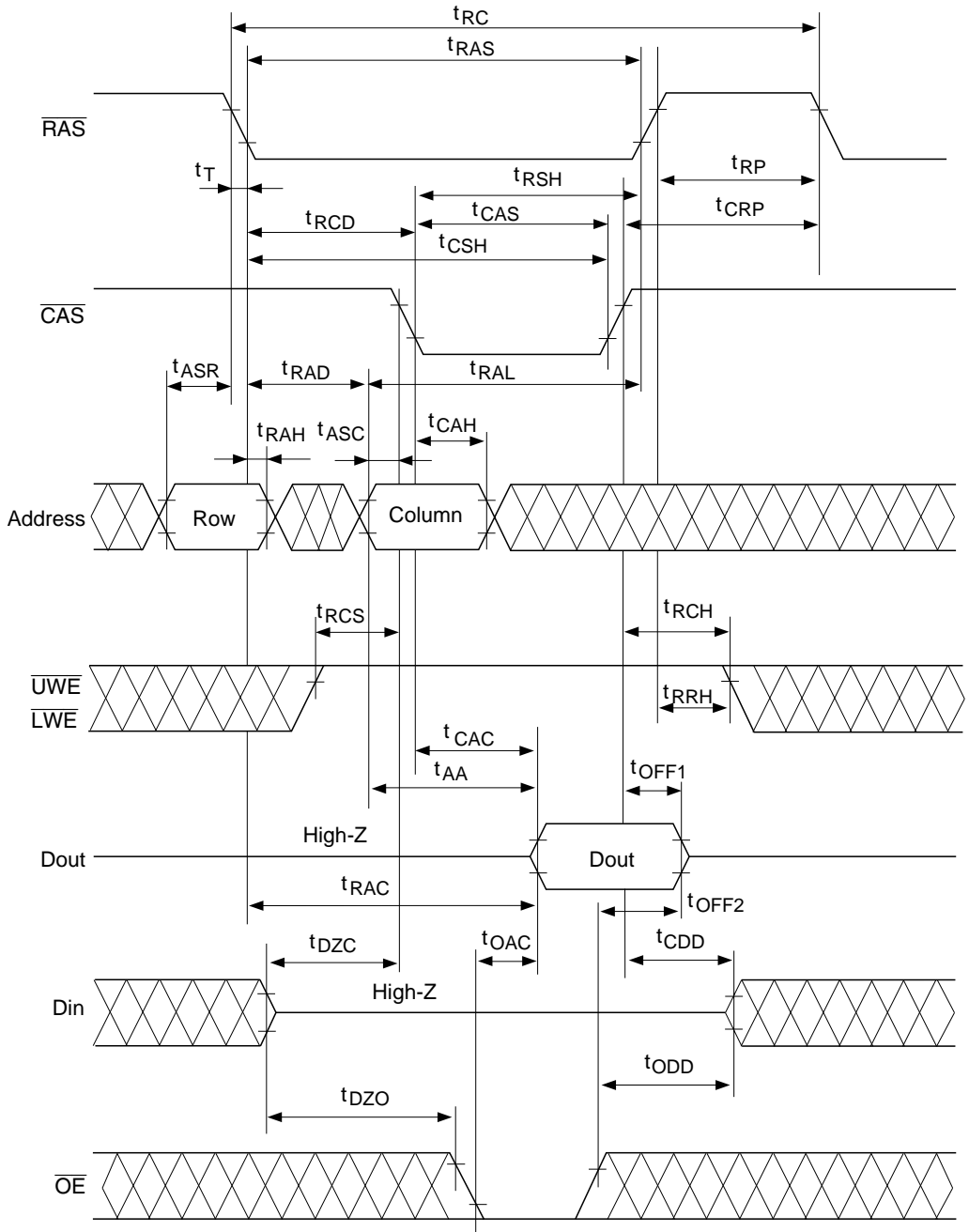


- (3) Closely separated upper/lower byte control is not allowed, unless the condition ( $t_{CP} \leq t_{UL}$ ) is satisfied.



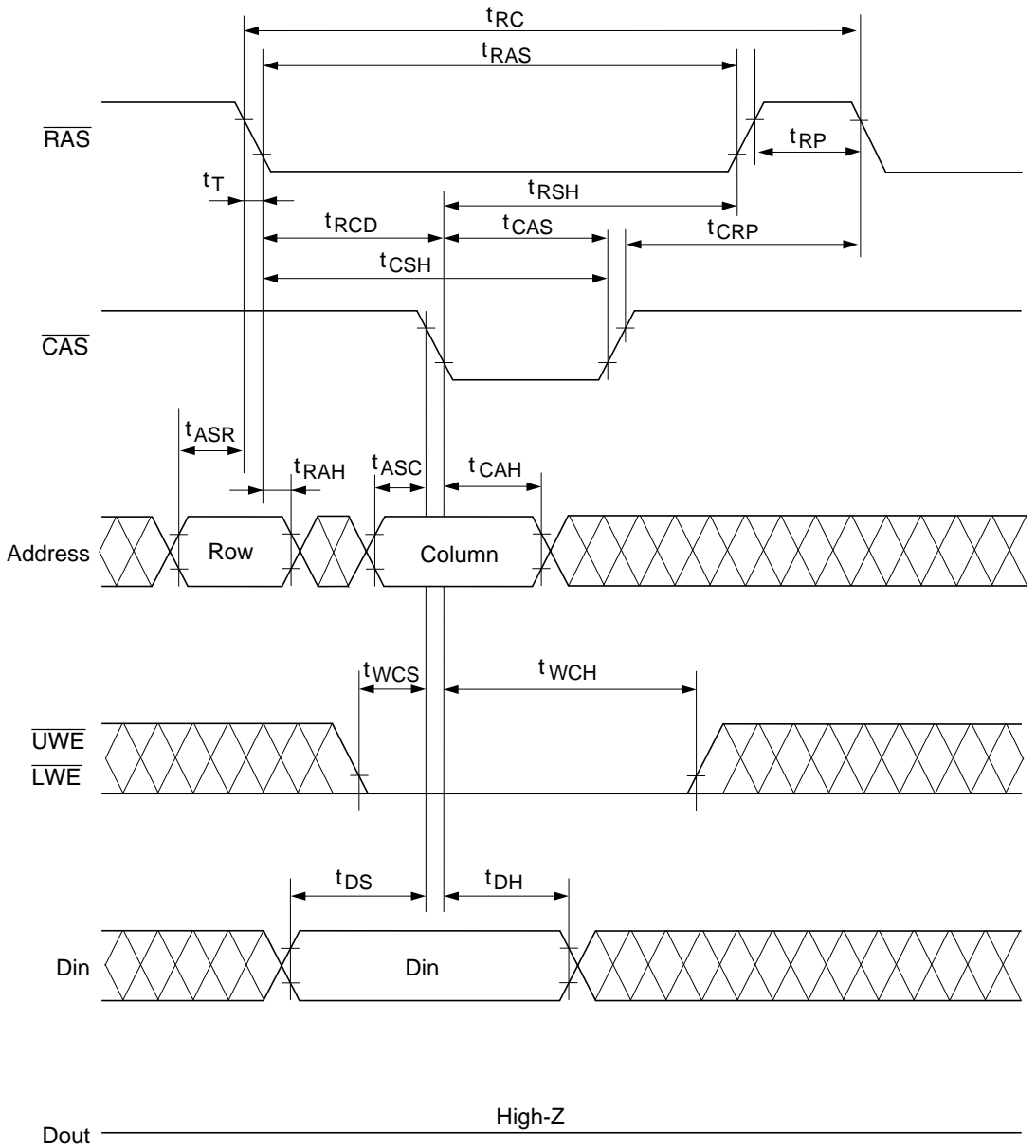
Timing Waveforms \*27

Read Cycle

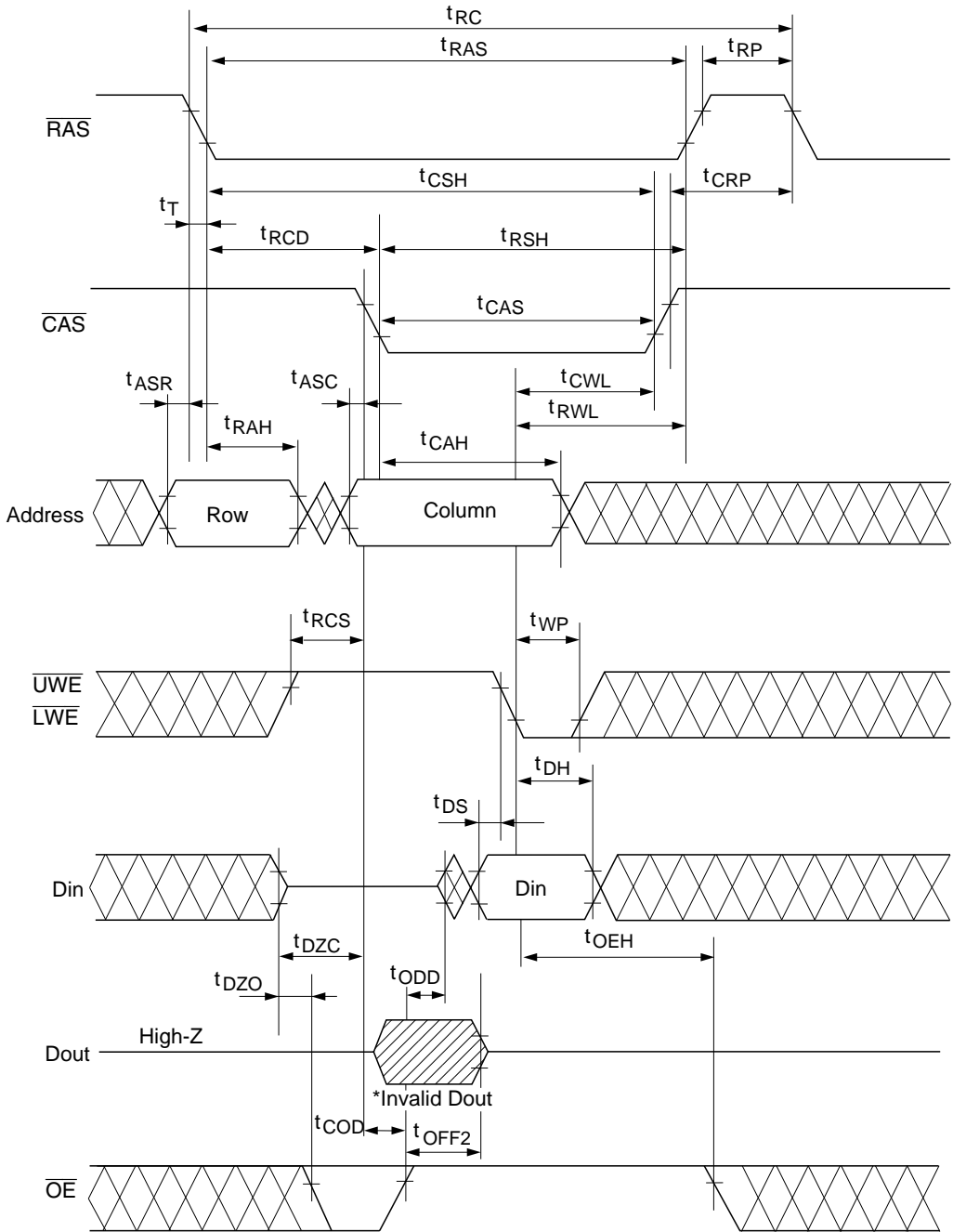


# HM51(S)4170D Series, HM51(S)4270D Series

## Early Write Cycle



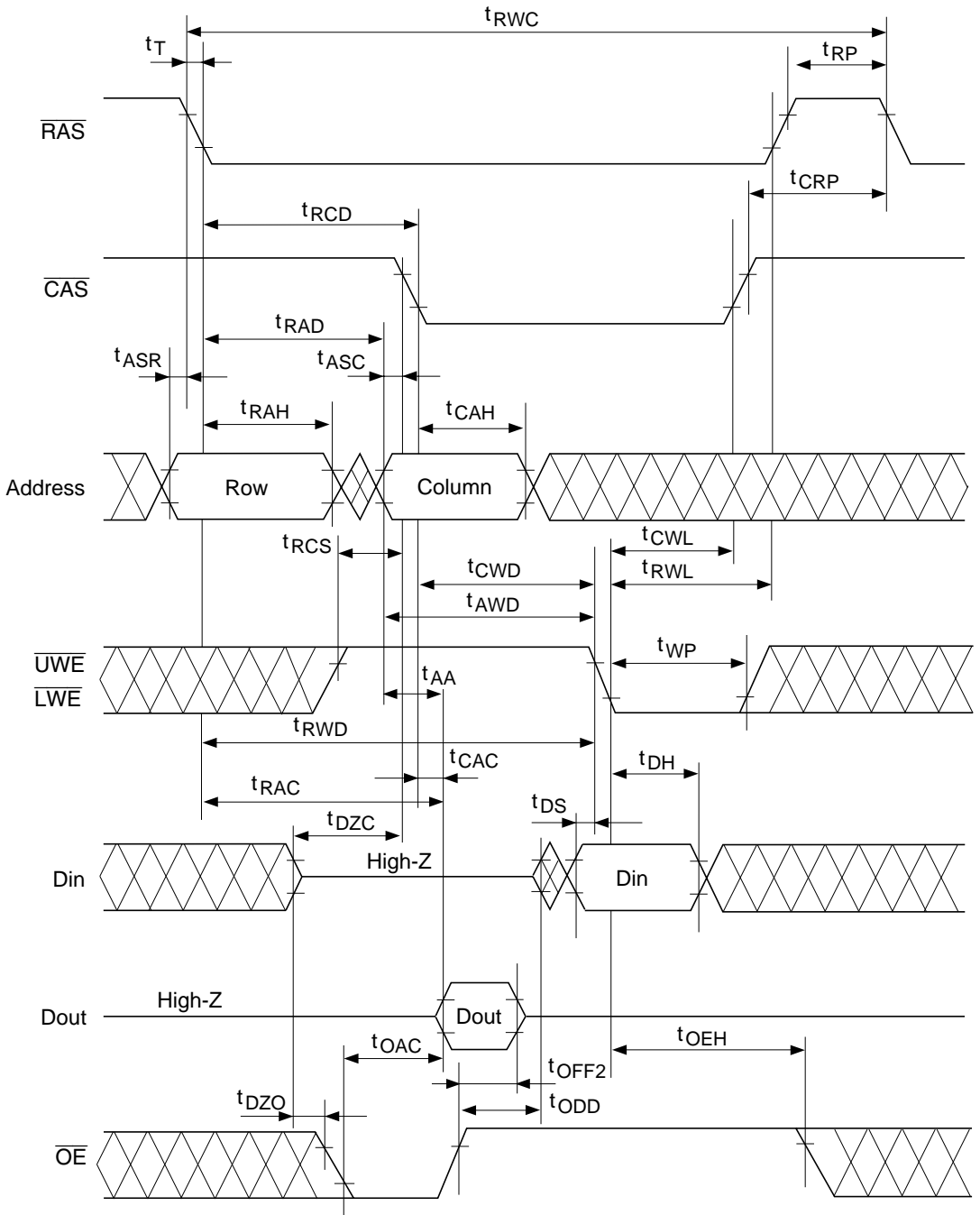
Delayed Write Cycle



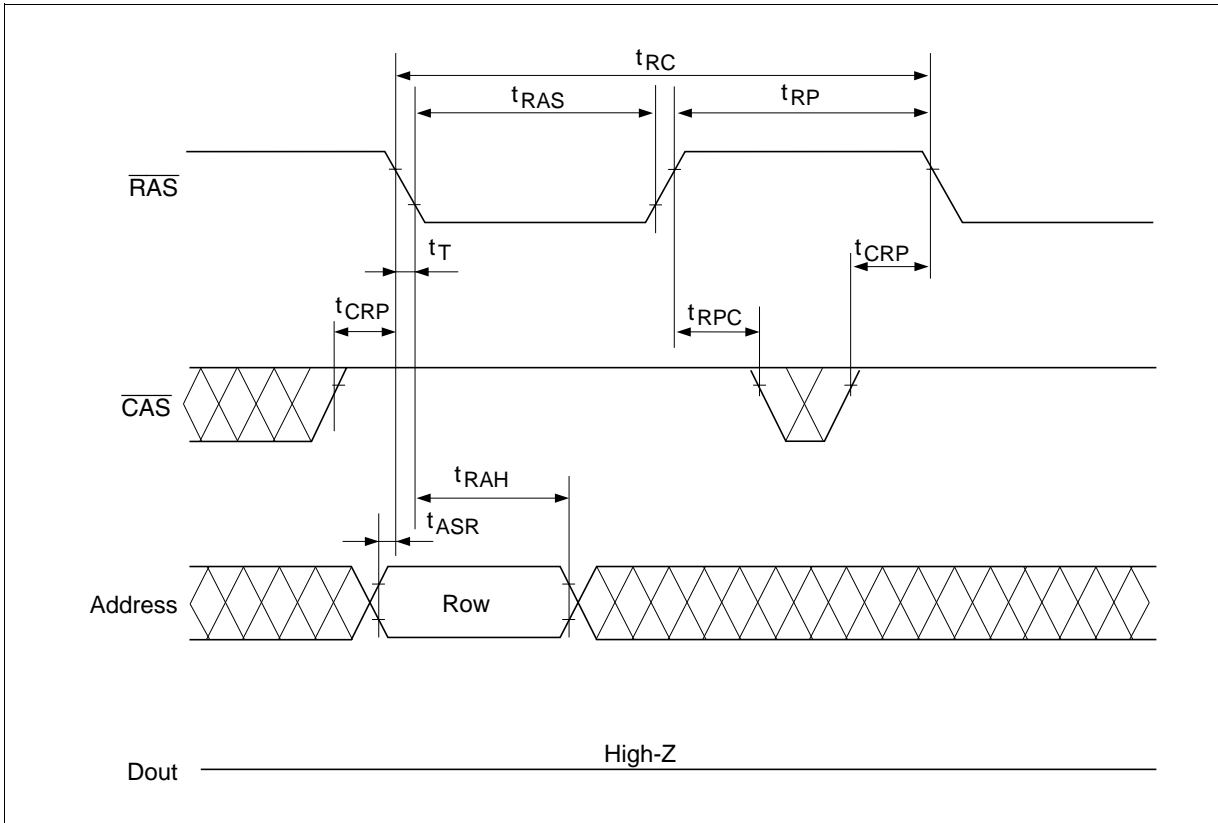
\* Do not enable Dout during delayed write cycle.

# HM51(S)4170D Series, HM51(S)4270D Series

## Read-Modify-Write Cycle

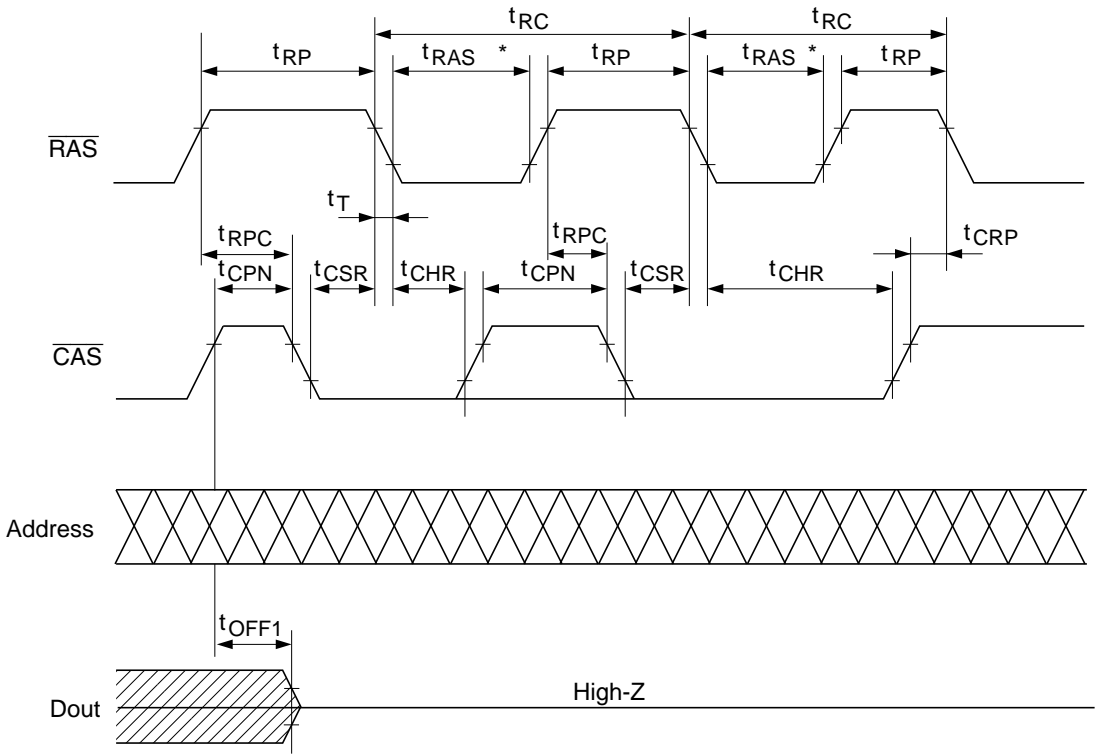


RAS-Only Refresh Cycle



# HM51(S)4170D Series, HM51(S)4270D Series

## CAS-Before-RAS Refresh Cycle



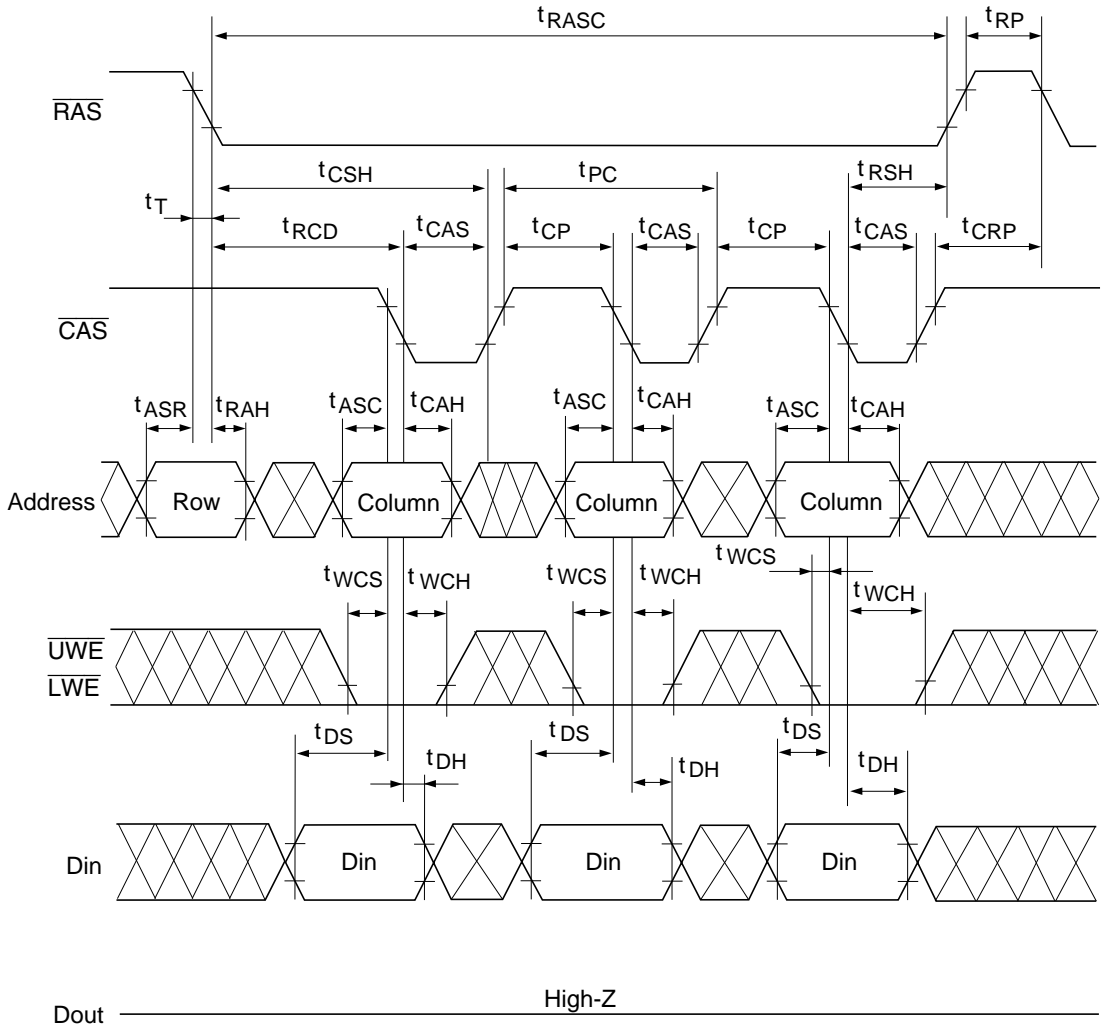
\* Do not extend  $t_{\text{RAS}} \geq t_{\text{RAS}} (\text{max})$ .  
Untested self refresh mode may be activated and loss of data may be resulted (HM514270D, HM514270D)



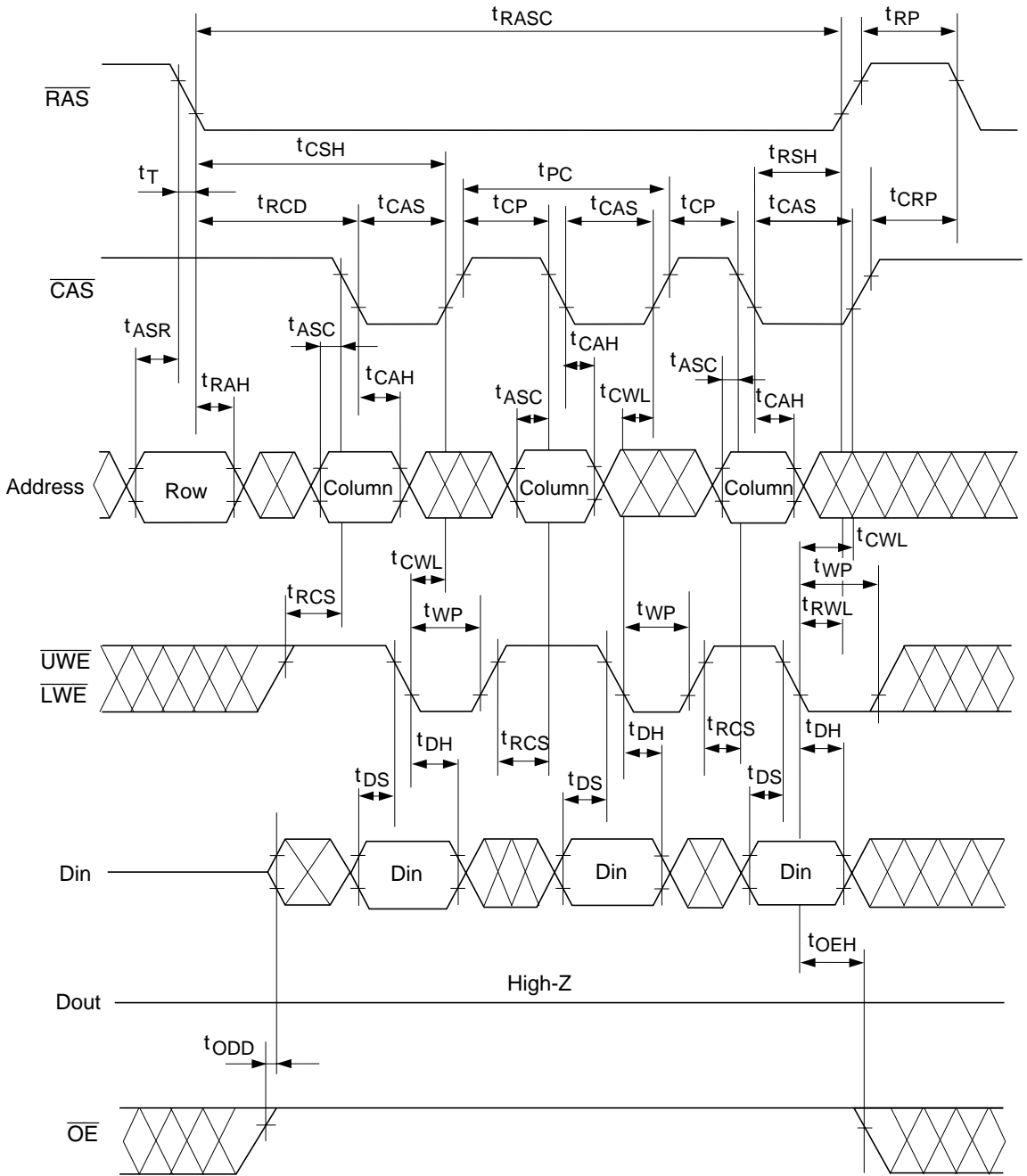


# HM51(S)4170D Series, HM51(S)4270D Series

## Fast Page Mode Early Write Cycle

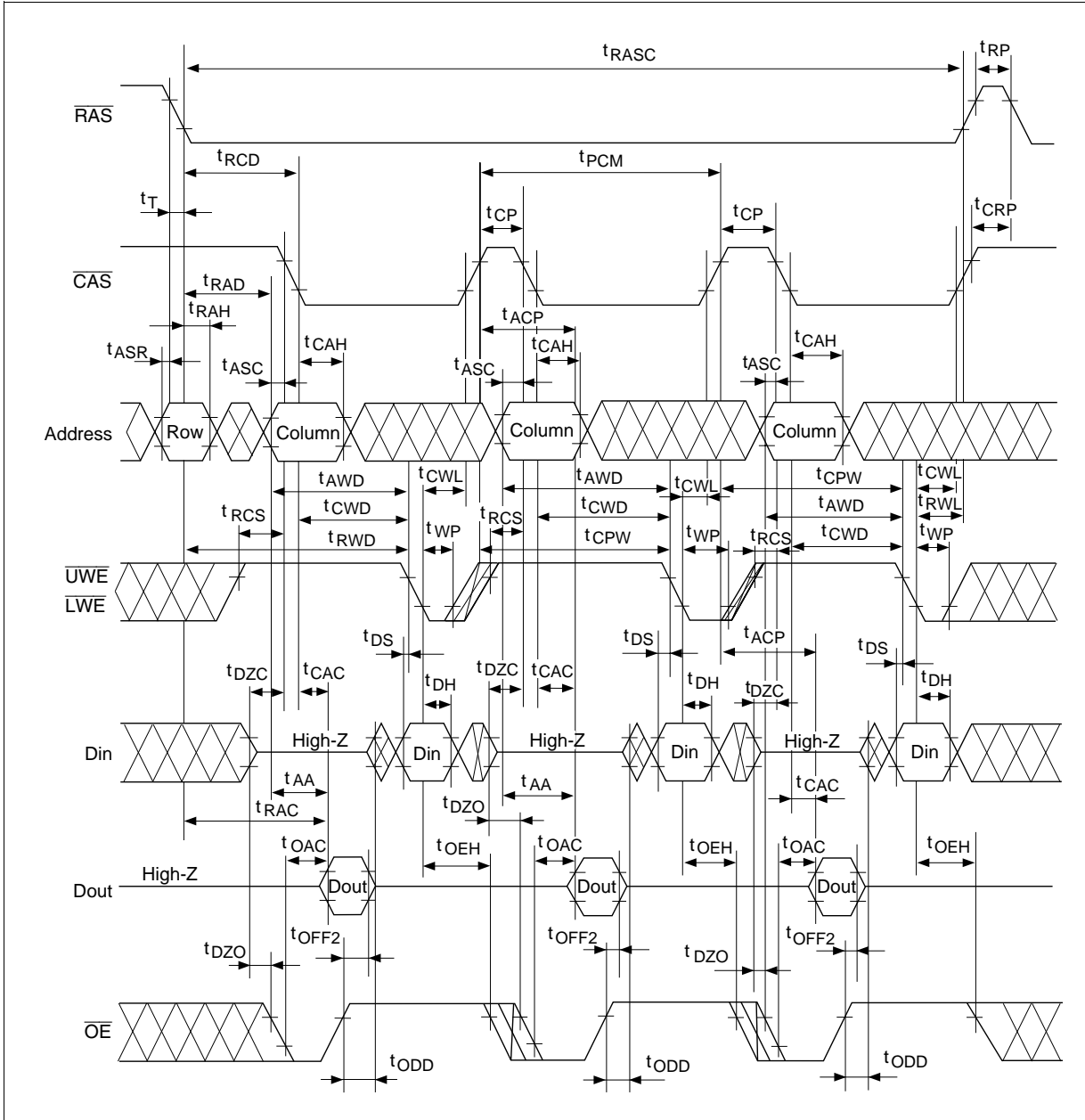


Fast Page Mode Delayed Write Cycle

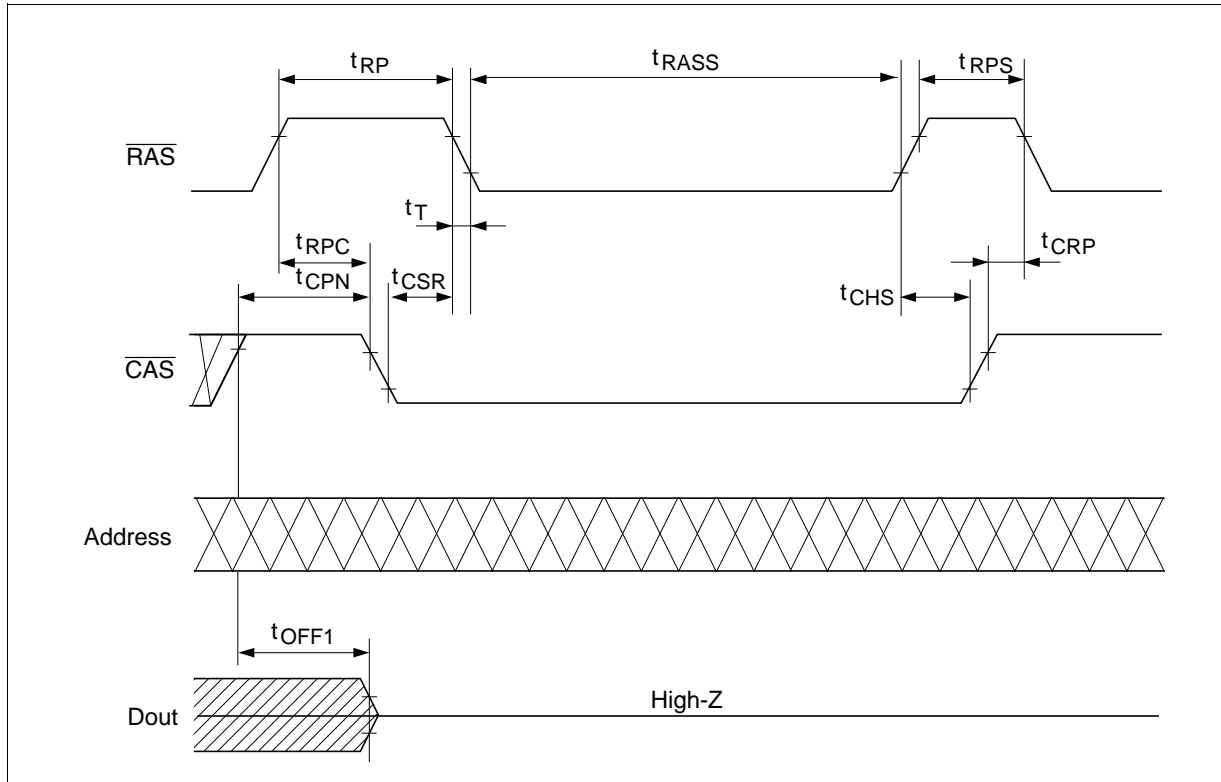


# HM51(S)4170D Series, HM51(S)4270D Series

## Fast Page Mode Read-Modify-Write Cycle



## Self Refresh Cycle\*23, 24, 25, 26



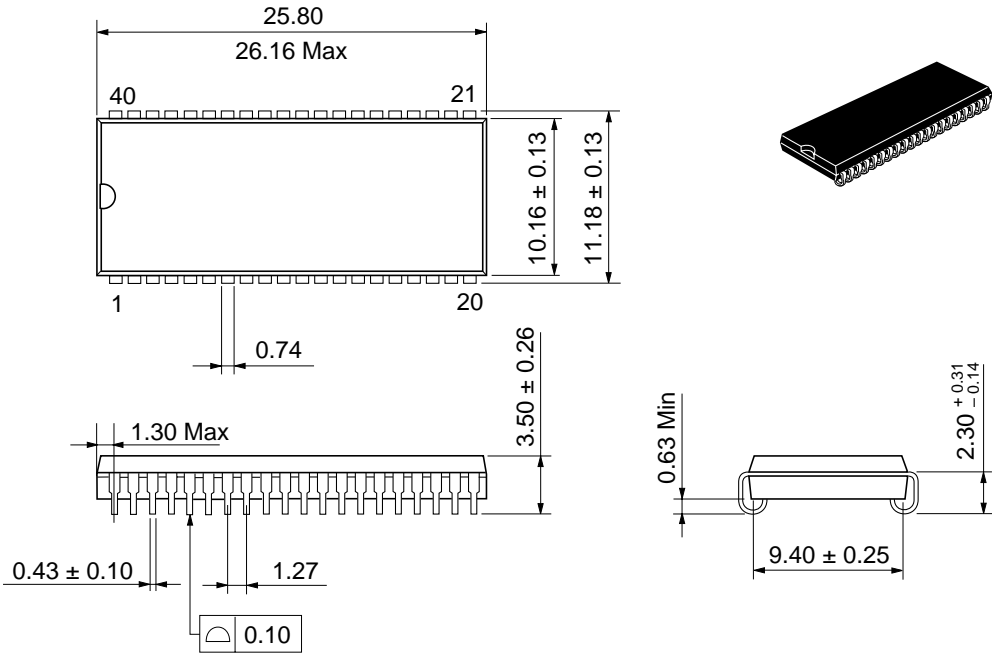
# HM51(S)4170D Series, HM51(S)4270D Series

## Package Dimensions

HM514170DJ/DLJ, HM514270DJ/DLJ Series

HM51S4170DJ/DLJ, HM51S4270DJ/DLJ Series (CP-40D)

Unit: mm

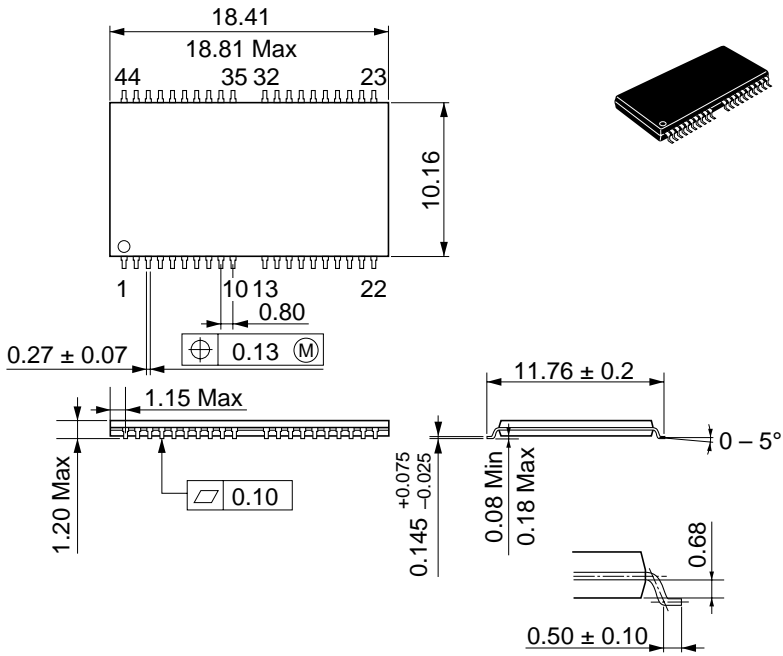


# HM51(S)4170D Series, HM51(S)4270D Series

HM514170DTT/DLTT, HM514270DTT/DLTT Series

HM51S4170DTT/DLTT, HM51S4270DTT/DLTT Series (TTP-44/40DB)

Unit: mm



When using this document, keep the following in mind:

1. This document may, wholly or partially, be subject to change without notice.
2. All rights are reserved: No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without Hitachi's permission.
3. Hitachi will not be held responsible for any damage to the user that may result from accidents or any other reasons during operation of the user's unit according to this document.
4. Circuitry and other examples described herein are meant merely to indicate the characteristics and performance of Hitachi's semiconductor products. Hitachi assumes no responsibility for any intellectual property claims or other problems that may result from applications based on the examples described herein.
5. No license is granted by implication or otherwise under any patents or other rights of any third party or Hitachi, Ltd.
6. **MEDICAL APPLICATIONS:** Hitachi's products are not authorized for use in **MEDICAL APPLICATIONS** without the written consent of the appropriate officer of Hitachi's sales company. Such use includes, but is not limited to, use in life support systems. Buyers of Hitachi's products are requested to notify the relevant Hitachi sales offices when planning to use the products in **MEDICAL APPLICATIONS**.

---

---

# HITACHI

## Hitachi, Ltd.

Semiconductor & IC Div.  
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan  
Tel: Tokyo (03) 3270-2111  
Fax: (03) 3270-5109

### For further information write to:

Hitachi America, Ltd.  
Semiconductor & IC Div.  
2000 Sierra Point Parkway  
Brisbane, CA. 94005-1835  
U S A  
Tel: 415-589-8300  
Fax: 415-583-4207

Hitachi Europe GmbH  
Electronic Components Group  
Continental Europe  
Domacher Straße 3  
D-85622 Feldkirchen  
München  
Tel: 089-9 91 80-0  
Fax: 089-9 29 30 00

Hitachi Europe Ltd.  
Electronic Components Div.  
Northern Europe Headquarters  
Whitebrook Park  
Lower Cookham Road  
Maidenhead  
Berkshire SL6 8YA  
United Kingdom  
Tel: 0628-585000  
Fax: 0628-778322

Hitachi Asia Pte. Ltd.  
16 Collyer Quay #20-00  
Hitachi Tower  
Singapore 0104  
Tel: 535-2100  
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.  
Unit 706, North Tower,  
World Finance Centre,  
Harbour City, Canton Road  
Tsim Sha Tsui, Kowloon  
Hong Kong  
Tel: 27359218  
Fax: 27306071



**Revision Record**

---

<b>Rev.</b>	<b>Date</b>	<b>Contents of Modification</b>	<b>Drawn by</b>	<b>Approved by</b>
0.0	Oct. 18, 1996	Initial issue		

---