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# HM6208H Series

65,536-word × 4-bit High Speed CMOS Static RAM

# HITACHI

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## Features

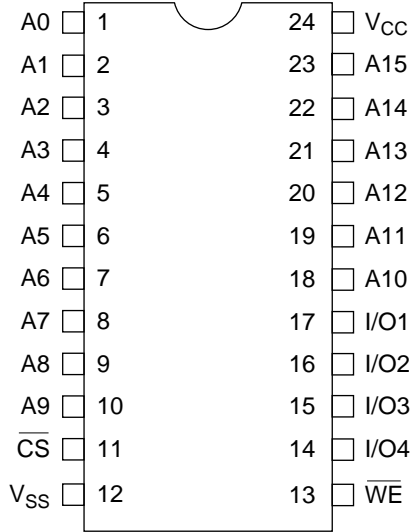
- Single 5 V supply and high density 24-pin package
- High speed: Access time 25/35/45 ns (max)
- Low power
  - Operation: 300 mW (typ)
  - Standby: 100  $\mu$ W (typ)  
30  $\mu$ W (typ) (L-version)
- Completely static memory required
  - No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible: All inputs and outputs
- Battery backup operation capability (L-version)

## Ordering Information

Type No.	Access Time	Package
HM6208HP-25	25 ns	300-mil, 24-pin plastic DIP (DP-24NC)
HM6208HP-35	35 ns	
HM6208HP-45	45 ns	
HM6208HLP-25	25 ns	300-mil, 24-pin SOJ (CP-24D)
HM6208HLP-35	35 ns	
HM6208HLP-45	45 ns	
HM6208HJP-25	25 ns	300-mil, 24-pin SOJ (CP-24D)
HM6208HJP-35	35 ns	
HM6208HJP-45	45 ns	
HM6208HLJP-25	25 ns	300-mil, 24-pin SOJ (CP-24D)
HM6208HLJP-35	35 ns	
HM6208HLJP-45	45 ns	

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## Pin Arrangement

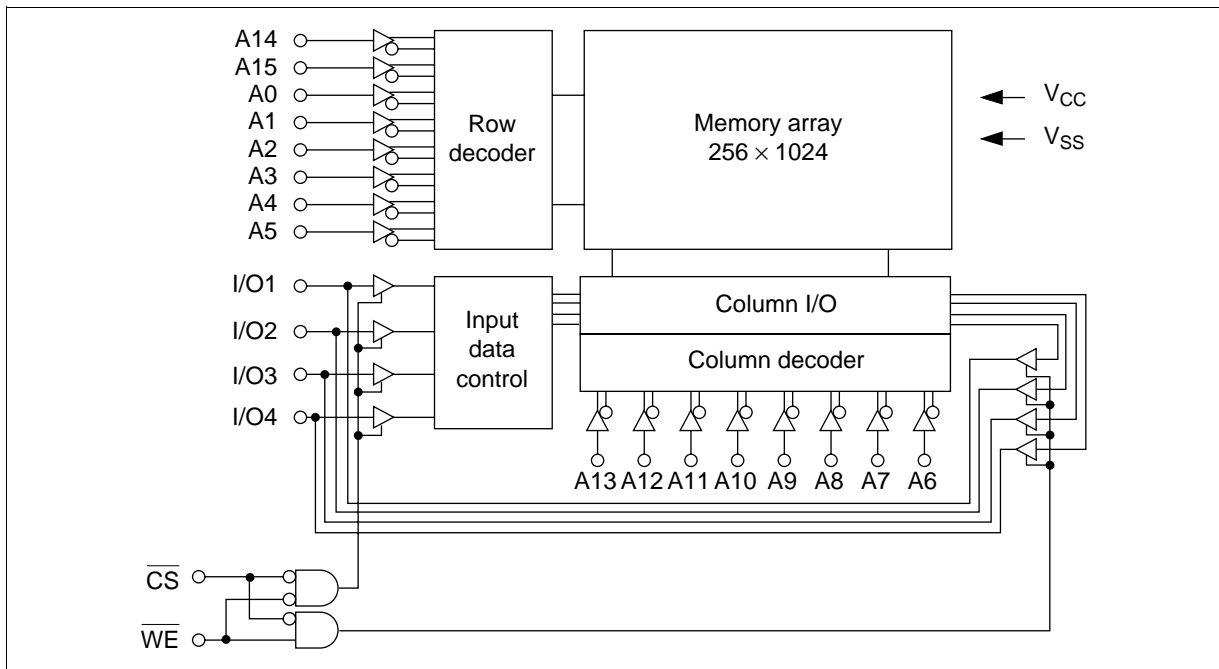


(Top view)

## Pin Description

Pin Name	Function
A0–A15	Address
I/O1–I/O4	Input/output
$\overline{\text{CS}}$	Chip select
$\overline{\text{WE}}$	Write enable
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground

Block Diagram



Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	$V_{CC}$ Current	I/O Pin	Ref. Cycle
H	×	Not selected	$I_{SB}, I_{SB1}$	High-Z	—
L	H	Read	$I_{CC}$	Dout	Read cycle
L	L	Write	$I_{CC}$	Din	Write cycle

Note: ×: Don't care.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to $V_{SS}$	$V_{in}$	$-0.5^{*1}$ to +7.0	V
Power dissipation	$P_T$	1.0	W
Operating temperature range	$T_{opr}$	0 to +70	°C
Storage temperature range	$T_{stg}$	-55 to +125	°C
Storage temperature range under bias	$T_{bias}$	-10 to +85	°C

Note: 1.  $V_{in}$  min = -2.5 V for pulse widths  $\leq 10$  ns.

# HM6208H Series

## Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
	V <sub>SS</sub>	0	0	0	V
Input high (logic 1) voltage	V <sub>IH</sub>	2.2	—	6.0	V
Input low (logic 0) voltage	V <sub>IL</sub>	-0.5 <sup>*1</sup>	—	0.8	V

Note: 1. V<sub>IL</sub> min = -2.0 V for pulse width ≤ 10 ns.

## DC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ± 10%, V<sub>SS</sub> = 0 V)

Parameter	Symbol	HM6208H-25			HM6208H-35/45			Unit	Test Conditions
		Min	Typ <sup>*2</sup>	Max	Min	Typ <sup>*2</sup>	Max		
Input leakage current	I <sub>LI</sub>	—	—	2.0	—	—	2.0	μA	V <sub>CC</sub> = Max Vin = V <sub>SS</sub> to V <sub>CC</sub>
Output leakage current	I <sub>LO</sub>	—	—	10.0	—	—	10.0	μA	$\overline{CS} = V_{IH}$ , V <sub>IO</sub> = V <sub>SS</sub> to V <sub>CC</sub>
Operating power supply current	I <sub>CC</sub>	—	60	120	—	50	100	mA	$\overline{CS} = V_{IL}$ , I <sub>IO</sub> = 0 mA, min cycle, duty = 100%
	I <sub>CC1</sub>	—	40	80	—	40	80	mA	$\overline{CS} = V_{IL}$ , I <sub>IO</sub> = 0 mA, t cycle = 50 ns, duty = 100%
Standby power supply current	ISB	—	20	40	—	15	30	mA	$\overline{CS} = V_{IH}$ , min cycle
Standby power supply current (1)	ISB1	—	0.02	2.0	—	0.02	2.0		$\overline{CS} \geq V_{CC} - 0.2$ V, 0 V ≤ Vin < 0.2 V, or Vin ≥ V <sub>CC</sub> - 0.2 V
	ISB1 <sup>*1</sup>	—	0.006	0.1 <sup>*1</sup>	—	0.006	0.1 <sup>*1</sup>		
Output low voltage	V <sub>OL</sub>	—	—	0.4	—	—	0.4	V	I <sub>OL</sub> = 8 mA
Output high voltage	V <sub>OH</sub>	2.4	—	—	2.4	—	—	V	I <sub>OH</sub> = -4.0 mA

Notes: 1. L-version

2. Typical values are at V<sub>CC</sub> = 5.0 V, Ta = +25°C and not guaranteed.

## Capacitance (Ta = 25°C, f = 1 MHz)<sup>\*1</sup>

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input capacitance	C <sub>in</sub>	—	6	pF	Vin = 0 V
Input/output capacitance	C <sub>IO</sub>	—	11	pF	V <sub>IO</sub> = 0 V

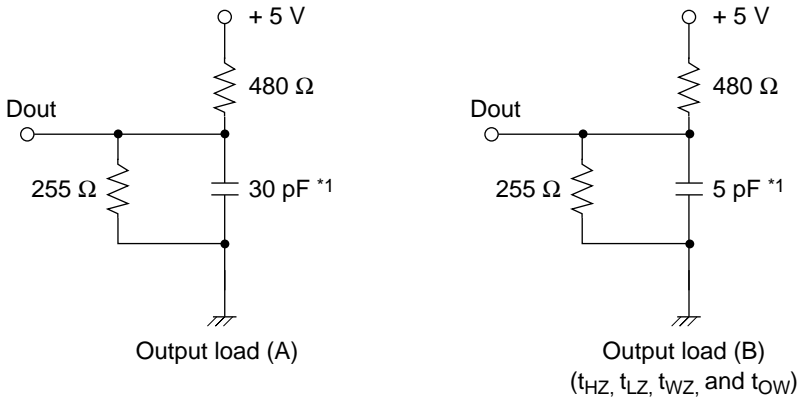
Note: 1. These parameters are sampled and not 100% tested.

**AC Characteristics** ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ , unless otherwise noted)

**Test Conditions**

- Input pulse levels:  $V_{SS}$  to 3.0 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figure

**Output Load**



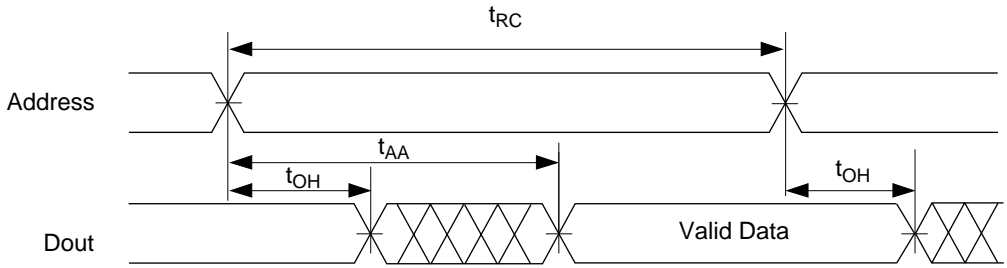
Note: 1. Including scope and jig

**Read Cycle**

Parameter	Symbol	HM6208H-25		HM6208H-35		HM6208H-45		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	$t_{RC}$	25	—	35	—	45	—	ns
Address access time	$t_{AA}$	—	25	—	35	—	45	ns
Chip select access time	$t_{ACS}$	—	25	—	35	—	45	ns
Output hold from address change	$t_{OH}$	5	—	5	—	5	—	ns
Chip selection to output in low-Z	$t_{LZ}^{*1}$	5	—	5	—	5	—	ns
Chip deselection to output in high-Z	$t_{HZ}^{*1}$	0	15	0	20	0	20	ns
Chip deselection to power up time	$t_{PU}$	0	—	0	—	0	—	ns
Chip deselection to power down time	$t_{PD}$	—	15	—	25	—	30	ns

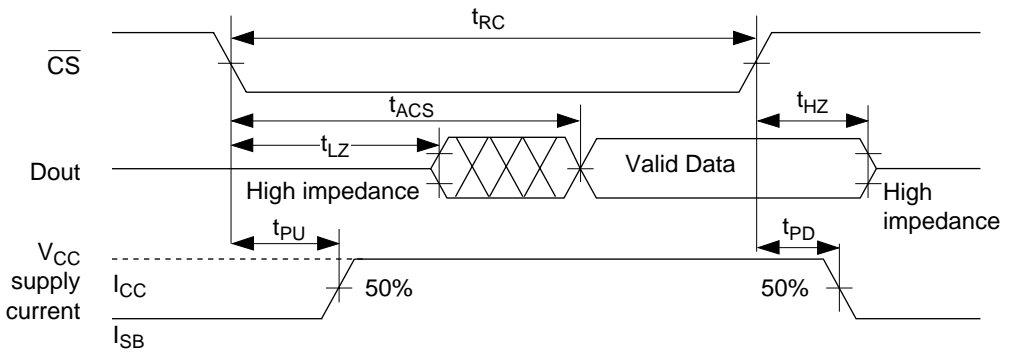
Note: 1. Transition is measured  $\pm 200$  mV from steady state voltage with load (B). These parameters are sampled and not 100% tested.

## Read Timing Waveform (1)



- Notes: 1.  $\overline{WE}$  is high for read cycle.  
2. Device is continuously selected.

## Read Timing Waveform (2)



- Notes: 1.  $\overline{WE}$  is high for read cycle.  
2. Address valid prior to or coincident with the  $\overline{CS}$  transition to low.

Write Cycle

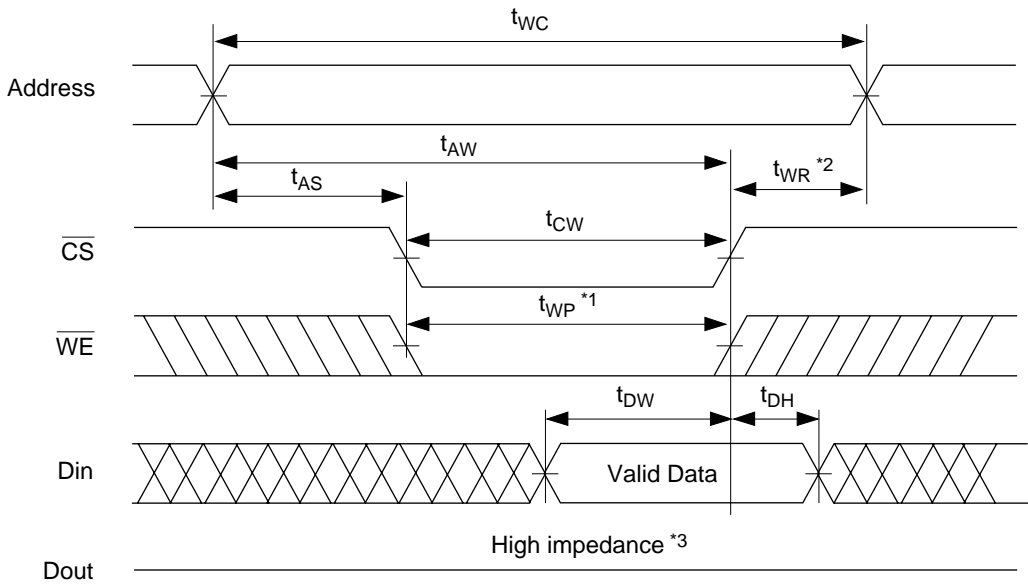
Parameter	Symbol	HM6208H-25		HM6208H-35		HM6208H-45		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	$t_{WC}$	25	—	35	—	45	—	ns
Chip selection to end of write	$t_{CW}$	20	—	30	—	40	—	ns
Address valid to end of write	$t_{AW}$	20	—	30	—	40	—	ns
Address setup time	$t_{AS}$	0	—	0	—	0	—	ns
Write pulse width	$t_{WP}$	20	—	25	—	30	—	ns
Write recovery time	$t_{WR}$	3	—	3	—	3	—	ns
Data valid to end of write	$t_{DW}$	15	—	20	—	20	—	ns
Data hold time	$t_{DH}$	0	—	0	—	0	—	ns
Write enabled to output in high-Z	$t_{WZ}^{*1}$	0	8	0	10	0	15	ns
Output active from end of write	$t_{OW}^{*1}$	0	—	0	—	0	—	ns

Note: 1. Transition is measured  $\pm 200$  mV from high impedance voltage with load (B).  
 These parameters are sampled and not 100% tested.





Write Timing Waveform (2) ( $\overline{CS}$  Controlled)



- Notes:
1. A write occurs during the overlap of a low  $\overline{CS}$  and a low  $\overline{WE}$  ( $t_{WP}$ ).
  2.  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going high to the end of the write cycle.
  3. If the  $\overline{CS}$  low transition occurs simultaneously with the  $\overline{WE}$  low transition or after the  $\overline{WE}$  transition, the output buffers remain in a high-impedance state.

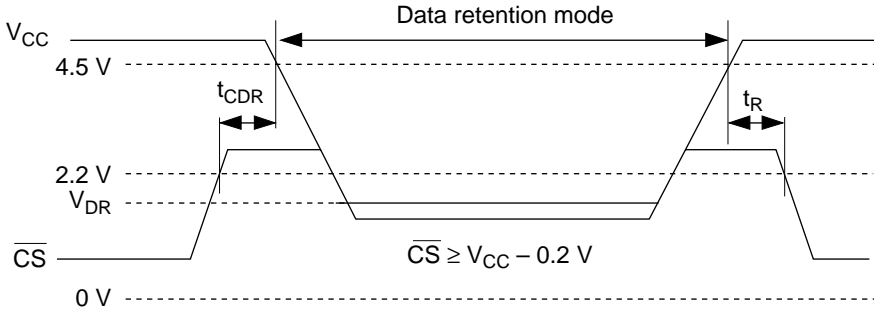
## Low $V_{CC}$ Data Retention Characteristics ( $T_a = 0$ to $+70^\circ\text{C}$ )

These characteristics are guaranteed for the L-version only.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
$V_{CC}$ for data retention	$V_{DR}$	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2 \text{ V}$ , $V_{in} \geq V_{CC} - 0.2 \text{ V}$ , or $0 \text{ V} \leq V_{in} < 0.2 \text{ V}$ , or
Data retention current	$I_{CCDR}$	—	2	$50^{*1}$	$\mu\text{A}$	
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	
Operation recovery time	$t_R$	5	—	—	ms	

Note: 1.  $V_{CC} = 3.0 \text{ V}$

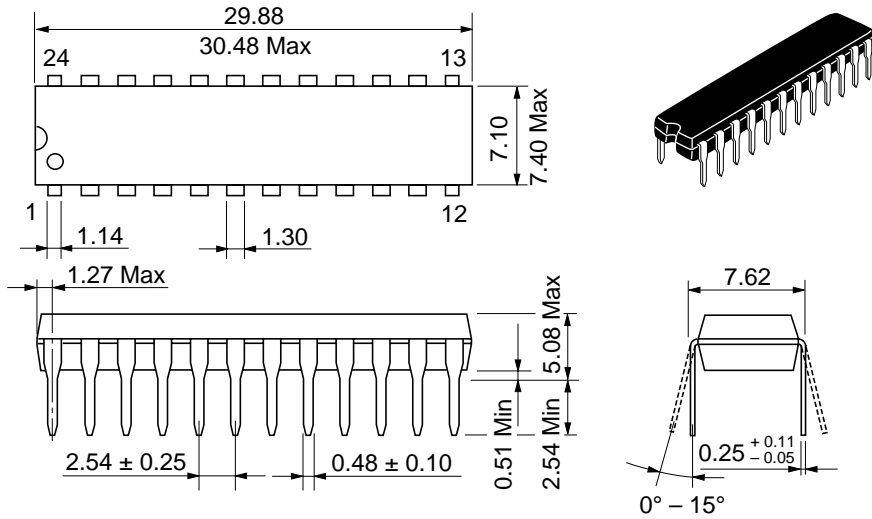
### Low $V_{CC}$ Data Retention Timing Waveform



Package Dimensions

HM6208HP/HLP Series (DP-24NC)

Unit: mm



HM6208HJP/HLJP Series (CP-24D)

Unit: mm

