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# HM62G18512 Series

8M Synchronous Fast Static RAM  
(512k-word × 18-bit)

# HITACHI

ADE-203-1185 (Z)  
Preliminary  
Rev. 0.0  
Jun. 12, 2000

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## Description

The HM62G18512 is a synchronous fast static RAM organized as 512-kword × 18-bit. It has realized high speed access time by employing the most advanced CMOS process and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. It is packaged in standard 119-bump BGA.

Note: All power supply and ground pins must be connected for proper operation of the device.

## Features

- Power supply: 3.3 V +10%, -5%
- Clock frequency: 200 MHz to 250 MHz
- Internal self-timed late write
- Byte write control (2 byte write selects, one for each 9-bit)
- Optional ×36 configuration
- HSTL compatible I/O
- Programmable impedance output drivers
- User selective input trip-point
- Differential, HSTL clock inputs
- Asynchronous  $\overline{G}$  output control
- Asynchronous sleep mode
- Limited set of boundary scan JTAG IEEE 1149.1 compatible
- Protocol: Single clock register-register mode

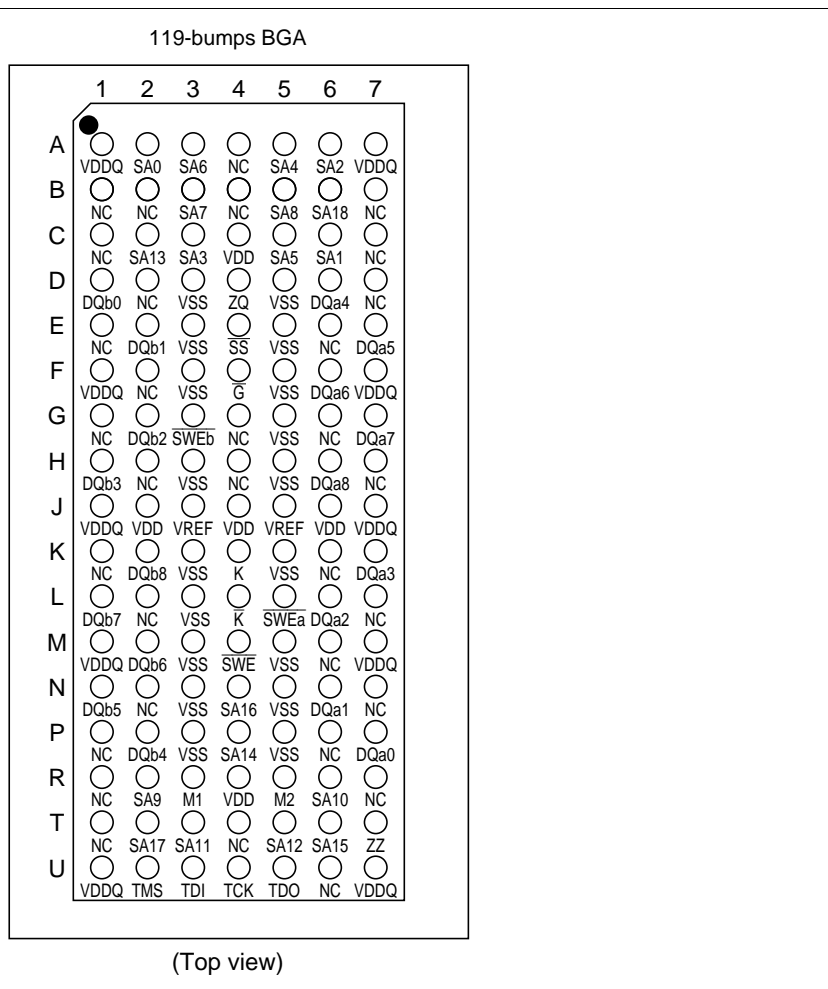
Preliminary: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

# HM62G18512 Series

## Ordering Information

Type No.	Access time	Cycle time	Package
HM62G18512BP-4	2.1 ns	4.0 ns	119-bump 1.27 mm
HM62G18512BP-5	2.5 ns	5.0 ns	14 mm × 22 mm BGA (BP-119A)

## Pin Arrangement



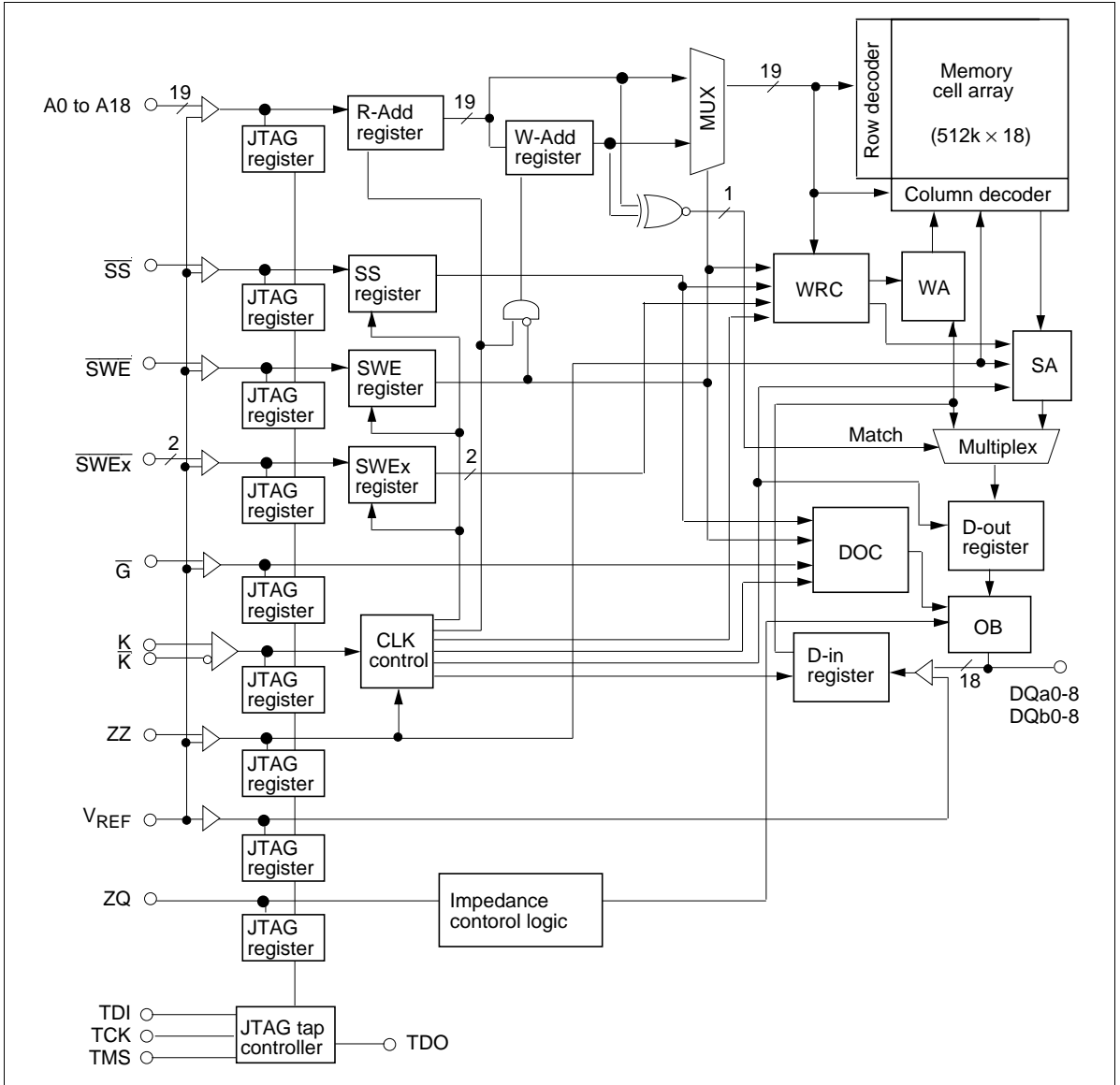
## Pin Description

Name	I/O type	Descriptions	Notes
$V_{DD}$	Supply	Core power supply	
$V_{SS}$	Supply	Ground	
$V_{DDQ}$	Supply	Output power supply	
$V_{REF}$	Supply	Input reference: provides input reference voltage	
K	Input	Clock input. Active high.	
$\bar{K}$	Input	Clock input. Active low.	
$\bar{SS}$	Input	Synchronous chip select	
$\bar{SWE}$	Input	Synchronous write enable	
$\overline{SAn}$	Input	Synchronous address input	n = 0, 1, 2...18
$\overline{SWEx}$	Input	Synchronous byte write enables	x = a, b
$\bar{G}$	Input	Asynchronous output enable	
ZZ	Input	Power down mode select	
ZQ	Input	Output impedance control	1
DQxn	I/O	Synchronous data input/output	x = a, b n = 0, 1, 2...8
M1, M2	Input	Output protocol mode select	
TMS	Input	Boundary scan test mode select	
TCK	Input	Boundary scan test clock	
TDI	Input	Boundary scan test data input	
TDO	Output	Boundary scan test data output	
NC	—	No connection	

M1	M2	Protocol	Notes
$V_{SS}$	$V_{DD}$	Synchronous register to register operation	2

- Notes:
1. ZQ is to be connected to  $V_{SS}$  via a resistance  $RQ$  where  $150 \Omega \leq RQ \leq 300 \Omega$ , if  $ZQ = V_{DDQ}$  or open, output buffer impedance will be maximum. A case of minimum impedance, it needs to connect over  $120 \Omega$  between ZQ and  $V_{SS}$ .
  2. There is 1 protocol with mode pin. Mode control pins (M1, M2) are to be tied either  $V_{DD}$  or  $V_{SS}$  respectively. The state of the Mode control inputs must be set before power-up and must not change during device operation. Mode control inputs are not standard inputs and may not meet  $V_{IH}$  or  $V_{IL}$  specification. This SRAM is tested only in the synchronous register to register operation.

## Block Diagram



## Operation Table

ZZ	$\overline{SS}$	$\overline{G}$	$\overline{SWE}$	$\overline{SWEa}$	$\overline{SWEb}$	K	$\overline{K}$	Operation	DQ (n)	DQ (n + 1)
H	×	×	×	×	×	×	×	sleep mode	High-Z	High-Z
L	H	×	×	×	×	L-H	H-L	Dead (not selected)	×	High-Z
L	×	H	×	×	×	×	×	Dead (Dummy read)	High-Z	High-Z
L	L	L	H	×	×	L-H	H-L	Read	×	Dout (a,b)0-8
L	L	×	L	L	L	L-H	H-L	Write a, b byte	High-Z	Din (a,b)0-8
L	L	×	L	L	H	L-H	H-L	Write a byte	High-Z	Din (a)0-8
L	L	×	L	H	L	L-H	H-L	Write b byte	High-Z	Din (b)0-8

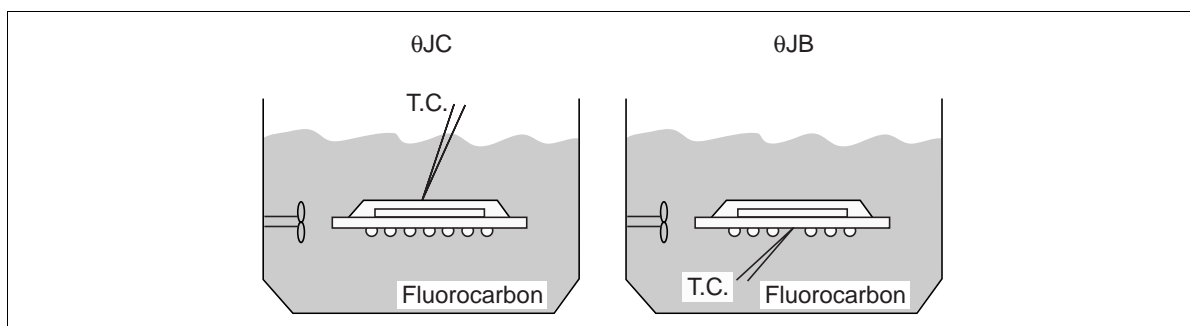
- Notes: 1. × means don't care for synchronous inputs, and H or L for asynchronous inputs.  
 2.  $\overline{SWE}$ ,  $\overline{SS}$ ,  $\overline{SWEa}$  to  $\overline{SWEb}$ , SA are sampled at the rising edge of K clock.  
 3. Although differential clock operation is implied, this SRAM will operate properly with one clock phase (either K or  $\overline{K}$ ) tied to  $V_{REF}$ . Under such single-ended clock operation, all parameters specified within this document will be met.

## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Notes
Input voltage on any pin	$V_{IN}$	-0.5 to $V_{DDQ} + 0.5$	V	1, 4
Core supply voltage	$V_{DD}$	-0.5 to 3.9	V	1
Output supply voltage	$V_{DDQ}$	-0.5 to 2.2	V	1, 4
Operating temperature	$T_{OPR}$	0 to 70	°C	
Storage temperature	$T_{STG}$	-55 to 125	°C	
Junction temperature	$T_j$	110	°C	
Output short-circuit current	$I_{OUT}$	25	mA	
Latch up current	$I_{LI}$	200	mA	
Package junction to case thermal resistance	$\theta_{JC}$	2	°C/W	5, 7
Package junction to ball thermal resistance	$\theta_{JB}$	5	°C/W	6, 7

Notes: 1. All voltage is referred to  $V_{SS}$ .

- Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted the Operation Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
- These CMOS memory circuits have been designed to meet the DC and AC specifications shown in the tables after thermal equilibrium has been established.
- The supply voltage application sequence need to be powered up in the following manner:  $V_{SS}$ ,  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{REF}$  then  $V_{IN}$ . Remember, according to the Absolute Maximum Ratings table,  $V_{DDQ}$  is not to exceed 3.9 V, whatever the instantaneous value of  $V_{DDQ}$ .
- $\theta_{JC}$  is measured at the center of mold surface in fluorocarbon (See Figure "Definition of Measurement").
- $\theta_{JB}$  is measured on the center ball pad after removing the ball in fluorocarbon (See Figure "Definition of Measurement").
- These thermal resistance values have error of  $\pm 5^\circ\text{C/W}$ .



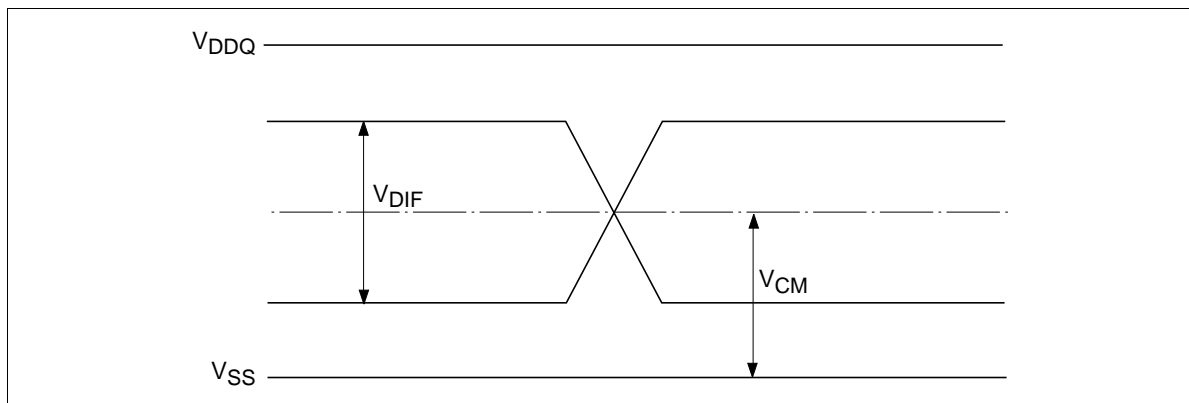
**Definition of Measurement**

Note: The following the DC and AC specifications shown in the Tables, this device is tested under the minimum transverse air flow exceeding 500 linear feet per minute.

## DC Operating Conditions (Ta = 0 to 70°C [Tj max = 110°C])

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage (Core)	$V_{DD}$	3.135	3.30	3.63	V	
Supply voltage (I/O)	$V_{DDQ}$	1.4	1.5	1.6	V	
Supply voltage	$V_{SS}$	0	0	0	V	
Input reference voltage (I/O)	$V_{REF}$	0.65	0.75	0.90	V	1
Input high voltage	$V_{IH}$	$V_{REF} + 0.1$	—	$V_{DDQ} + 0.3$	V	4
Input low voltage	$V_{IL}$	-0.5	—	$V_{REF} - 0.1$	V	4
Clock differential voltage	$V_{DIF}$	0.1	—	$V_{DDQ} + 0.3$	V	2, 3
Clock common mode voltage	$V_{CM}$	0.55	—	0.90	V	3

- Notes:
1. Peak to peak AC component superimposed on  $V_{REF}$  may not exceed 5% of  $V_{REF}$ .
  2. Minimum differential input voltage required for differential input clock operation.
  3. See following figure.
  4.  $V_{REF} = 0.75$  V (typ).



**Differential Voltage/Common Mode Voltage**

## DC Characteristics (Ta = 0 to 70°C, [Tj] max = 110°C), V<sub>DD</sub> = 3.3 V +10%, -5%)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input leakage current	I <sub>LI</sub>	—	—	2	μA	1
Output leakage current	I <sub>LO</sub>	—	—	5	μA	2
Standby current	I <sub>SBZZ</sub>	—	—	100	mA	3
V <sub>DD</sub> operating current, excluding output drivers 4 ns cycle	I <sub>DD4</sub>	—	—	700	mA	4
V <sub>DD</sub> operating current, excluding output drivers 5 ns cycle	I <sub>DD5</sub>	—	—	600	mA	4
Quiescent active power supply current	I <sub>DD2</sub>	—	—	200	mA	5
Output low voltage	V <sub>OL</sub>	V <sub>SS</sub>	—	V <sub>SS</sub> + 0.4	V	6
Output high voltage	V <sub>OH</sub>	V <sub>DDQ</sub> - 0.4	—	V <sub>DDQ</sub>	V	6
ZQ pin connect resistance	RQ	150	250	300	Ω	
Output low current	I <sub>OL</sub>	(V <sub>DDQ</sub> /2)/[(RQ/5)-15%]	—	(V <sub>DDQ</sub> /2)/[(RQ/5)+15%]	mA	7, 9
Output high current	I <sub>OH</sub>	(V <sub>DDQ</sub> /2)/[(RQ/5-4)+15%]	—	(V <sub>DDQ</sub> /2)/[(RQ/5-4)-15%]	mA	8, 9

Notes: 1.  $0 \leq V_{in} \leq V_{DDQ}$  for all input pins (except V<sub>REF</sub>, ZQ, M1, M2 pin).

2.  $0 \leq V_{out} \leq V_{DDQ}$ , DQ in High-Z.

3. All inputs (except clock) are held at either V<sub>IH</sub> or V<sub>IL</sub>, ZZ is held at V<sub>IH</sub>, Iout = 0 mA, Spec is guaranteed at 75°C junction temperature.

4. Iout = 0 mA, read 50%/write 50%, V<sub>DD</sub> = V<sub>DD</sub> max, V<sub>IN</sub> = V<sub>IH</sub> or V<sub>IL</sub>, Frequency = minimum cycle.

5. Iout = 0 mA, read 50%/write 50%, V<sub>DD</sub> = V<sub>DD</sub> max, V<sub>IN</sub> = V<sub>IH</sub> or V<sub>IL</sub>, Frequency = 3 MHz.

6. Minimum impedance push pull output buffer mode, I<sub>OH</sub> = -6 mA, I<sub>OL</sub> = 6 mA.

7. Measured at V<sub>OL</sub> = 1/2 V<sub>DDQ</sub>.

8. Measured at V<sub>OH</sub> = 1/2 V<sub>DDQ</sub>.

9. Output buffer impedance can be programmed by terminating the ZQ pin to V<sub>SS</sub> through a precision resistor (RQ). The value of RQ is five times the output impedance desired. The allowable range of RQ to guarantee impedance matching with a tolerance of 15% is between 150 Ω and 300 Ω. If the status of ZQ pin is open, output impedance is maximum. Maximum impedance occurs with ZQ connected to V<sub>DDQ</sub>. The impedance update of the output driver occurs when the SRAM is in High-Z. Write and Deselect operations will synchronously switch the SRAM into and out of High-Z, therefore triggering an update. The user may choose to invoke asynchronous  $\bar{G}$  updates by providing a  $\bar{G}$  setup and hold about the K clock to guarantee the proper update. At power-up, the output impedance defaults to minimum impedance. It will take 2048 cycles for the impedance to be completely updated if the programmed impedance is much higher than minimum impedance.



**Capacitance** ( $T_a = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )

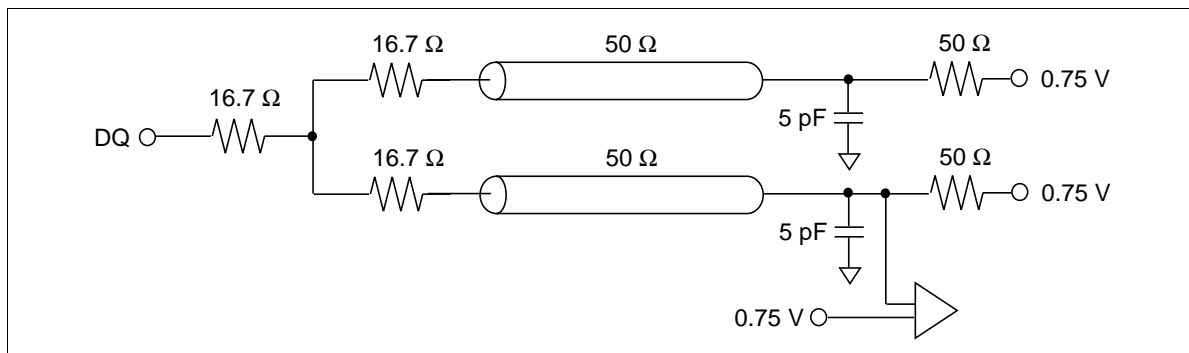
Parameter	Symbol	Min	Max	Unit	Note
Input capacitance ( $\overline{\text{SAn}}$ , $\overline{\text{SS}}$ , $\overline{\text{SWE}}$ , $\overline{\text{SWEx}}$ )	$C_{\text{IN}}$	—	4	pF	1
Input capacitance ( $\text{K}$ , $\overline{\text{K}}$ , $\overline{\text{G}}$ )	$C_{\text{CLK}}$	—	7	pF	1
Input/Output capacitance ( $\text{DQxn}$ )	$C_{\text{IO}}$	—	5	pF	1

Note: 1. This parameter is sampled and not 100% tested.

**AC Characteristics** ( $T_a = 0\text{ to }70^\circ\text{C}$ , [ $T_j \text{ max} = 110^\circ\text{C}$ ],  $V_{\text{DD}} = 3.3\text{ V} +10\%$ ,  $-5\%$ )

**Test Conditions**

- Input pulse levels ( $\text{K}$ ,  $\overline{\text{K}}$ ):  $V_{\text{DIF}} = 0.75\text{ V}$ ,  $V_{\text{CM}} = 0.75\text{ V}$
- Input timing reference level ( $\text{K}$ ,  $\overline{\text{K}}$ ): Differential cross point
- Input pulse levels (except  $\text{K}$ ,  $\overline{\text{K}}$ ):  $V_{\text{IL}} = 0.25\text{ V}$ ,  $V_{\text{IH}} = 1.25\text{ V}$
- Input and output timing reference levels (except  $\text{K}$ ,  $\overline{\text{K}}$ ):  $V_{\text{REF}} = 0.75\text{ V}$
- Input rise and fall time:  $0.5\text{ ns}$  (10% to 90%)
- Measurement condition: the minimum impedance push pull output buffer mode,  $I_{\text{OH}} = -6\text{ mA}$ ,  $I_{\text{OL}} = 6\text{ mA}$
- Output driver supply voltage:  $V_{\text{DDQ}} = 1.5\text{ V}$
- Output load: See figure



# HM62G18512 Series

Single Differential Clock Register-Register Mode ( $M1 = V_{SS}$ ,  $M2 = V_{DD}$ )

Parameter	Symbol	HM62G18512				Unit	Notes
		-4		-5			
		Min	Max	Min	Max		
CK clock cycle time	$t_{KHKH}$	4.0	—	5.0	—	ns	
CK clock high width	$t_{KHKL}$	1.5	—	1.5	—	ns	
CK clock low width	$t_{KLKH}$	1.5	—	1.5	—	ns	
Address setup time	$t_{AVKH}$	0.5	—	0.5	—	ns	
Data setup time	$t_{DVKH}$	0.5	—	0.5	—	ns	
Address hold time	$t_{KHAX}$	0.75	—	1.0	—	ns	1
Data hold time	$t_{KHDX}$	0.75	—	1.0	—	ns	1
Clock high to output valid	$t_{KHQV}$	—	2.1	—	2.5	ns	2
Clock high to output hold	$t_{KHQX}$	0.5	—	0.5	—	ns	2
Clock high to output valid ( $\overline{SS}$ control)	$t_{KHQX2}$	—	2.1	—	2.5	ns	2, 5
Clock high to output High-Z	$t_{KHQZ}$	—	2.5	—	3.0	ns	2, 3
Output enable low to output Low-Z	$t_{GLQX}$	0.5	—	0.5	—	ns	2, 5
Output enable low to output valid	$t_{GLQV}$	—	2.5	—	2.5	ns	2, 3
Output enable low to output High-Z	$t_{GHQZ}$	—	2.5	—	2.5	ns	2, 3
Sleep mode recovery time	$t_{ZZR}$	10.0	—	10.0	—	ns	6
Sleep mode enable time	$t_{ZZE}$	—	10.0	—	10.0	ns	2, 3, 6

Notes: 1. Guaranteed by design.

2. Refer to the Test Conditions.

3. Transitions are measured at start point of output high impedance from output low impedance.

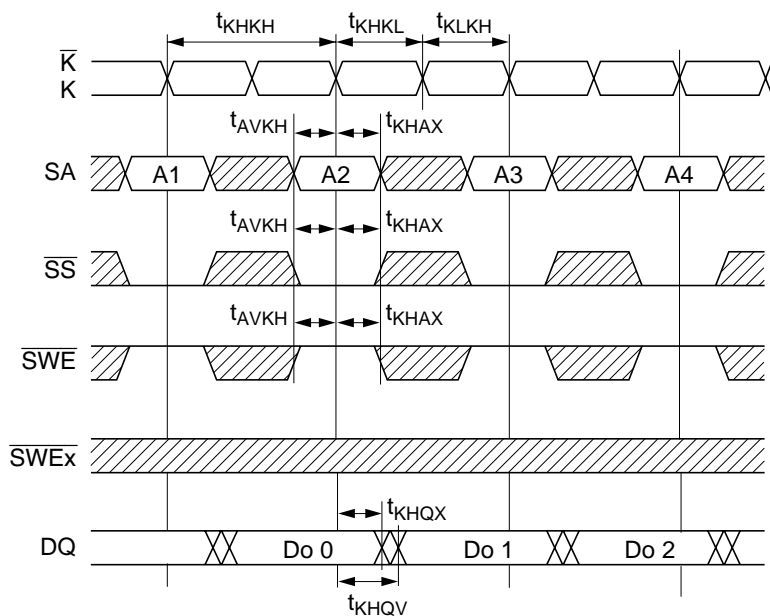
4. Output driver impedance updates during High-Z.

5. Transitions are measured  $\pm 50$  mV from steady state voltage.

6. When ZZ is switching, clock input K must be at same logic levels for reliable operation.

Timing Waveforms

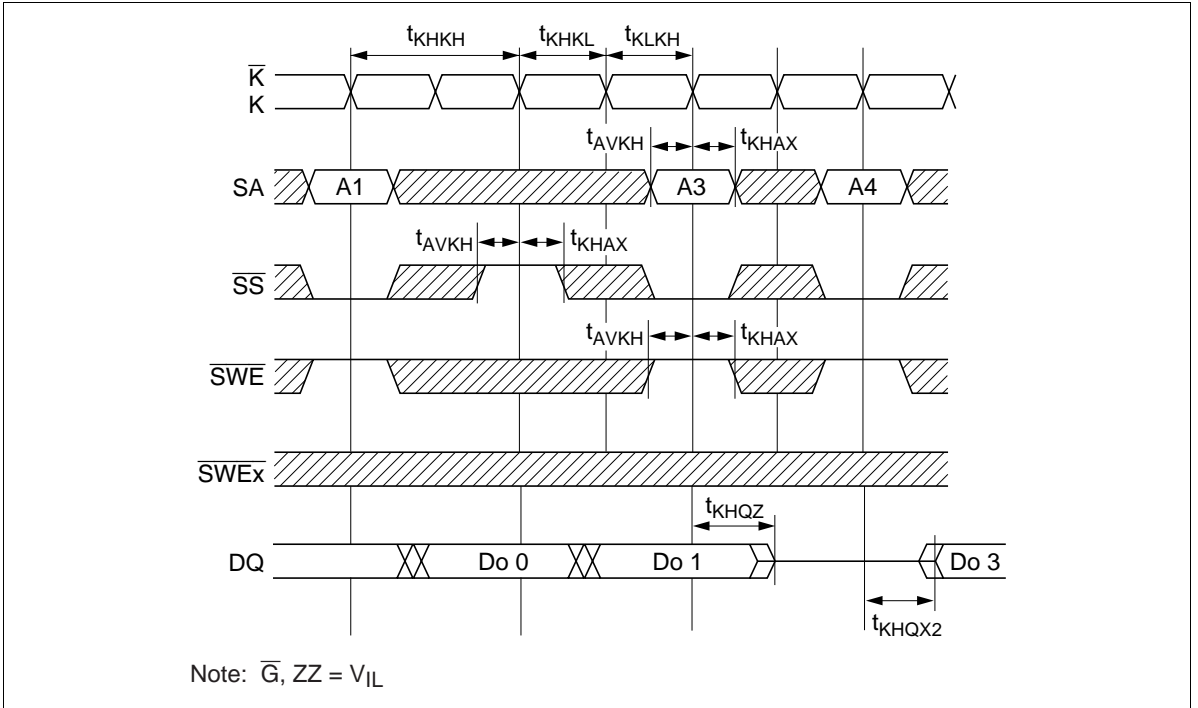
Read Cycle-1



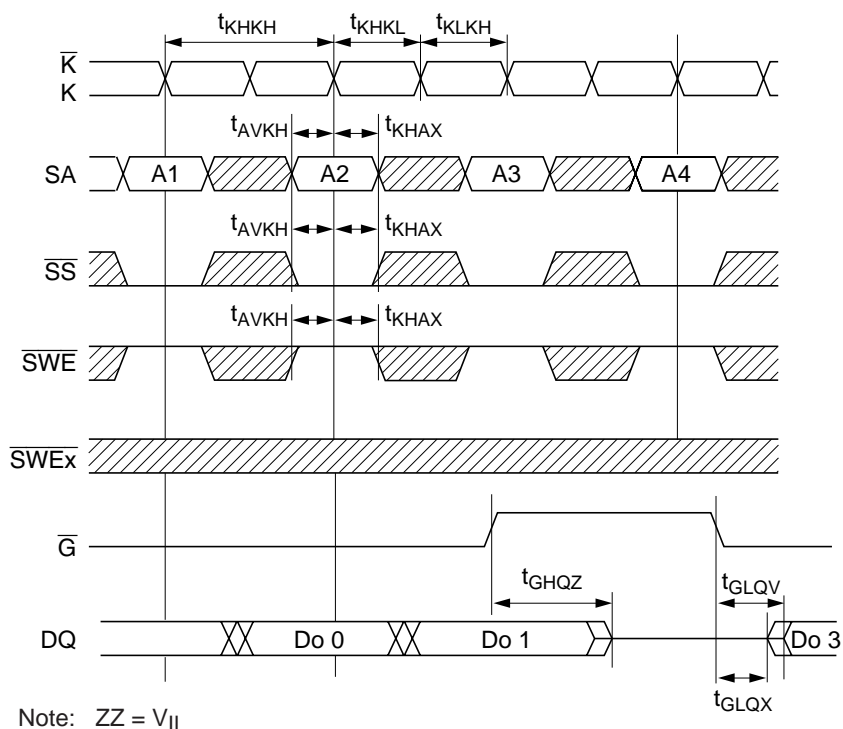
Note:  $\bar{G}$ , ZZ =  $V_{IL}$

# HM62G18512 Series

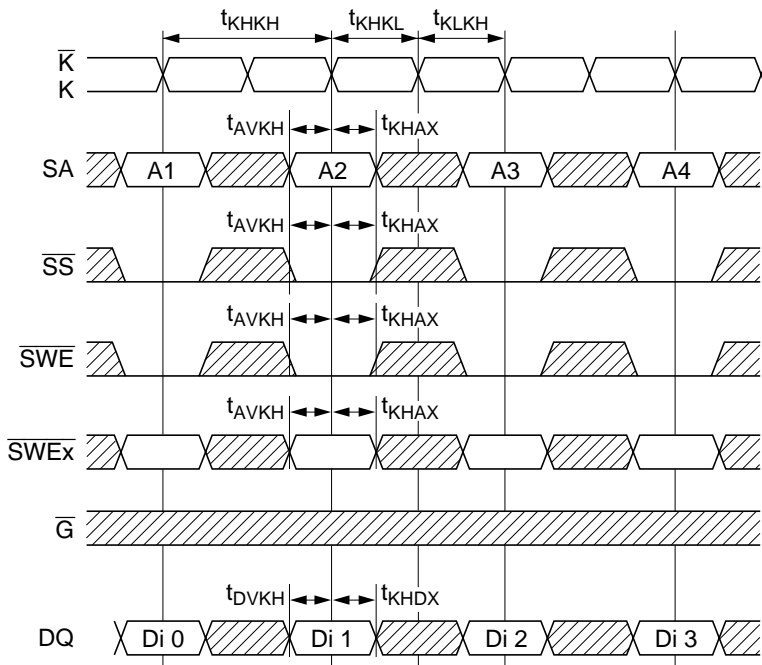
## Read Cycle-2 ( $\overline{SS}$ Controlled)



Read Cycle-3 ( $\overline{G}$  Controlled)

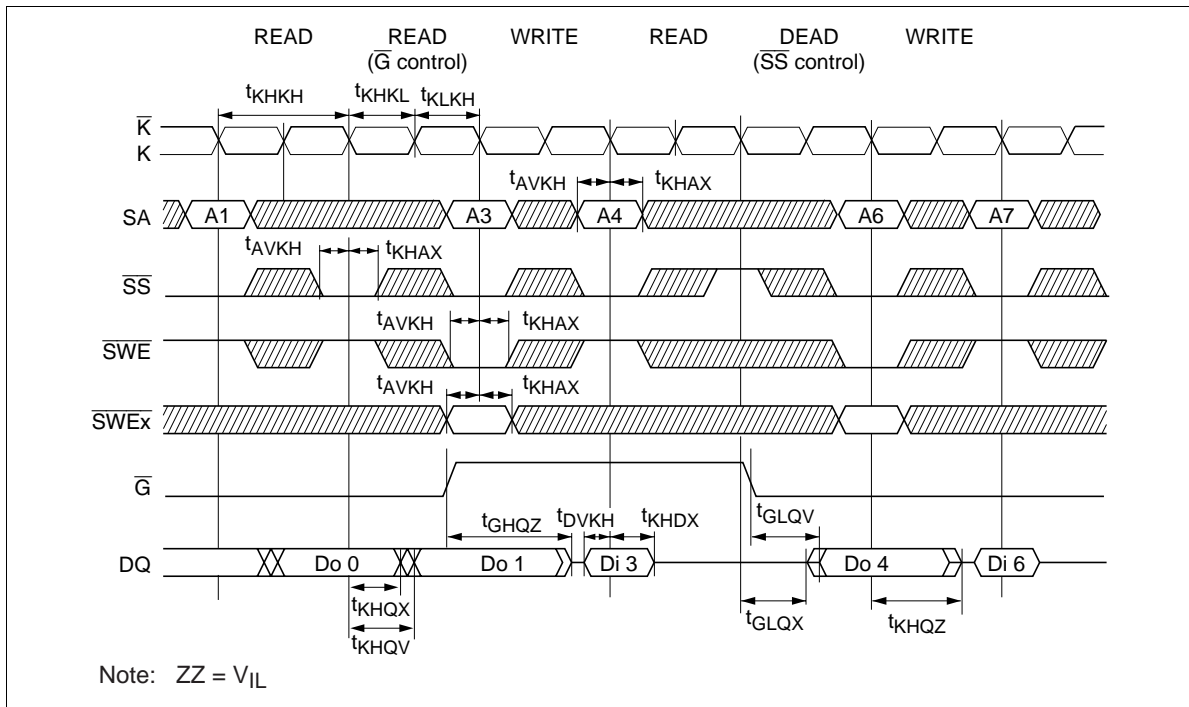


## Write Cycle

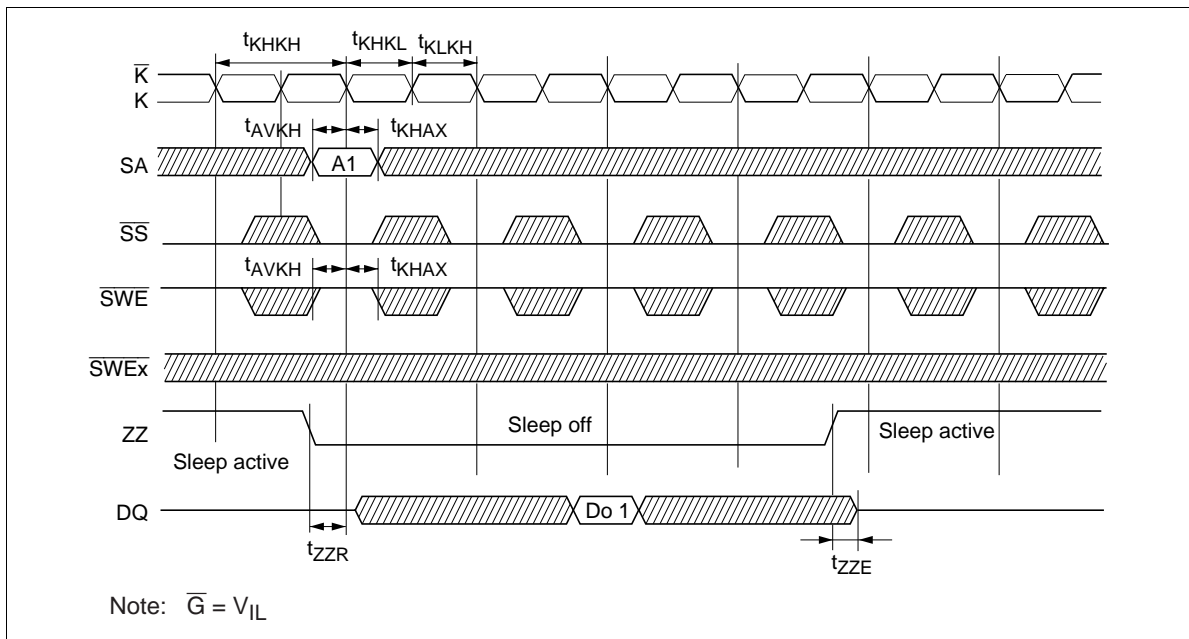


Note: ZZ =  $V_{IL}$

Read-Write Cycle



ZZ Control



## Boundary Scan Test Access Port Operations

In order to perform the interconnect testing of the modules that include this SRAM, the serial boundary scan test access port (TAP) is designed to operate in a manner consistent with IEEE Standard 1149.1 - 1990. But does not implement all of the functions required for 1149.1 compliance. The HM62Gxx series contains a TAP controller. Instruction register, Boundary scans register, Bypass register and ID register.

### Test Access Port Pins

Symbol I/O	Name
TCK	Test clock
TMS	Test mode select
TDI	Test data in
TDO	Test data out

Note: This Device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. To disable the TAP, TCK must be connected to  $V_{SS}$ . TDO should be left unconnected. To test Boundary scan, ZZ pin need to be kept below  $V_{REF} - 0.4$  V.

### TAP DC Operating Conditions ( $T_a = 0$ to $70^\circ\text{C}$ , $[T_j]_{\text{max}} = 110^\circ\text{C}$ )

Parameter	Symbol	Min	Max	Unit	Notes
Boundary scan input high voltage	$V_{IH}$	2.0	$V_{DD} + 0.3$	V	
Boundary scan input low voltage	$V_{IL}$	-0.5	0.8	V	
Boundary scan input leakage current	$I_{LI}$	-2	2	$\mu\text{A}$	1
Boundary scan output low voltage	$V_{OL}$	—	0.4	V	2
Boundary scan output high voltage	$V_{OH}$	2.4	—	V	3

Notes: 1.  $0 \leq V_{in} \leq V_{DD}$  for all logic input pin.  
2.  $I_{OL} = 8$  mA.  
3.  $I_{OH} = -8$  mA.



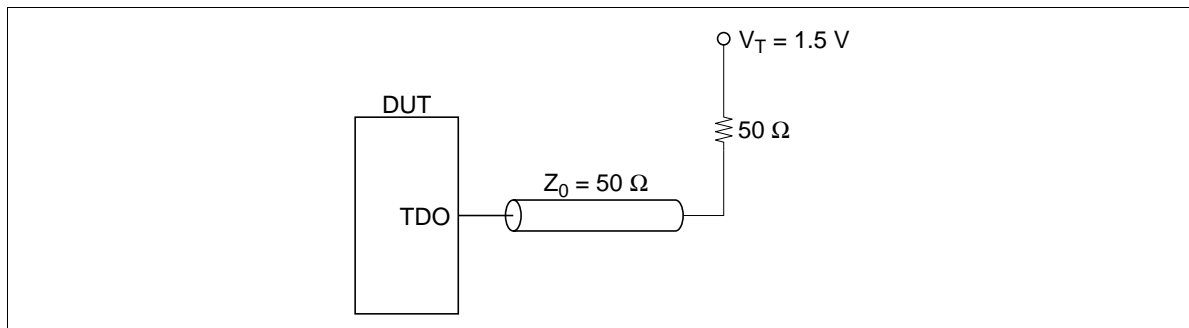
## TAP AC Characteristics (Ta = 0 to 70°C, [Tj] max = 110°C)

Parameter	Symbol	Min	Max	Unit	Note
Test clock cycle time	$t_{\text{THTH}}$	67	—	ns	
Test clock high pulse width	$t_{\text{THTL}}$	30	—	ns	
Test clock low pulse width	$t_{\text{TLTH}}$	30	—	ns	
Test mode select setup	$t_{\text{MVTH}}$	10	—	ns	
Test mode select hold	$t_{\text{THMX}}$	10	—	ns	
Capture setup	$t_{\text{CS}}$	10	—	ns	1
Capture hold	$t_{\text{CH}}$	10	—	ns	1
TDI valid to TCK high	$t_{\text{DVTH}}$	10	—	ns	
TCK high to TDI don't care	$t_{\text{THDX}}$	10	—	ns	
TCK low to TDO unknown	$t_{\text{TLQX}}$	0	—	ns	
TCK low to TDO valid	$t_{\text{TLQV}}$	—	20	ns	

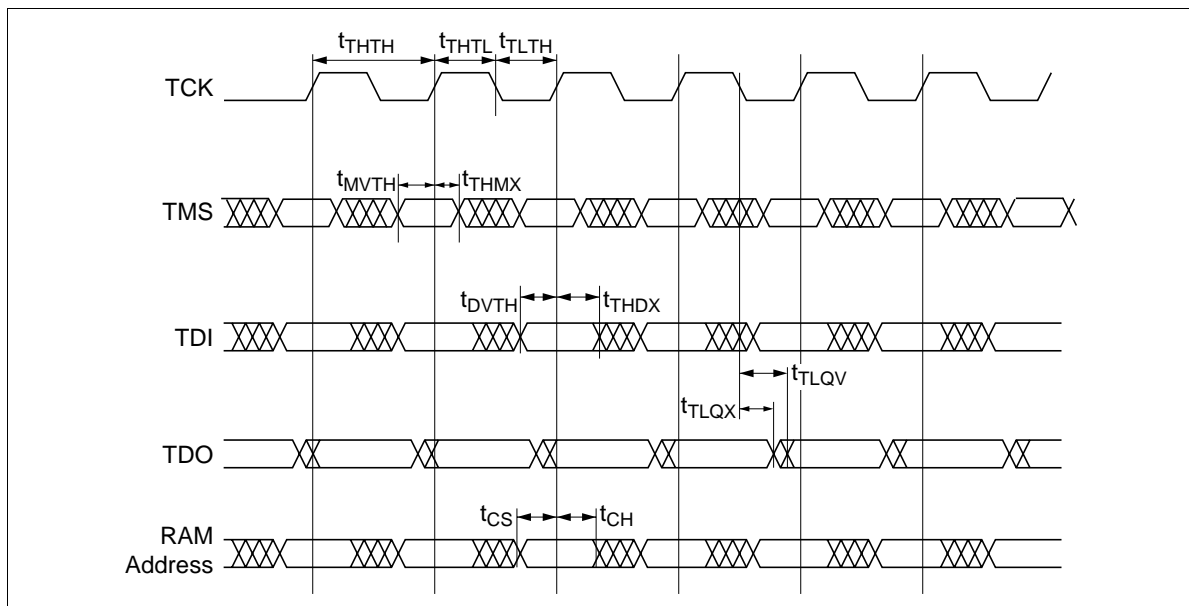
Note: 1.  $t_{\text{CS}} + t_{\text{CH}}$  defines the minimum pause in RAM I/O pad transitions to assure pad data capture.

## TAP Test Conditions

- Input pulse levels: 0 to 3.0 V
- Input and output timing reference levels: 1.5 V
- Input rise and fall time: 2 ns (10% to 90%) (typ)
- Output Load: See figure



## TAP Controller Timing Diagram



## Test Access Port Registers

Register name	Length	Symbol	Note
Instruction register	3 bits	IR [0;2]	
Bypass register	1 bit	BP	
ID register	32 bits	ID [0;31]	
Boundary scan register	51 bits	BS [1;51]	

**TAP Controller Instruction Set**

<b>IR2</b>	<b>IR1</b>	<b>IR0</b>	<b>Instruction</b>	<b>Operation</b>
0	0	0	SAMPLE-Z	Tristate all data drivers and capture the pad value
0	0	1	IDCODE	
0	1	0	SAMPLE-Z	Tristate all data drivers and capture the pad value
0	1	1	BYPASS	
1	0	0	SAMPLE	
1	0	1	BYPASS	
1	1	0	BYPASS	
1	1	1	BYPASS	

Note: This Device does not perform EXTEST, INTEST or the preload portion of the PRELOAD command in IEEE 1149.1.

# HM62G18512 Series

## Boundary Scan Order

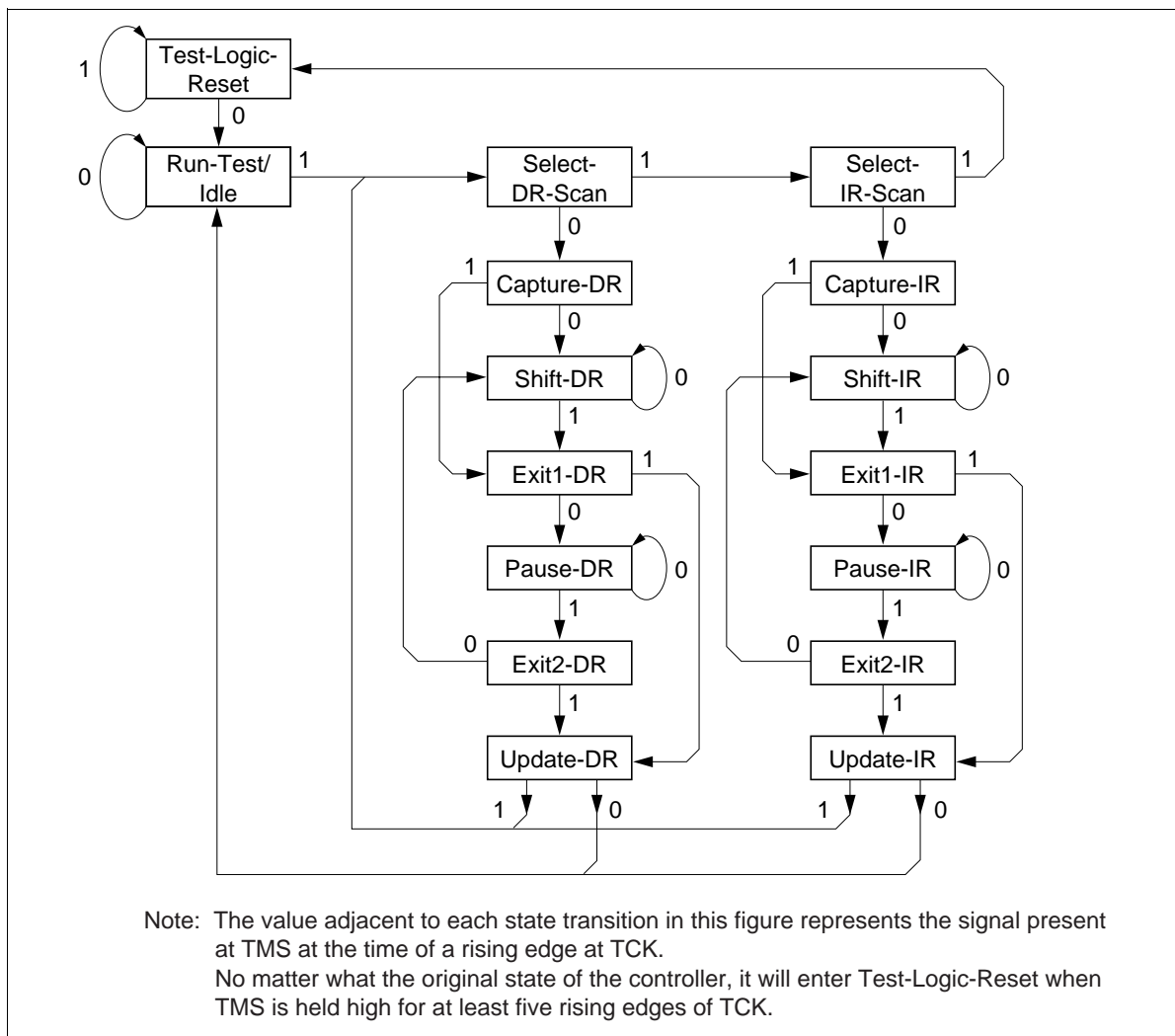
Bit No.	Bump ID	Signal name	Bit No.	Bump ID	Signal name
1	5R	M2	27	2B	NC
2	6T	SA15	28	3A	SA6
3	4P	SA14	29	3C	SA3
4	6R	SA10	30	2C	SA13
5	5T	SA12	31	2A	SA0
6	7T	ZZ	32	1D	DQb0
7	7P	DQa0	33	2E	DQb1
8	6N	DQa1	34	2G	DQb2
9	6L	DQa2	35	1H	DQb3
10	7K	DQa3	36	3G	$\overline{\text{SWEb}}$
11	5L	$\overline{\text{SWEa}}$	37	4D	ZQ
12	4L	$\overline{\text{K}}$	38	4E	$\overline{\text{SS}}$
13	4K	K	39	4G	NC
14	4F	$\overline{\text{G}}$	40	4H	NC
15	6H	DQa8	41	4M	$\overline{\text{SWE}}$
16	7G	DQa7	42	2K	DQb8
17	6F	DQa6	43	1L	DQb7
18	7E	DQa5	44	2M	DQb6
19	6D	DQa4	45	1N	DQb5
20	6A	SA2	46	2P	DQb4
21	6C	SA1	47	3T	SA11
22	5C	SA5	48	2R	SA9
23	5A	SA4	49	4N	SA16
24	6B	SA18	50	2T	SA17
25	5B	SA8	51	3R	M1
26	3B	SA7			

- Notes:
1. Bit number1 is the first scan bit to exit the chip.
  2. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a "Place Holder". Placeholder registers are internally connected to  $V_{SS}$ .
  3. In Boundary scan mode, differential input K and  $\overline{\text{K}}$  are referred to each other and must be at opposite logic levels for reliable operation.
  4. ZZ must remain at  $V_{IL}$  during boundary scan.
  5. In boundary scan mode, ZQ must be driven to  $V_{DDQ}$  or  $V_{SS}$  supply rail to ensure consistent results.
  6. M1 and M2 must be driven to  $V_{DD}$  or  $V_{SS}$  supply rail to ensure consistent results.

ID register

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	x	x	x	x	0	0	1	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
	Vendor Revision No.				Depth			Width			Use in the future				Vendor ID No.								Fix									

TAP Controller State Diagram

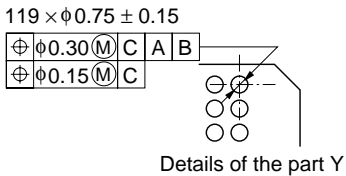
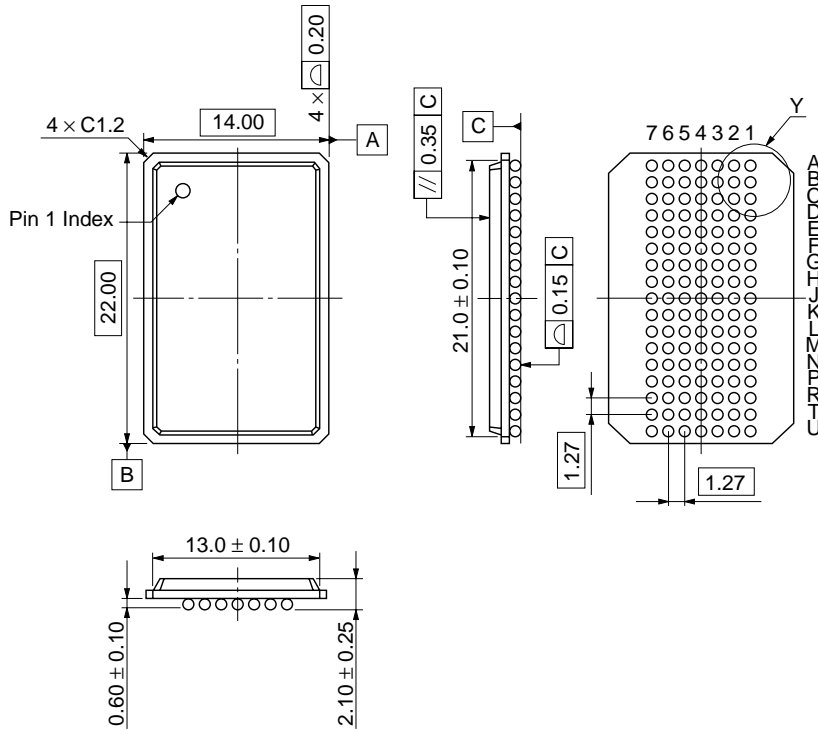
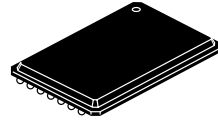


# HM62G18512 Series

## Package Dimensions

### HM62G18512BP Series (BP-119A)

Unit: mm



Hitachi Code	BP-119A
JEDEC	Conforms
EIAJ	—
Mass (reference value)	1.2 g

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# HITACHI

## Hitachi, Ltd.

Semiconductor & Integrated Circuits.  
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan  
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL	NorthAmerica	: <a href="http://semiconductor.hitachi.com/">http://semiconductor.hitachi.com/</a>
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### For further information write to:

Hitachi Semiconductor  
(America) Inc.  
179 East Tasman Drive,  
San Jose, CA 95134  
Tel: <1> (408) 433-1990  
Fax: <1>(408) 433-0223

Hitachi Europe GmbH  
Electronic Components Group  
Dornacher Straße 3  
D-85622 Feldkirchen, Munich  
Germany  
Tel: <49> (89) 9 9180-0  
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.  
Electronic Components Group.  
Whitebrook Park  
Lower Cookham Road  
Maidenhead  
Berkshire SL6 8YA, United Kingdom  
Tel: <44> (1628) 585000  
Fax: <44> (1628) 585160

Hitachi Asia Ltd.  
16 Collyer Quay #20-00  
Hitachi Tower  
Singapore 049318  
Tel: 535-2100  
Fax: 535-1533

Hitachi Asia Ltd.  
Taipei Branch Office  
3rd Flr, Hung Kuo Building, No.167,  
Tun Hwa North Road, Taipei (105)  
Taiwan  
Tel: <886> (2) 2718-3666  
Fax: <886> (2) 2718-8180  
Telex: 23222 HAS-TP

Hitachi Asia (Hong Kong) Ltd.  
Group III (Electronic Components)  
7th Flr, North Tower, World Finance Centre,  
Harbour City, Canton Road, Tsim Sha Tsui,  
Kowloon, Hong Kong  
Tel: <852> (2) 735 9218  
Fax: <852> (2) 730 0281  
Telex: 40815 HITEC HX

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