HMC154S8

GaAs MMIC SMT LOW DISTORTION T/R SWITCH, DC - 2.5 GHz

Typical Applications

The HMC154S8 is ideal for:

- MMDS & WirelessLAN
- Basestation Infrastructure
- Portable Wireless

Features

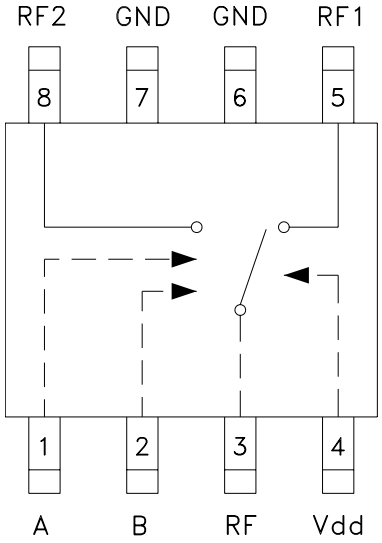
High Third Order Intercept: +60 dBm

Single Positive Supply: +3 to +10V

High RF Power Capability

TTL/CMOS Control

Functional Diagram



General Description

The HMC154S8 is a low-cost SPDT switch in an 8-lead SOIC package for use in transmit-receive applications which require very low distortion at high signal power levels. The device can control signals from DC to 2.5 GHz and is especially suited for 900 MHz and 1.8 - 2.2 GHz applications. The design provides exceptional inter-modulation performance; providing a +60dBm third order intercept at 8 Volt bias. RF1 and RF2 are reflective shorts when "Off". On-chip circuitry allows single positive supply operation at very low DC current with control inputs compatible with CMOS and most TTL logic families.

Electrical Specifications, T_A = +25° C, Vdd = +5 Vdc, 50 Ohm System

Parameter		Frequency	Min.	Typ.	Max.	Units
Insertion Loss		DC - 1.0 GHz DC - 2.0 GHz DC - 2.5 GHz		0.5 0.7 1.0	0.7 0.9 1.3	dB dB dB
Isolation		DC - 1.0 GHz DC - 2.0 GHz DC - 2.5 GHz	22 19 15	25 22 18		dB dB dB
Return Loss		DC - 1.0 GHz DC - 2.0 GHz DC - 2.5 GHz	20 14 10	30 18 13		dB dB dB
Input Power for 1 dB Compression	0/8V Control	0.5 - 1.0 GHz 0.5 - 2.0 GHz	35 34	39 38		dBm dBm
Input Third Order Intercept	0/8V Control	0.5 - 1.0 GHz 0.5 - 2.0 GHz	55 54	60 60		dBm dBm
Switching Characteristics	 tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)	DC - 2.5 GHz		 10 24		 ns ns

For price, delivery, and to place orders, please contact Hittite Microwave Corporation:
12 Elizabeth Drive, Chelmsford, MA 01824 Phone: 978-250-3343 Fax: 978-250-3373
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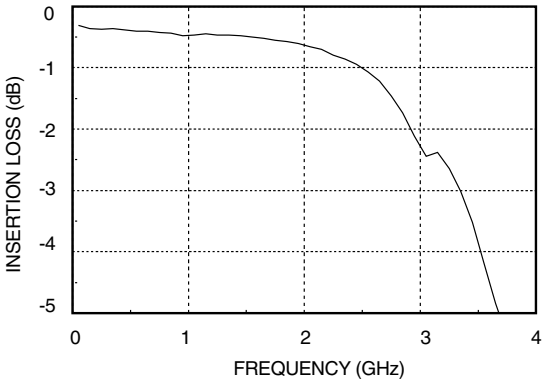
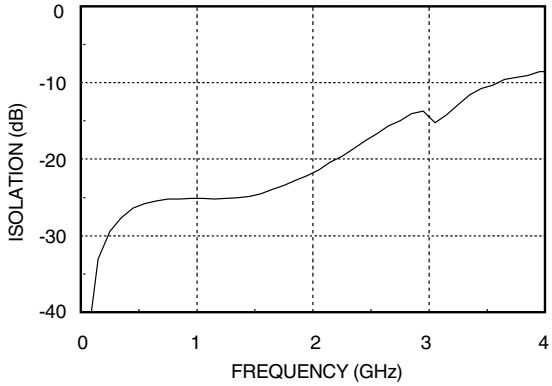
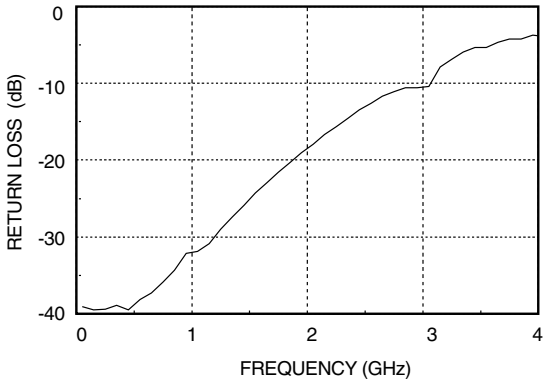
Insertion Loss



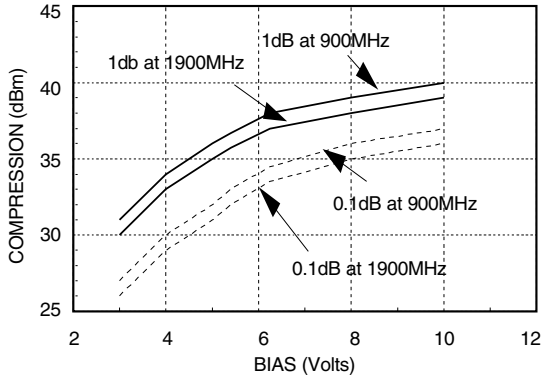
Isolation



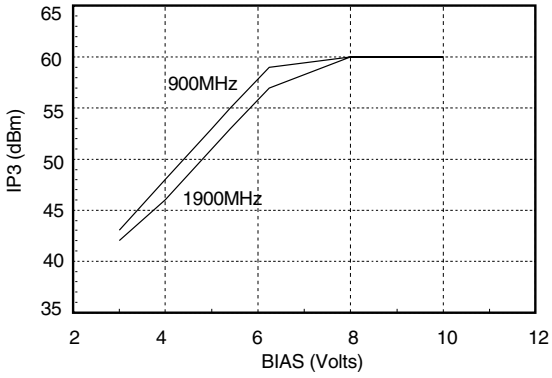
Return Loss



Input Power for 0.1 and 1.0 dB Compression vs. Bias Voltage



Input Third Order Intercept vs. Bias Voltage



Compression vs. Bias Voltage

	Carrier at 900 MHz		Carrier at 1900 MHz	
Bias Vdd	Input Power for 0.1 dB Compression	Input Power for 1.0 dB Compression	Input Power for 0.1 dB Compression	Input Power for 1.0 dB Compression
(Volts)	(dBm)	(dBm)	(dBm)	(dBm)
3	27	31	26	30
4	30	34	29	33
5	32	36	31	35
8	36	39	35	38
10	37	40	36	39

Caution: Do not operate in 1dB compression at power levels above +35dBm and do not "hot switch" power levels greater than +23dBm (Vdd = +5V).

Distortion vs. Bias Voltage

	1 Watt Carrier at 900 MHz			1 Watt Carrier at 1900 MHz		
Bias Vdd	Third Order Intercept	Second Order Intercept	Second Harmonic	Third Order Intercept	Second Order Intercept	Second Harmonic
(Volts)	(dBm)	(dBm)	(dBc)	(dBm)	(dBm)	(dBc)
3	43	71	45	42	78	55
4	48	85	55	46	88	65
5	53	90	56	51	87	58
8	60	90	58	60	90	59
10	60	90	59	60	90	60

Truth Table

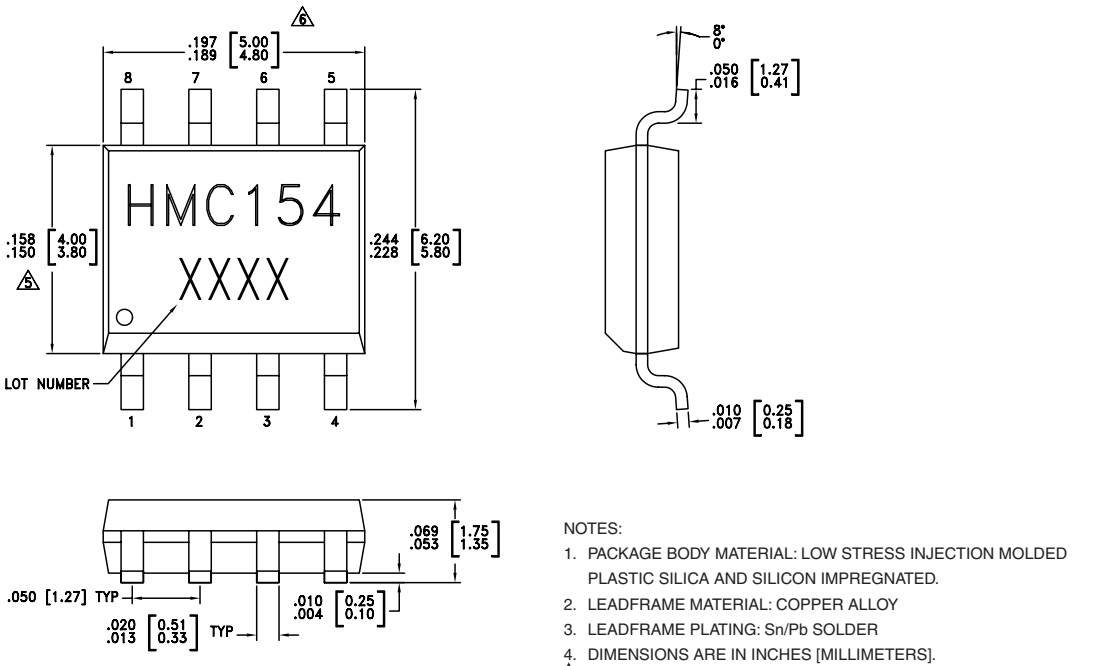
***Control Input Voltage Tolerances are ± 0.2 Vdc.**

Bias	Control Input*		Bias Current	Control Current	Control Current	Signal Path State	
Vdd (Vdc)	A (Vdc)	B (Vdc)	Idd (uA)	Ia (uA)	Ib (uA)	RF to RF1	RF to RF2
3	0	0	30	-15	-15	OFF	OFF
3	0	Vdd	25	-25	0	ON	OFF
3	Vdd	0	25	0	-25	OFF	ON
5	0	0	110	-55	-55	OFF	OFF
5	0	Vdd	115	-100	-15	ON	OFF
5	Vdd	0	115	-15	-100	OFF	ON
10	0	0	380	-190	-190	OFF	OFF
10	0	Vdd	495	-275	-220	ON	OFF
10	Vdd	0	495	-220	-275	OFF	ON
5	-Vdd	Vdd	600	-600	225	ON	OFF
5	Vdd	-Vdd	600	225	-600	OFF	ON

Absolute Maximum Ratings

Bias Voltage Range (Vdd)	-0.2 to +12 Vdc
Control Voltage Range (A & B)	-0.2 to Vdd Vdc
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

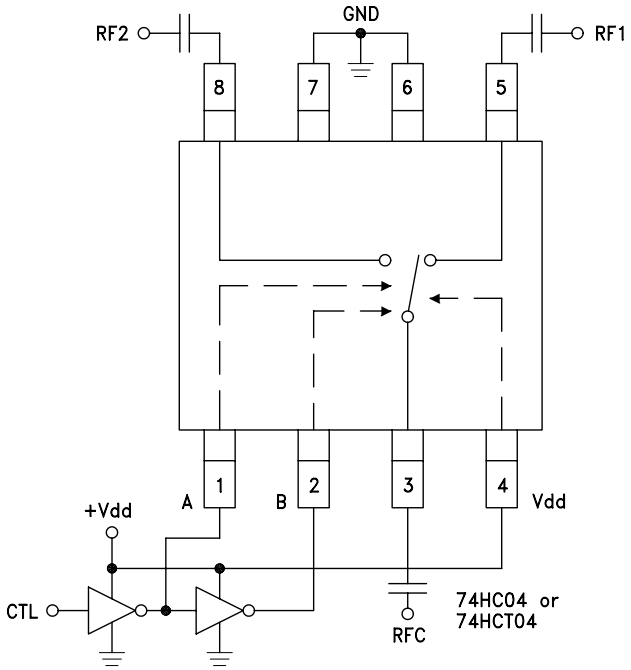
Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEADFRAME MATERIAL: COPPER ALLOY
3. LEADFRAME PLATING: Sn/Pb SOLDER
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
6. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
7. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.

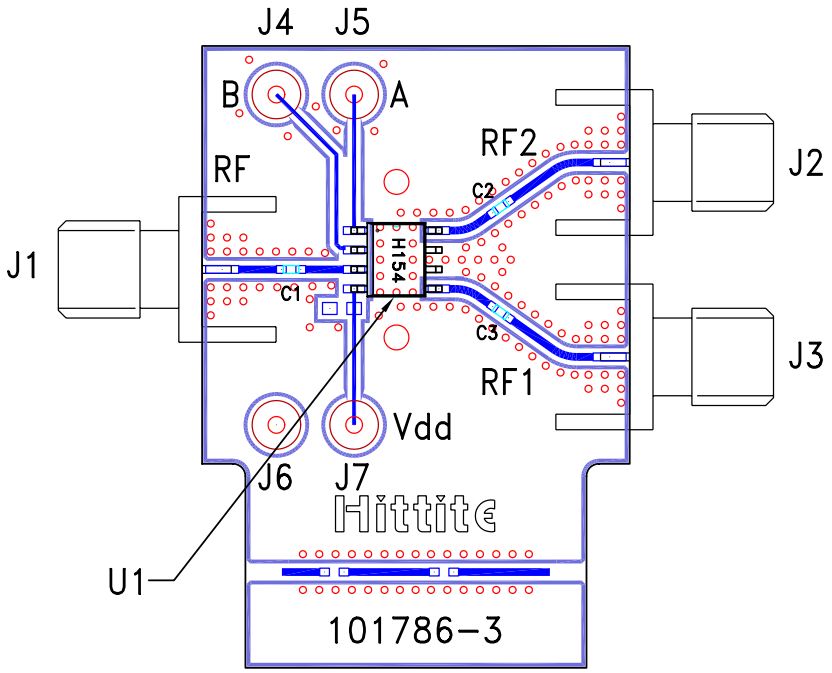
Typical Application Circuit



Notes:

1. Set logic gate and switch Vdd = +3V to +5V and use HCT series logic to provide a TTL driver interface.
2. Control inputs A/B can be driven directly with CMOS logic (HC) with Vdd of 3 to 8 Volts applied to the CMOS logic gates and to pin 4 of the RF switch.
3. DC Blocking capacitors are required for each RF port as shown. Capacitor value determines lowest frequency of operation.
4. Highest RF signal power capability is achieved with V set to +10V. The switch will operate properly (but at lower RF power capability) at bias voltages down to +3V.

Evaluation Circuit Board



List of Material

Item	Description
J1 - J3	PC Mount SMA RF Connector
J4 - J7	DC Pin
C1 - C3	330 pF Capacitor, 0402 Pkg.
U1	HMC154S8 SPDT Switch
PCB*	101786 Evaluation PCB
* Circuit Board Material: Rogers 4350	

The circuit board used in the final application should be generated with proper RF circuit design techniques. Signal lines at the RF port should have 50 ohm impedance and the package ground leads and package bottom should be connected directly to the ground plane similar to that shown above. The evaluation circuit board shown above is available from Hittite Microwave Corporation upon request.