64Mbyte(4Mx144) 200-pin ECC Mode 4K Ref. DIMM Design 5V

Part No. HMD4M144D9WG

GENERAL DESCRIPTION

The HMD4M144D9WG is a 4Mbit x 144bit dynamic RAM high-density memory module. The module consists of eight CMOS 4Mx16bit DRAMs in 50-pin TSOP packages and one CMOS 4M x 16bit DRAM in 50pin TSOP package mounted on a 200-pin, double-sided, FR-4-printed circuit board. A 0.1uF or 4.7uF decoupling capacitor is mounted on the printed circuit board for each DRAM components.

The module is a dual In-line memory module with edge connections and is intended for mounting in to 200-pin edge connector sockets. All module components may be powered from a single 5V DC power supply and all inputs and outputs are TTL-compatible.

FEATURES

- Access times : 50, 60 ns
- High -density 64MByte design
- Part identification
  - HMD4M144D9WG (4K Cycles/64ms Ref, Gold)
- Single +5V ± 0.5V power supply
- JEDEC Standard pinout
- ECC mode operation
- TTL compatible inputs and output

OPTIONS	MARKING
Timing	
50ns access	-5
60ns access	-6
Packages	
200-pin DIMM	D

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns

PIN NAMES

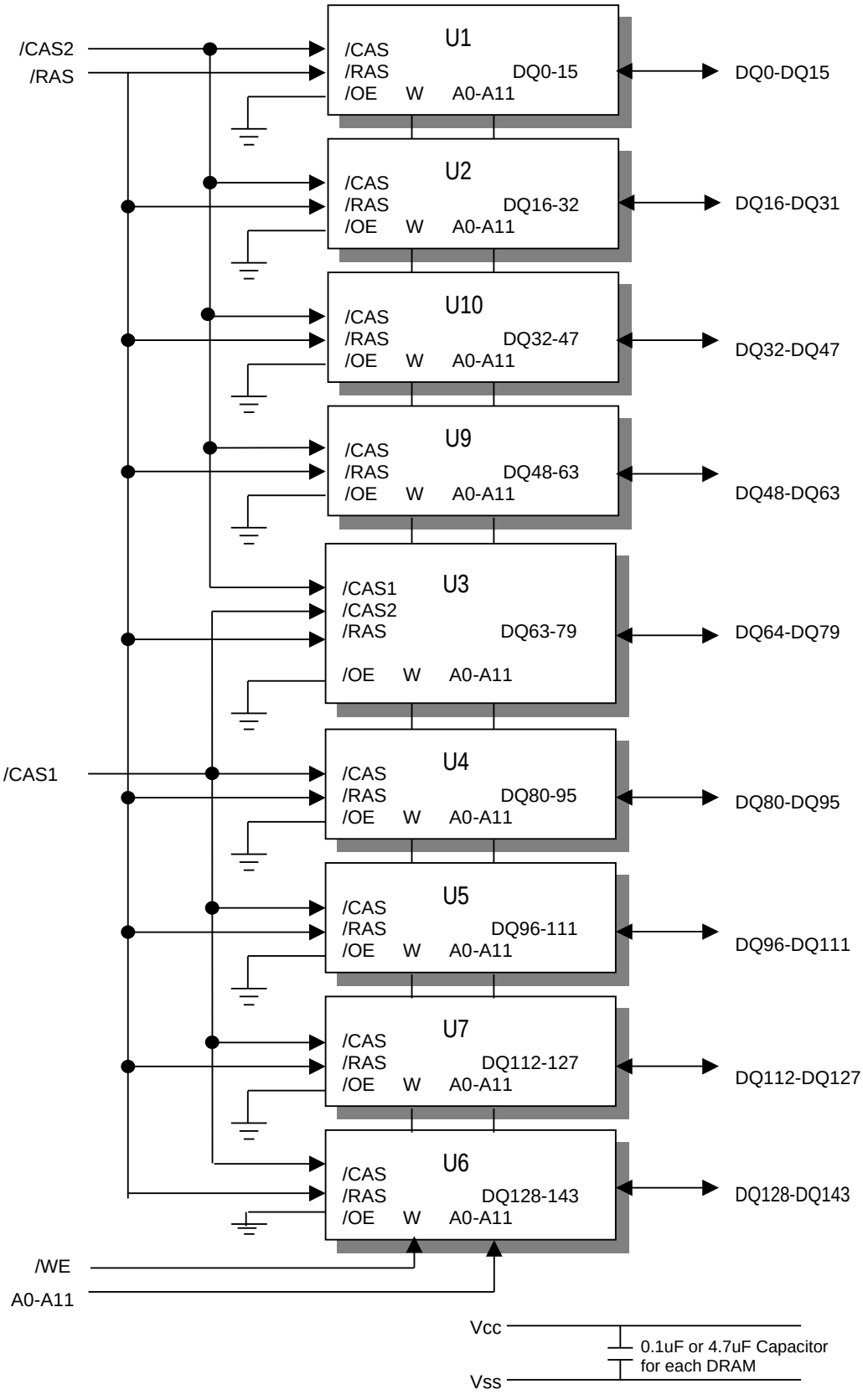
Pin Name	Function	Pin Name	Function	Pin Name	Function
BA0-BA11	Address Input	BRAS	Row Address Strobe	Vss	Ground
DQ0-DQ143	Data In/Out	BCAS1,BCAS2	Column Address Strobe	NC	No Connection
BWE	Read/Write Enable	Vcc	Power(+5V)		

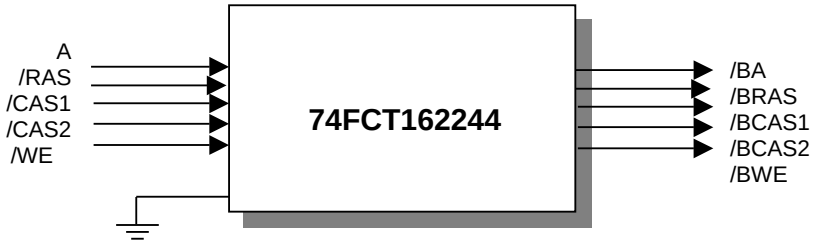
PIN ASSIGNMENT

PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol
1	Vss	35	DQ14	69	DQ29	101	Vss	135	Vss	169	DQ94
2	Vss	36	DQ50	70	DQ65	102	Vss	136	Vss	170	DQ130
3	DQ0	37	DQ15	71	DQ30	103	BA6	137	DQ80	171	DQ95
4	DQ36	38	DQ51	72	DQ66	104	BA7	138	DQ116	172	DQ131
5	DQ1	39	DQ16	73	DQ31	105	BA8	139	DQ81	173	DQ96
6	DQ37	40	DQ52	74	DQ67	106	BA9	140	DQ117	174	DQ132
7	DQ2	41	DQ17	75	DQ32	107	BA10	141	DQ82	175	DQ97
8	DQ38	42	DQ53	76	DQ68	108	BA11	142	DQ118	176	DQ133
9	DQ3	43	DQ18	77	DQ33	109	NC	143	DQ83	177	DQ98
10	DQ39	44	DQ54	78	DQ69	110	/BWE	144	DQ119	178	DQ134
11	DQ4	45	DQ19	79	DQ34	111	NC	145	DQ84	179	DQ99
12	DQ40	46	DQ55	80	DQ70	112	NC	146	DQ120	180	DQ135
13	DQ5	47	DQ20	81	Vcc	113	Vss	147	DQ85	181	DQ100
14	DQ41	48	DQ56	82	Vcc	114	Vss	148	DQ121	182	DQ136
15	DQ6	49	Vcc	83	DQ35	115	Vss	149	DQ86	183	Vcc
16	DQ42	50	Vcc	84	DQ71	116	Vss	150	DQ122	184	Vcc
17	Vcc	51	DQ21	85	/BCAS1	117	DQ72	151	Vcc	185	DQ101
18	Vcc	52	DQ57	86	/BCAS2	118	DQ108	152	Vcc	186	DQ137
19	DQ7	53	DQ22	87	/BRAS	119	Vcc	153	DQ87	187	DQ102
20	DQ43	54	DQ58	88	NC	120	Vcc	154	DQ123	188	DQ138
21	DQ8	55	DQ23	89	NC	121	DQ73	155	DQ88	189	DQ103
22	DQ44	56	DQ59	90	NC	122	DQ109	156	DQ124	190	DQ139
23	DQ9	57	DQ24	91	NC	123	DQ74	157	DQ89	191	DQ104
24	DQ45	58	DQ60	92	NC	124	DQ110	158	DQ125	192	DQ140
25	DQ10	59	DQ25	93	BA0	125	DQ75	159	DQ90	193	DQ105
26	DQ46	60	DQ61	94	BA1	126	DQ111	160	DQ126	194	DQ141
27	DQ11	61	DQ26	95	BA2	127	DQ76	161	DQ91	195	DQ106
28	DQ47	62	DQ62	96	BA3	128	DQ112	162	DQ127	196	DQ142
29	DQ12	63	DQ27	97	BA4	129	DQ77	163	DQ92	197	DQ107
30	DQ48	64	DQ63	98	BA5	130	DQ113	164	DQ128	198	DQ143
31	DQ13	65	Vss	99	Vss	131	DQ78	165	DQ93	199	Vss
32	DQ49	66	Vss	100	Vss	132	DQ114	166	DQ129	200	Vss
33	Vss	67	DQ28			133	DQ79	167	Vss		
34	Vss	68	DQ64			134	DQ115	168	Vss		

200PIN DIMM TOP VIEW

FUNCTIONAL BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-1V to 7.0V
Voltage on Vcc Supply Relative to Vss	Vcc	-1V to 7.0V
Power Dissipation	P_D	9W
Storage Temperature	T_{STG}	-55^{o}C to 150^{o}C
Short Circuit Output Current	I_{OS}	50mA

w Permanent device damage may occur if " Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(Voltage reference to V_{SS}, T_A=0 to 70 ^{o} C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V

DC AND OPERATING CHARACTERISTICS

SYMBOL	SPEED	MIN	MAX	UNITS
I_{CC1}	-5	-	396	mA
	-6	-	366	mA
I_{CC2}	Don't care	-	12	mA
I_{CC3}	-5	-	396	mA
	-6	-	366	mA
I_{CC4}	-5	-	396	mA
	-6	-	366	mA
I_{CC5}	Don't care	-	6	mA
I_{CC6}	-5	-	990	mA
	-6	-	900	mA

$I_{I(L)}$		-60	40	μA
$I_{O(L)}$		-5	5	μA
V_{OH}		2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * (/RAS , /CAS , Address cycling @t_{RC}=min.)

I_{CC2} : Standby Current (/RAS=/CAS=V_{IH})

I_{CC3} : /RAS Only Refresh Current * (/CAS=V_{IH}, /RAS, Address cycling @t_{RC}=min)

I_{CC4} : Fast Page Mode Current * (/RAS=V_{IL}, /CAS, Address cycling @t_{PC}=min)

I_{CC5} : Standby Current (/RAS=/CAS=Vcc-0.2V)

I_{CC6} : /CAS-Before-/RAS Refresh Current * (/RAS and /CAS cycling @t_{RC}=min)

I_{IL} : Input Leakage Current (Any input 0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)

I_{OL} : Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V

V_{OH} : Output High Voltage Level (I_{OH}= -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address cad be changed maximum once while /RAS=V_{IL}. In I_{CC4}, address can be changed maximum once within one page mode cycle.

CAPACITANCE (T_A=25°C, Vcc = 5V, f = 1Mz)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Input Capacitance (A0-A11)	C_{IN1}	-	65	pF
Input Capacitance (/WE)	C_{IN2}	-	80	pF
Input Capacitance (/RAS0)	C_{IN3}	-	50	pF
Input Capacitance (/CAS1-/CAS2)	C_{IN4}	-	40	pF
Input/Output Capacitance (DQ0-31)	C_{DO1}	-	20	pF

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C , Vcc = 5V±10%, See notes 1,2.)

STANDARD OPERATION	SYMBOL	-5		-6		UNIT
		MIN	MAX	MIN	MAX	
Random read or write cycle time	t_{RC}	110		130		ns
Access time from /RAS	t_{RAC}		50		60	ns
Access time from /CAS	t_{CAC}		15		20	ns
Access time from column address	t_{AA}		30		35	ns
/CAS to output in Low-Z	t_{CLZ}	0		0		ns
Output buffer turn-off delay	t_{OFF}	0	15	0	20	ns
Transition time (rise and fall)	t_T	3	50	3	50	ns

/RAS precharge time	t_{RP}	40		50		ns
/RAS pulse width	t_{RAS}	60	10K	70	10K	ns
/RAS hold time	t_{RSH}	15		20		ns
/CAS hold time	t_{CSH}	60		70		ns
/CAS pulse width	t_{CAS}	15	10K	20	10K	ns
/RAS to /CAS delay time	t_{RCD}	20	45	20	50	ns
/RAS to column address delay time	t_{RAD}	15	30	15	35	ns
/CAS to /RAS precharge time	t_{CRP}	5		5		ns
Row address set-up time	t_{ASR}	0		0		ns
Row address hold time	t_{RAH}	10		10		ns
Column address set-up time	t_{ASC}	0		0		ns
Column address hold time	t_{CAH}	15		15		ns
Column address hold referenced to /RAS	t_{AR}	50		55		ns
Column Address to /RAS lead time	t_{RAL}	30		35		ns
Read command set-up time	t_{RCS}	0		0		ns
Read command hold referenced to /CAS	t_{RCH}	0		0		ns
Read command hold referenced to /RAS	t_{RRH}	0		0		ns
Write command hold time	t_{WCH}	15		15		ns
Write command hold referenced to /RAS	t_{WCR}	50		55		ns
Write command pulse width	t_{WP}	15		15		ns
Write command to /RAS lead time	t_{RWL}	15		20		ns
Write command to /CAS lead time	t_{CWL}	15		20		ns
Data-in set-up time	t_{DS}	0		0		ns
Data-in hold time	t_{DH}	15		15		ns
Data-in hold referenced to /RAS	t_{DHR}	50		55		ns
Refresh period	t_{REF}		16		16	ns
Write command set-up time	t_{WCS}	0		0		ns
/CAS setup time (C-B-R refresh)	t_{CSR}	10		10		ns

/CAS hold time (C-B-R refresh)	t_{CHR}	15		15		ns
/RAS precharge to /CAS hold time	t_{RPC}	5		5		ns
Access time from /CAS precharge	t_{CPA}		35		40	ns
Fast page mode cycle time	t_{PC}	40		45		ns
/CAS precharge time (Fast page)	t_{CP}	10		10		ns
/RAS pulse width (Fast page)	t_{RASP}	60	100K	70	100K	ns
/W to /RAS precharge time (C-B-R refresh)	t_{WRP}	10		10		ns
/W to /RAS hold time (C-B-R refresh)	t_{WRH}	10		10		ns
/CAS precharge(C-B-R counter test)	t_{CPT}	20		30		ns

NOTES

1.An initial pause of 200μs is required after power-up followed by any 8 /RAS-only or /CAS-before-/RAS refresh cycles before proper device operation is achieved.

2.$V_{IH\ (min)}$ and $V_{IL\ (max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$ and are assumed to be 5ns for all inputs.

3.Measured with a load equivalent to 2TTL loads and 100pF

4.Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.

5.Assumes that $t_{RCD} \geq t_{RCD(max)}$

6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$

7.This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

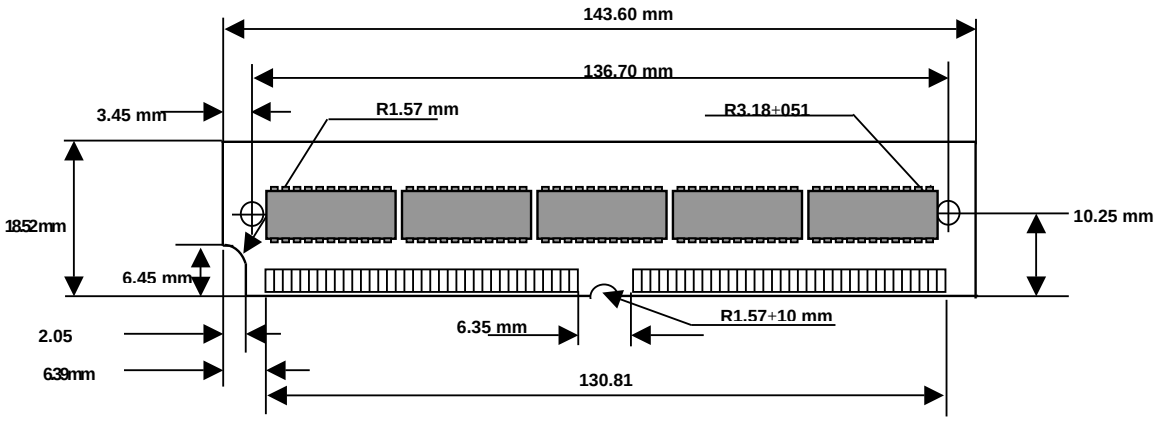
8. t_{WCS}, t_{RWD}, t_{CWD} anf t_{AWD} are non restrictive operating parameter.
They are included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

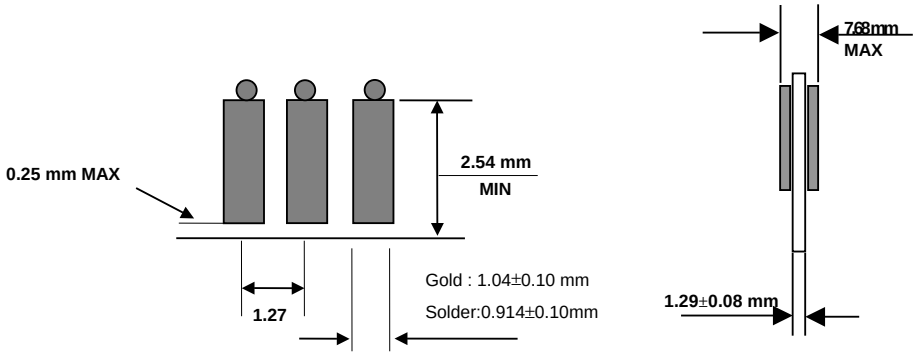
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

10. These parameters are referenced to the CAS leading edge in early write cycles and to the W leading edge in read-write cycles.

11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit. then access time is controlled by t_{AA}.

PACKAGING INFORMATION





ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	MODE	SPEED
HMD4M144D9WG-5	64MByte	x 144	200 Pin-DMM	9EA	5V	ECC	50ns
HMD4M144D9WG-6	64MByte	x 144	200 Pin-DIMM	9EA	5V	ECC	60ns