SRAM MODULE 512KByte (128K x 32-Bit), 64PIN SIMM / ZIP

Part No. HMS12832M4G, HMS12832Z4

GENERAL DESCRIPTION

The HMS12832M4G/Z4 is a high-speed static random access memory (SRAM) module containing 131,072 words organized in a x32-bit configuration. The module consists of four 128K x 8 SRAMs mounted on a 64-pin, single-sided, FR4-printed circuit board.

PD0 and PD1 identify the module's density allowing interchangeable use of alternate density, industry- standard modules. Four chip enable inputs, (/CE1, /CE2, /CE3 and /CE4) are used to enable the module's 4 bytes independently. Output enable(/OE) and write enable(/WE) can set the memory input and output.

Data is written into the SRAM memory when write enable (/WE) and chip enable (/CE) inputs are both LOW. Reading is accomplished when /WE remains HIGH and /CE and output enable (/OE) are LOW.

For reliability, this SRAM module is designed as multiple power and ground pin. All module components may be powered from a single +5V DC power supply and all inputs and outputs are fully TTL-compatible.

FEATURES

- Access times : 10, 12, 15 and 20ns
- High-density 512KByte design
- High-reliability, high-speed design
- Single + 5V ±0.5V power supply
- Easy memory expansion with /CE and /OE functions
- All inputs and outputs are TTL-compatible
- Industry-standard pinout
- FR4-PCB design

OPTIONS MARKING

- Timing

8ns access	- 8
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20

- Packages

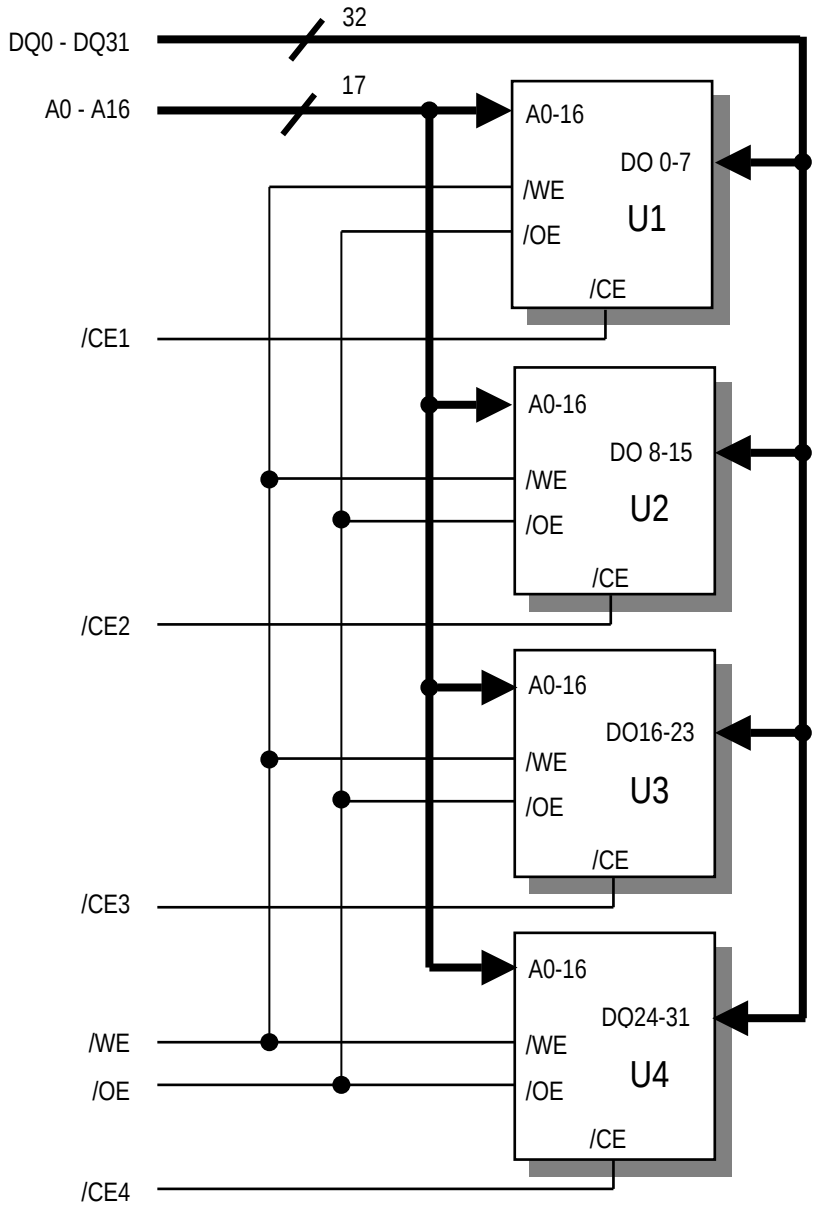
64-pin SIMM	M
64-pin ZIP	Z

PIN ASSIGNMENT

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	17	A2	33	/CE4	49	A4
2	NC	18	A9	34	/CE3	50	A11
3	NC	19	DQ12	35	NC	51	A5
4	DQ0	20	DQ4	36	A16	52	A12
5	DQ8	21	DQ13	37	/OE	53	Vcc
6	DQ1	22	DQ5	38	Vss	54	A13
7	DQ9	23	DQ14	39	DQ24	55	A6
8	DQ2	24	DQ6	40	DQ16	56	DQ20
9	DQ10	25	DQ15	41	DQ25	57	DQ28
10	DQ3	26	DQ7	42	DQ17	58	DQ21
11	DQ11	27	Vss	43	DQ26	59	DQ29
12	Vcc	28	/WE	44	DQ18	60	DQ22
13	A0	29	A15	45	DQ27	61	DQ30
14	A7	30	A14	46	DQ19	62	DQ23
15	A1	31	/CE2	47	A3	63	DQ31
16	A8	32	/CE1	48	A10	64	Vss

SIMM
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



PRESENCE-DETECT

PD0 = Open

PD1 = Open

TRUTH TABLE

MODE	/OE	/CE	/WE	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
READ	L	L	H	Dout	ACTIVE
WRITE	X	L	L	Din	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5V to Vcc+0.5V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5V to +7.0V
Power Dissipation	P_D	4.0W
Storage Temperature	T_{STG}	-65°C to +150°C
Operating Temperature	T_A	0°C to +70°C

w Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

PARAMETER	SYMBOL	MIN	TYP.	MAX
Supply Voltage	V_{CC}	4.5V	5.0V	5.5V
Ground	V_{SS}	0	0	0
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5V**
Input Low Voltage	V_{IL}	-0.5*	-	0.8V

* V_{IL}(Min.) = -2.0V ac (Pulse Width ≤ 10ns) for I ≤ 20 mA

****** V_{IH}(Min.) = Vcc+2.0V ac (Pulse Width ≤ 10ns) for I ≤ 20 mA

DC AND OPERATING CHARACTERISTICS (1)(0°C ≤ T_A ≤ 70 °C ; Vcc = 5V ± 10%)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNITS
Input Leakage Current	VIN=Vss to Vcc	IL_I	-8	8	µA
Output Leakage Current	/CE=V_{IH} or /OE =V_{IH} or /WE=V_{IL} V_{OUT}=Vss to V_{CC}	IL_0	-8	8	µA
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V

* Vcc=5.0V, Temp=25 °C

DC AND OPERATING CHARACTERISTICS (2)

DESCRIPTION	TEST CONDITIONS	SYMBOL	MAX			UNIT
			-12	-15	-20	
Power Supply Current:Operating	Min. Cycle, 100% Duty /CE=V_{IL}, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA	I_{CC}	300	292	280	mA
Power Supply Current:Standby	Min. Cycle, /CE=V_{IH}	I_{SB}	120	120	120	mA
	f=0MHZ, /CE≥V_{CC}-0.2V, V_{IN}≥ V_{CC}-0.2V or V_{IN}≤0.2V	I_{SB1}	20	20	20	mA

CAPACITANCE (T_A =25 ^oC , f= 1.0Mhz)

DESCRIPTION	TEST CONDITIONS	SYMBOL	MAX	UNIT
Input /Output Capacitance	$V_{I/O}$=0V	$C_{I/O}$	32	pF
Input Capacitance	V_{IN}=0V	C_{IN}	24	pF

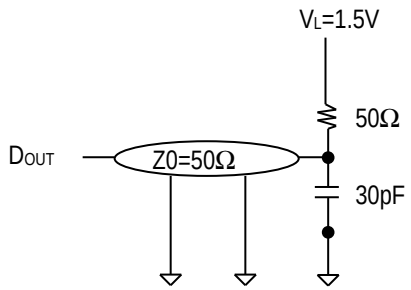
* NOTE : Capacitance is sampled and not 100% tested

AC CHARACTERISTICS ($0^oC \le T_A \le 70\ ^oC$; Vcc = 5V ± 0.5V, unless otherwise specified)

Test conditions

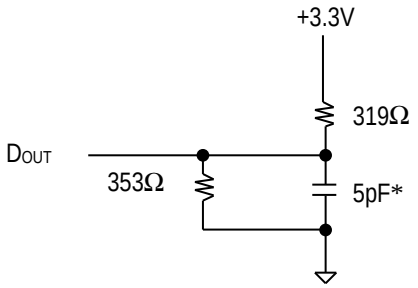
PARAMETER	VALUE
Input Pulse Level	0V to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)

for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ}



READ CYCLE

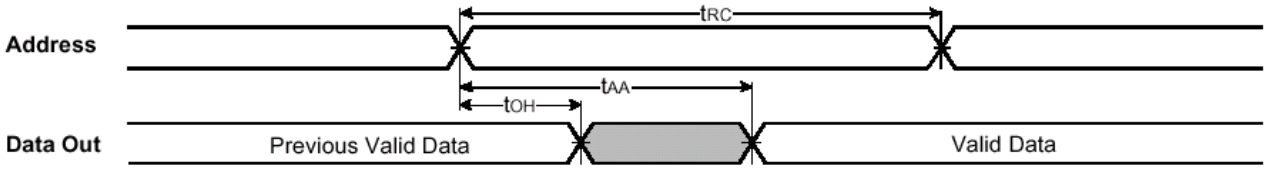
PARAMETER	SYMBOL	-12		-15		-20		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC}	12		15		20		ns
Address Access Time	t_{AA}		12		15		20	ns
Chip Select to Output	t_{CO}		12		15		20	ns
Output Enable to Output	t_{OE}		6		7		9	ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		ns
Chip Enable to Low-Z Output	t_{LZ}	3		3		3		ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	9	ns
Chip Disable to High-Z Output	t_{HZ}	0	6	0	7	0	9	ns
Output Hold from Address Change	t_{OH}	3		3		3		ns
Chip Select to Power Up Time	t_{PU}	0		0		0		ns
Chip Select to Power Down Time	t_{PD}	-	12		15		20	ns

WRITE CYCLE

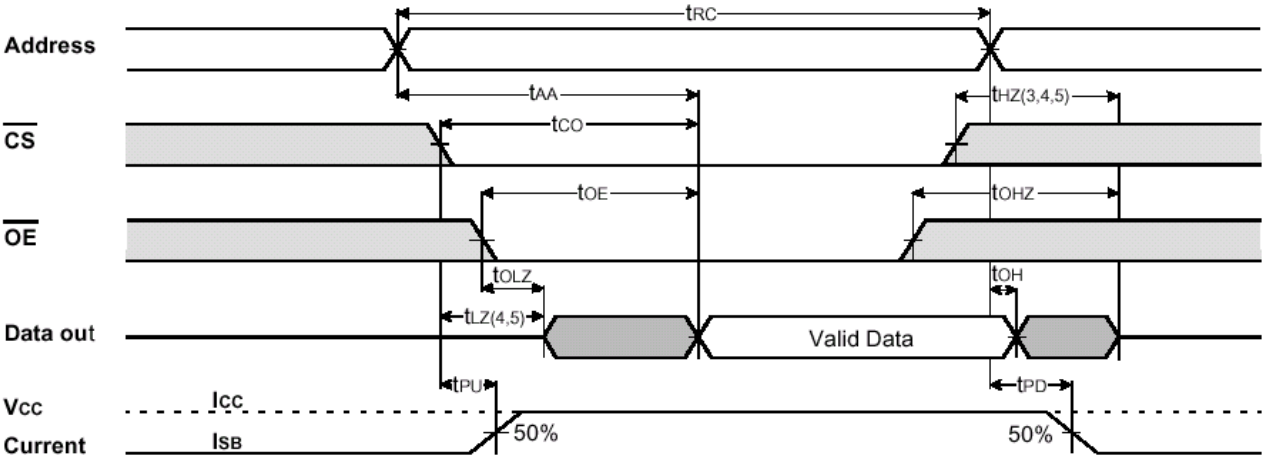
PARAMETER	SYMBOL	-12		-15		-20		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Write Cycle Time	t_{WC}	12		15		20		ns
Chip Select to End of Write	t_{CW}	8		10		12		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	8		9		10		ns
Write Pulse Width	t_{WP}	8		9		10		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WHZ}	0	6	0	7	0	9	ns
Data to Write Time Overlap	t_{DW}	6		7		8		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End of Write to Output Low-Z	t_{OW}	3		3		3		ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



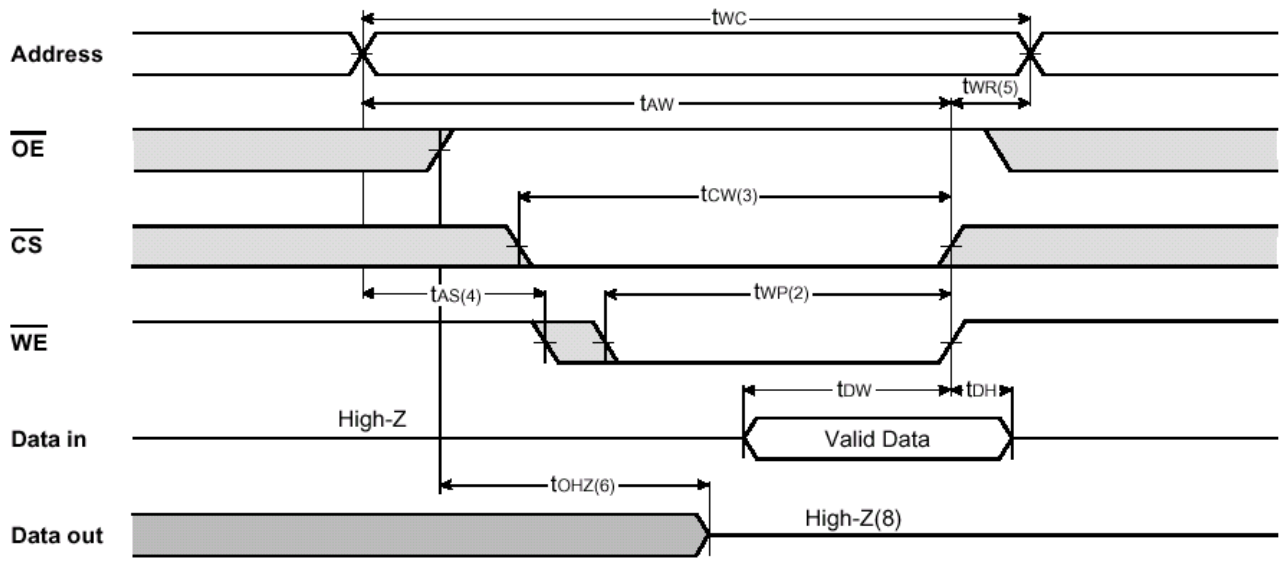
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



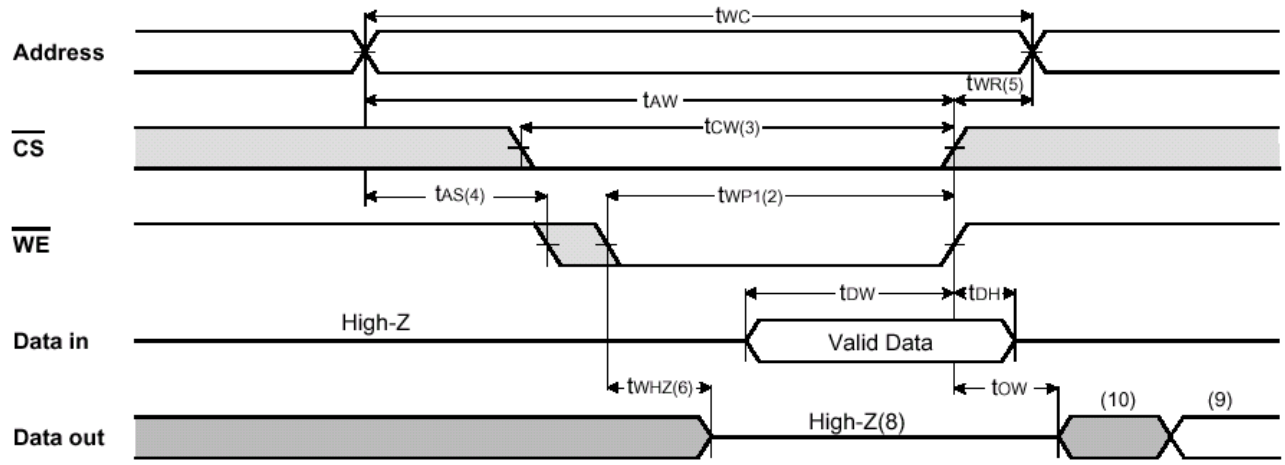
NOTES(READ CYCLE)

1. WE is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(Max.) is less than tLZ(Min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with CS=VIL.
7. Address valid prior to coincident with CS transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

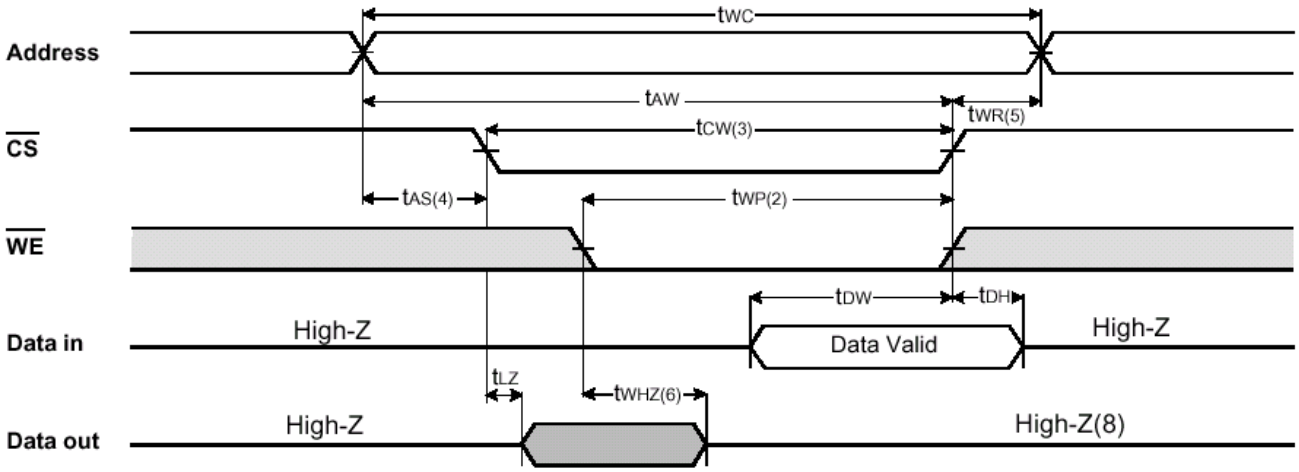
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$= Clock)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{CS}$ = Controlled)



NOTES(WRITE CYCLE)

1. ll write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low CS and WE. A write begins at the latest transition CS going low and WE going low ; A write ends at the earliest transition CS going high or WE going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of CS going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
6. If OE, CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When CS is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

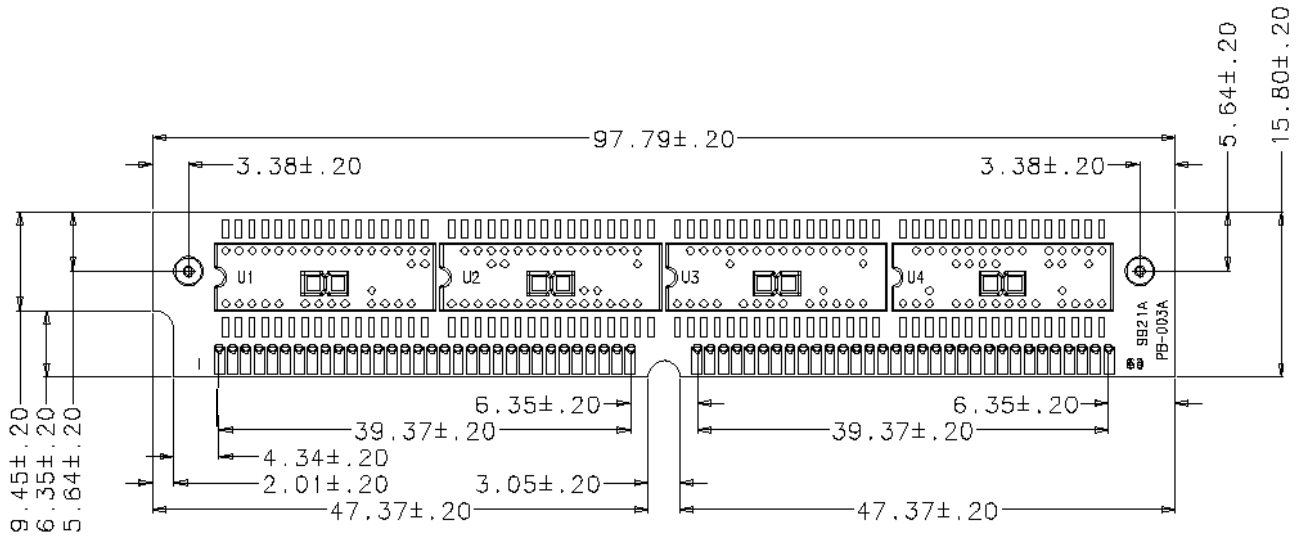
/CE	/WE	/OE	MODE	I/O PIN	SUPPLY CURRENT
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

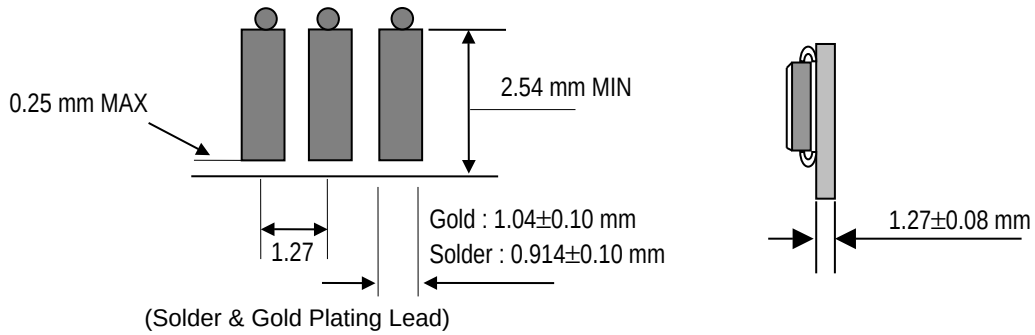
Note: X means Don't Care

PACKAGING INFORMATION

UNIT : mm

SIMM Design





ZIP Design

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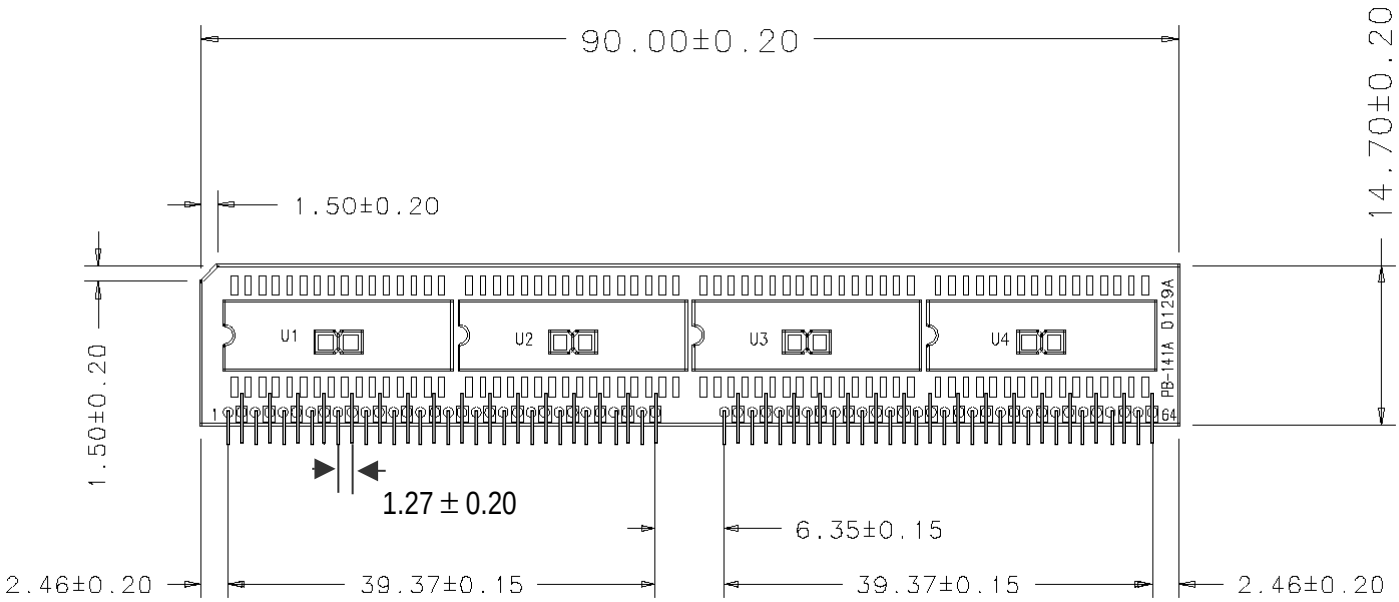

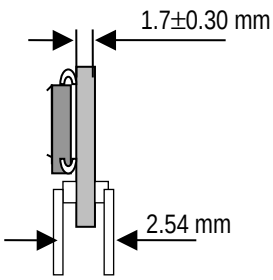

ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	Access Time
HMS12832M4G-10	512KByte	128KX 32bit	64 Pin-SIMM	4EA	5V	10ns
HMS12832M4G-12	512KByte	128KX 32bit	64 Pin-SIMM	4EA	5V	12ns
HMS12832M4G-15	512KByte	128KX 32bit	64 Pin-SIMM	4EA	5V	15ns
HMS12832M4G-20	512KByte	128KX 32bit	64 Pin-SIMM	4EA	5V	20ns
HMS12832Z4-10	512KByte	128KX 32bit	64 Pin-ZIP	4EA	5V	10ns
HMS12832Z4-12	512KByte	128KX 32bit	64 Pin-ZIP	4EA	5V	12ns
HMS12832Z4-15	512KByte	128KX 32bit	64 Pin-ZIP	4EA	5V	15ns
HMS12832Z4-20	512KByte	128KX 32bit	64 Pin-ZIP	4EA	5V	20ns