SRAM MODULE 2Mbyte (512K x 32-Bit), 72PIN SIMM, 5V
Part No. HMS51232M4G

GENERAL DESCRIPTION

The HMS51232M4GG is a high-speed static random access memory (SRAM) module containing 1,048,576 words organized in a x32-bit configuration. The module consists of four 512K x 8 SRAMs mounted on a 72-pin, single-sided, FR4-printed circuit board.

PD0 to PD3 identify the module's density allowing interchangeable use of alternate density, industry- standard modules. Four chip enable inputs, (/CE1, /CE2, /CE3 and /CE4) are used to enable the module's 4 bytes independently. Output enable(/OE) and write enable(/WE) can set the memory input and output.

Data is written into the SRAM memory when write enable (/WE) and chip enable (/CE) inputs are both LOW. Reading is accomplished when /WE remains HIGH and /CE and output enable (/OE) are LOW.

For reliability, this SRAM module is designed as multiple power and ground pin. All module components may be powered from a single +5V DC power supply and all inputs and outputs are fully TTL-compatible.

FEATURES

- Access times : 10, 12, 15, 17 and 20
- High-density 2Mbyte design
- High-reliability, high-speed design
- Single + 5V ±0.5V power supply
- Easy memory expansion /CE and /OE functions
- All inputs and outputs are TTL-compatible
- Industry-standard pinout
- FR4-PCB design
- Part Identification
  - HMS51232M4G : SIMM design

OPTIONS MARKING

- Timing

10ns access	-10
12ns access	-12
15ns access	-15
17ns access	-17
20ns access	-20

- Packages

72-pin SIMM	M

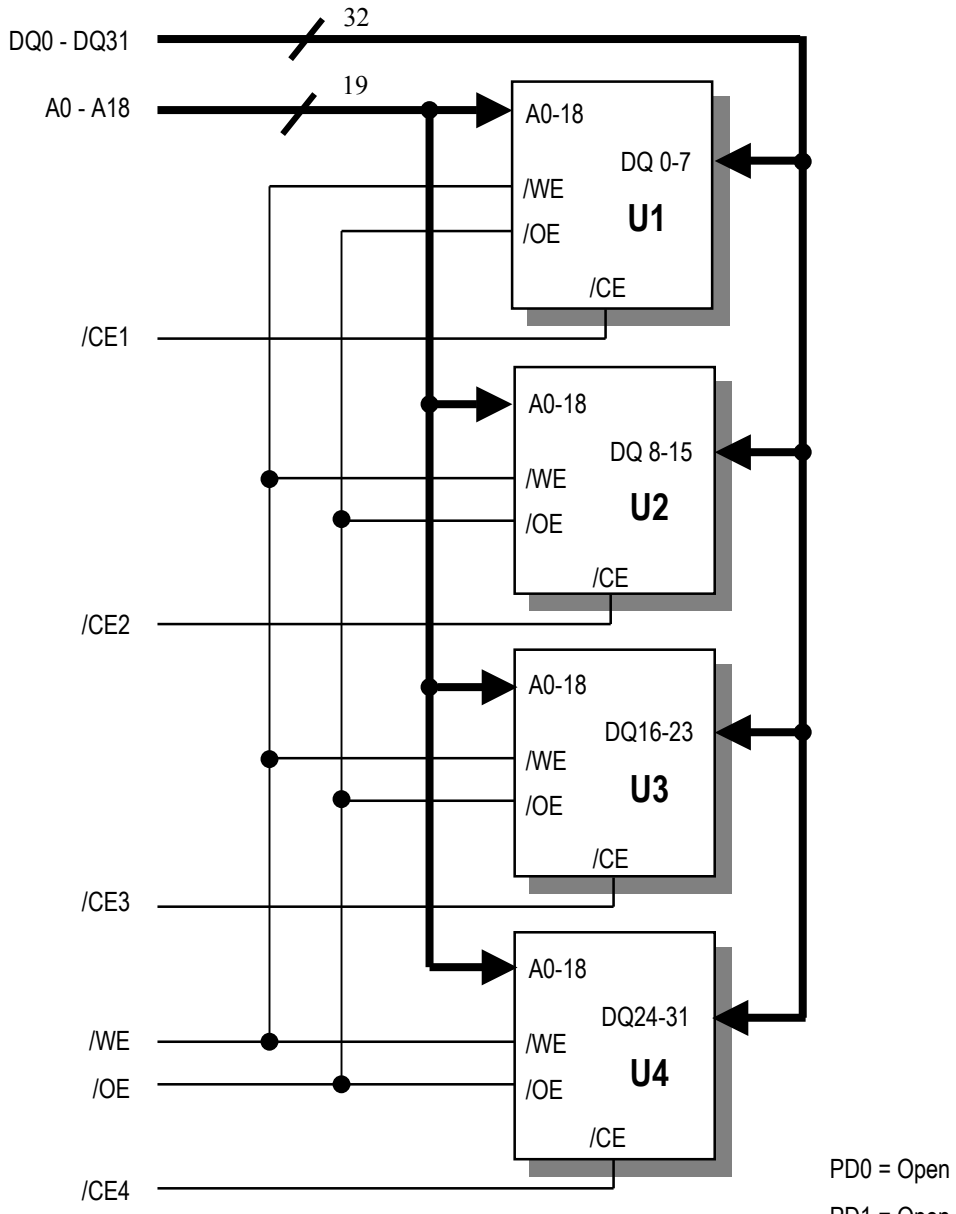
PIN ASSIGNMENT

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	NC	25	DQ13	49	DQ27
2	NC	26	DQ5	50	DQ19
3	PD2	27	DQ14	51	A3
4	PD3	28	DQ6	52	A10
5	Vss	29	DQ15	53	A4
6	PD0	30	DQ7	54	A11
7	PD1	31	Vss	55	A5
8	DQ0	32	/WE	56	A12
9	DQ8	33	A15	57	Vcc
10	DQ1	34	A14	58	A13
11	DQ9	35	/CE2	59	A6
12	DQ2	36	/CE1	60	DQ20
13	DQ10	37	/CE4	61	DQ28
14	DQ3	38	/CE3	62	DQ21
15	DQ11	39	A17	63	DQ29
16	Vcc	40	A16	64	DQ22
17	A0	41	/OE	65	DQ30
18	A7	42	Vss	66	DQ23
19	A1	43	DQ24	67	DQ31
20	A8	44	DQ16	68	Vss
21	A2	45	DQ25	69	A18
22	A9	46	DQ17	70	NC
23	DQ12	47	DQ26	71	NC
24	DQ4	48	DQ18	72	NC

PD0 = Open
PD1 = Open
PD2 = Vss
PD3 = Open

72-Pin SIMM
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	/OE	/CE	/WE	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
READ	L	L	H	Dout	ACTIVE
WRITE	X	L	L	Din	ACTIVE

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5V to +7.0V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5V to +7.0V
Power Dissipation	P_D	4W
Storage Temperature	T_{STG}	-65°C to +150°C
Operating Temperature	T_A	0°C to +70°C

- Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

PARAMETER	SYMBOL	MIN	TYP.	MAX
Supply Voltage	V_{CC}	4.5V	5.0V	5.5V
Ground	V_{SS}	0	0	0
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5V**
Input Low Voltage	V_{IL}	-0.5*	-	0.8V

* V_{IL}(Min.) = -2.0V (Pulse Width ≤ 10ns) for I ≤ 20 mA

** V_{IH}(Max.) = Vcc+2.0V (Pulse Width ≤ 10ns) for I ≤ 20 mA

DC AND OPERATING CHARACTERISTICS (1)(0°C ≤ T_A ≤ 70 °C ; Vcc = 5V ± 0.5V)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNITS
Input Leakage Current	V_{IN} = Vss to Vcc	IL_I	-2	2	μA
Output Leakage Current	/CE=V_{IH} or /OE =V_{IH} or /WE=V_{IL} V_{OUT}=Vss to V_{CC}	IL_0	-2	2	μA
Output High Voltage	V_{OH} = -4.0mA	V_{OH}	2.4	-	V
Output Low Voltage	V_{OL} = 8.0mA	V_{OL}		0.4	V

* Vcc=5.0V, Temp=25 °C

DC AND OPERATING CHARACTERISTICS (2)

DESCRIPTION	TEST CONDITIONS	SYMBOL	MAX			UNIT
			-15	-17	-20	
Power Supply Current: Operating	Min. Cycle, 100% Duty /CE=V_{IL}, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA	I_{CC}	170	165	160	mA
Power Supply Current: Standby	Min. Cycle, /CE=V_{IH}	I_{SB}	50	50	50	mA
	f=0MHZ, /CE≥V_{CC}-0.2V, V_{IN}≥ V_{CC}-0.2V or V_{IN}≤0.2V	I_{SB1}	10	10	10	mA

CAPACITANCE

DESCRIPTION	TEST CONDITIONS	SYMBOL	MAX	UNIT
Input /Output Capacitance	$V_{I/O}$=0V	$C_{I/O}$	8	pF
Input Capacitance	V_{IN}=0V	C_{IN}	7	pF

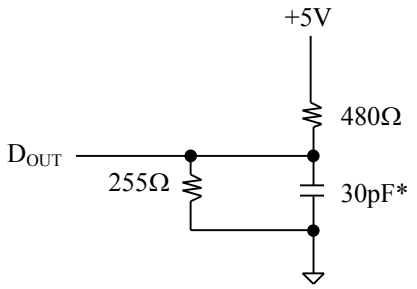
* NOTE : Capacitance is sampled and not 100% tested

AC CHARACTERISTICS ($0^oC \le T_A \le 70\ ^oC$; Vcc = 5V ± 0.5V, unless otherwise specified)

TEST CONDITIONS

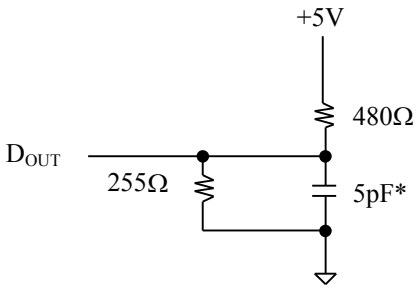
PARAMETER	VALUE
Input Pulse Level	0.V to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)

for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ}



* Including scope and jig capacitance

READ CYCLE

PARAMETER	SYMBOL	-15		-17		-20		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC}	15	-	17	-	20	-	ns
Address Access Time	t_{AA}	-	15	-	17	-	20	ns
Chip Select to Output	t_{CO}	-	15	-	17	-	20	ns
Output Enable to Output	t_{OE}	-	7	-	8	-	9	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Disable to High-Z Output	t_{OHZ}	0	7	0	8	0	9	ns
Chip Disable to High-Z Output	t_{HZ}	0	7	0	8	0	9	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns
Chip Select to Power Up Time	t_{PU}	0	-	0	-	0	-	ns
Chip Select to Power Down Time	t_{PD}	-	15	-	17	-	20	ns

WRITE CYCLE

PARAMETER	SYMBOL	-15		-17		-20		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Write Cycle Time	t_{WC}	15	-	17	-	20	-	ns
Chip Select to End of Write	t_{CW}	12	-	13	-	14	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	12	-	13	-	14	-	ns
Write Pulse Width (/OE=High)	t_{WP}	12	-	13	-	14	-	ns
Write Recovery Time (/OE=Low)	t_{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t_{WZ}	0	7	0	8	0	9	ns
Data to Write Time Overlap	t_{DW}	8	-	9	-	10	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End of Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	ns

TIMING DIAGRAMS

Please refer to timing diagram chart.

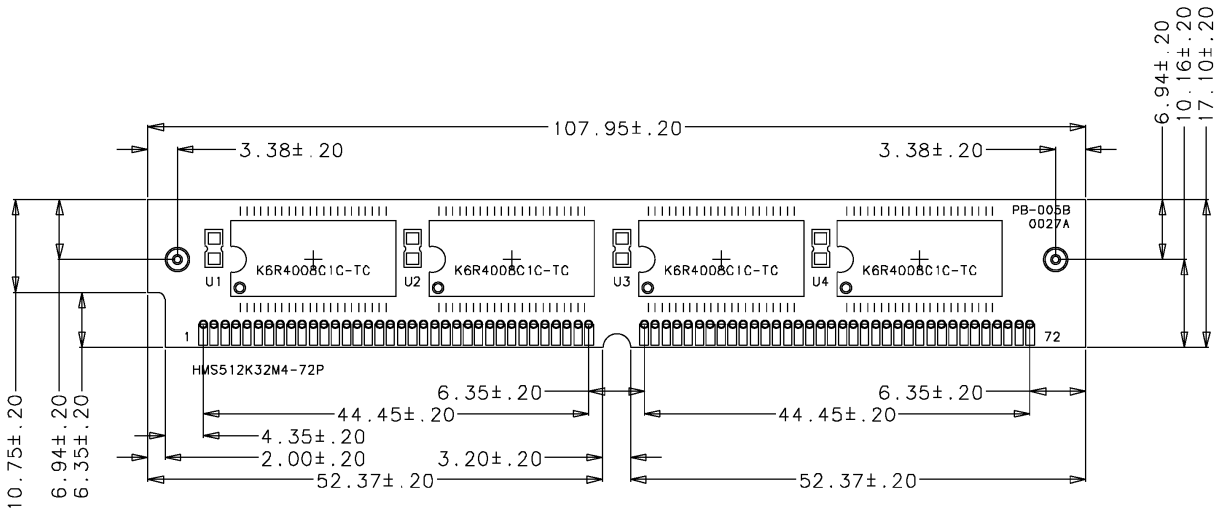
FUNCTIONAL DESCRIPTION

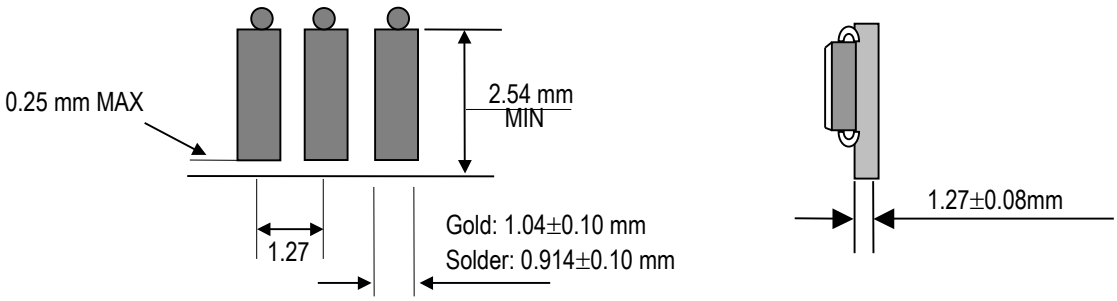
/CE	/WE	/OE	MODE	I/O PIN	SUPPLY CURRENT
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note: X means Don't Care

PACKAGING INFORMATION

SIMM Design





(Solder & Gold Plating Lead)

ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	Speed
HMS 51232M4G-10	2MByte	512K x 32bit	72 Pin-SIMM	4EA	5V	10ns
HMS 51232M4G-12	2MByte	512K x 32bit	72 Pin-SIMM	4EA	5V	12ns
HMS 51232M4G-15	2MByte	512K x 32bit	72 Pin-SIMM	4EA	5V	15ns
HMS 51232M4G-17	2MByte	512K x 32bit	72 Pin-SIMM	4EA	5V	17ns
HMS 51232M4G-20	2MByte	512K x 32bit	72 Pin-SIMM	4EA	5V	20ns