Data Sheet | July 1999 | File Number 4608.1

Radiation Hardened 2K x 8 CMOS PROM

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

The Intersil HS-6617RH-T is a radiation hardened 16k CMOS PROM, organized in a 2K word by 8-bit format. The chip is manufactured using a radiation hardened CMOS process, and is designed to be functionally equivalent to the HM-6617. Synchronous circuit design techniques combine with CMOS processing to give this device high speed performance with very low power dissipation.

On chip address latches are provided, allowing easy interfacing with recent generation microprocessors that use multiplexed address/data bus structure, such as the HS-80C86RH. The output enable control ($\overline{G}$) simplifies microprocessor system interfacing by allowing output data bus control, in addition to, the chip enable control. Synchronous operation of the HS-6617RH-T is ideal for high speed pipe-lined architecture systems and also in synchronous logic replacement functions.

Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the HS-6617RH-T are contained in SMD 5962-95708. A "hot-link" is provided from our website for downloading**.**
www.intersil.com/spacedefense/newsafclasst.asp

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.
www.intersil.com/quality/manuals.asp

Ordering Information

ORDERING NUMBER	PART NUMBER	TEMP. RANGE (^oC)
5962R9570801TJC	HS1-6617RH-T	-55 to 125
HS1-6617RH/Proto	HS1-6617RH/Proto	-55 to 125
5962R9570801TXC	HS9-6617RH-T	-55 to 125
HS9-6617RH/Proto	HS9-6617RH/Proto	-55 to 125

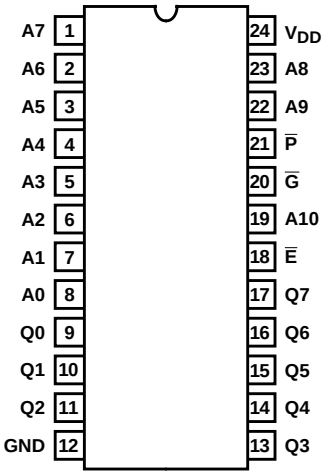
NOTE: ***Minimum order quantity for -T is 150 units through distribution, or 450 units direct.***

Features

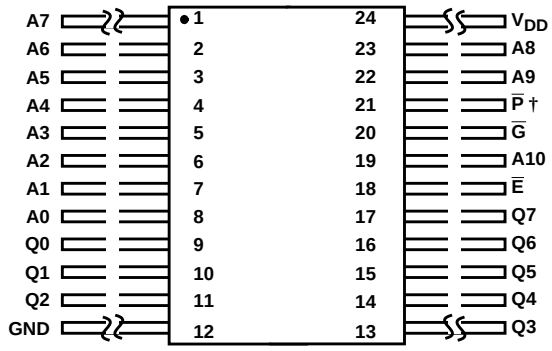
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose (γ) 1 x 10^5 RAD(Si)
  - SEU LET 16MeV/mg/cm^2
  - SEL LET 100MeV/mg/cm^2
- Field Programmable Nicrome Fuse Links
- Low Standby Power 1.1mW Max
- Low Operating Power 137.5mW/MHz Max
- Fast Access Time 100ns Max
- TTL Compatible Inputs/Outputs
- Synchronous Operation
- On Chip Address Latches, Three-State Outputs

Pinouts

HS1-6617RH-T (SBDIP), CDIP2-T24
TOP VIEW

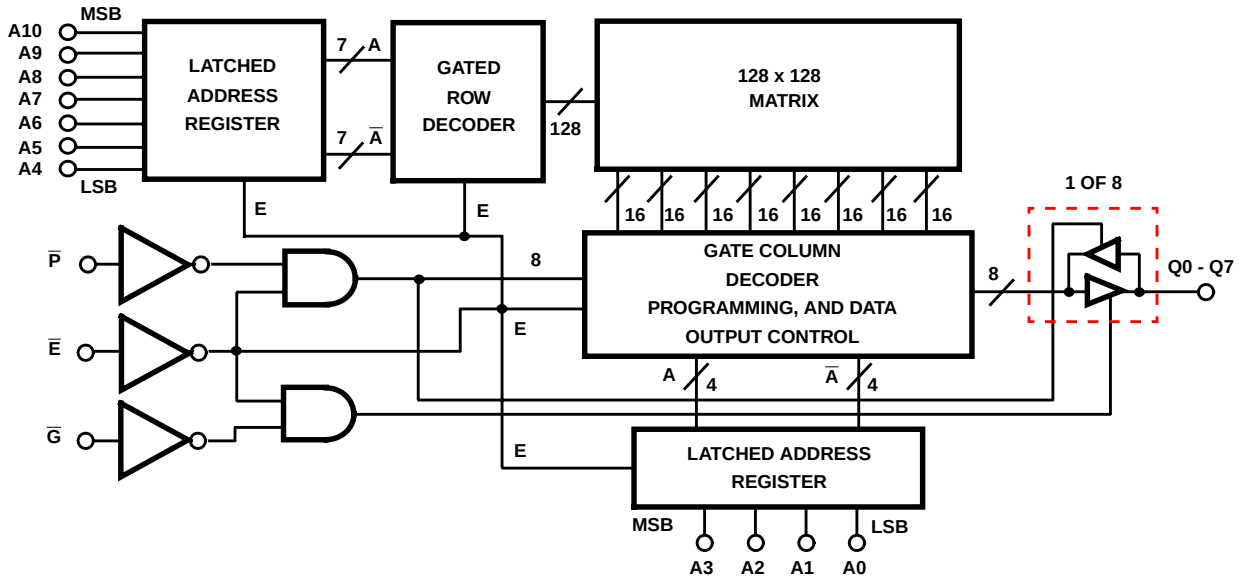


HS9-6617RH-T (FLATPACK), CDFP4-F24
TOP VIEW



† $\overline{P}$ must be hardwired at all times to V_{DD}, except during programming.

Functional Diagram



ALL LINES POSITIVE LOGIC:
ACTIVE HIGH
THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

ADDRESS LATCHES & GATED DECODERS:
LATCH ON FALLING EDGE OF $\overline{E}$
GATE ON FALLING EDGE OF $\overline{G}$
$\overline{P}$ = HARDWIRED TO V_{DD} EXCEPT DURING PROGRAMMING

TRUTH TABLE

$\overline{E}$	$\overline{G}$	MODE
0	0	Enabled
0	1	Output Disabled
1	X	Disabled

Timing Waveform

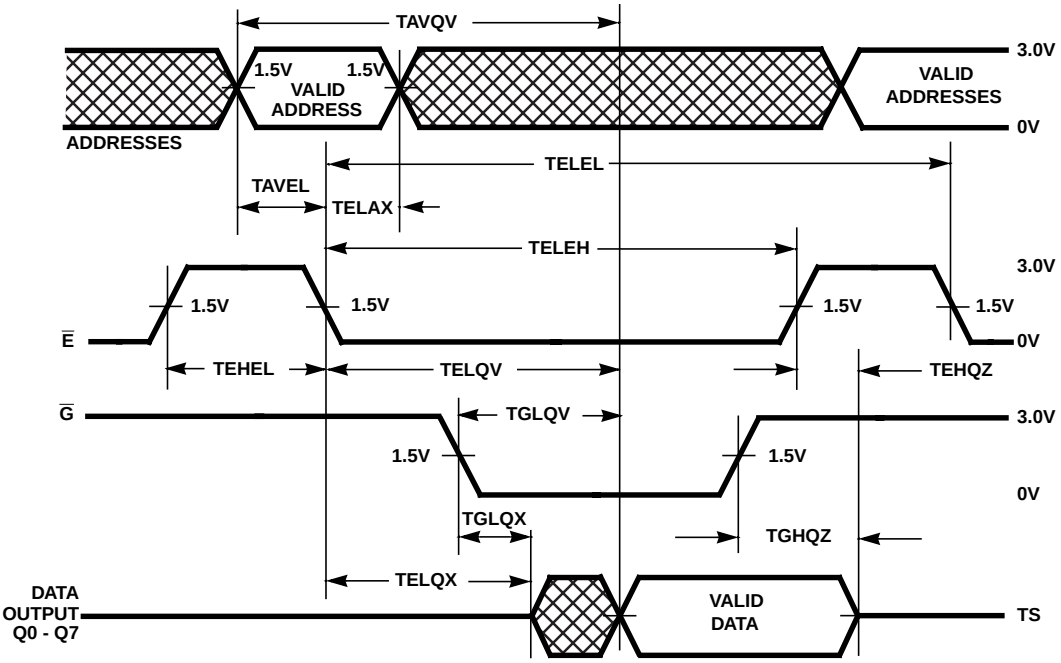


FIGURE 1. READ CYCLE

Die Characteristics

DIE DIMENSIONS:

(4166µm x 6350µm x 483µm ±25.4µm)

164 x 250 x 19mils ±1mil

METALLIZATION:

Type: Silicon - Aluminum

Thickness: 13.0kÅ ±2kÅ

SUBSTRATE POTENTIAL:

V_{DD}

BACKSIDE FINISH:

Silicon

PASSIVATION:

Type: Silox (S_iO_2)

Thickness: 8.0kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

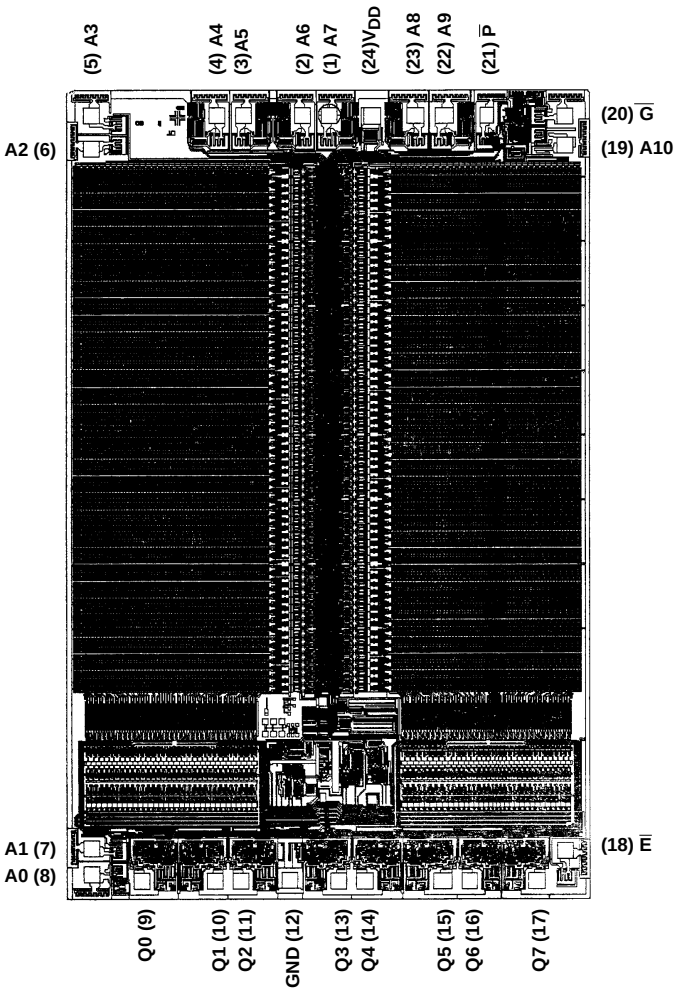
< 2.0e5 A/cm^2

PROCESS:

SSAJIIV-RH

Metallization Mask Layout

HS-6617RH-T



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.