



**Synchronous DRAM Module, 256Mbyte (32M x 64-Bit) SMM based
on 32Mx8, 4Banks, 8K Ref., 3.3V Part No. HSD32M64F8V/VA**

GENERAL DESCRIPTION

The HSD32M64F8V/VA is a 32M x 64 bit Synchronous Dynamic RAM high density memory module. The module consists of eight CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II packages is mounted on a 120-pin, double-sided, FR-4-printed circuit board., Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The HSD32M64F8V/VA is a SMM (Stackable Memory Module) designed and is intended for mounting into two 60-pin connector sockets. Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications All module components may be powered from a single 3.3V DC power supply and all inputs and outputs are LVTTTL-compatible.

FEATURES

- Part Identification

HSD32M64F8V :

Stacking Height (T = 11.3mm)

HSD32M64F8VA :

Stacking Height (T = 7.3mm)

- Burst mode operation
- Auto & self refresh capability (8192 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm 0.3V$ power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- 120pin-SMM type FR4-PCB design
- The used device is 32Mx8bit SRAM
- Pin assignment is compatible with
 - HSD8M64F8V
 - HSD16M64F8V

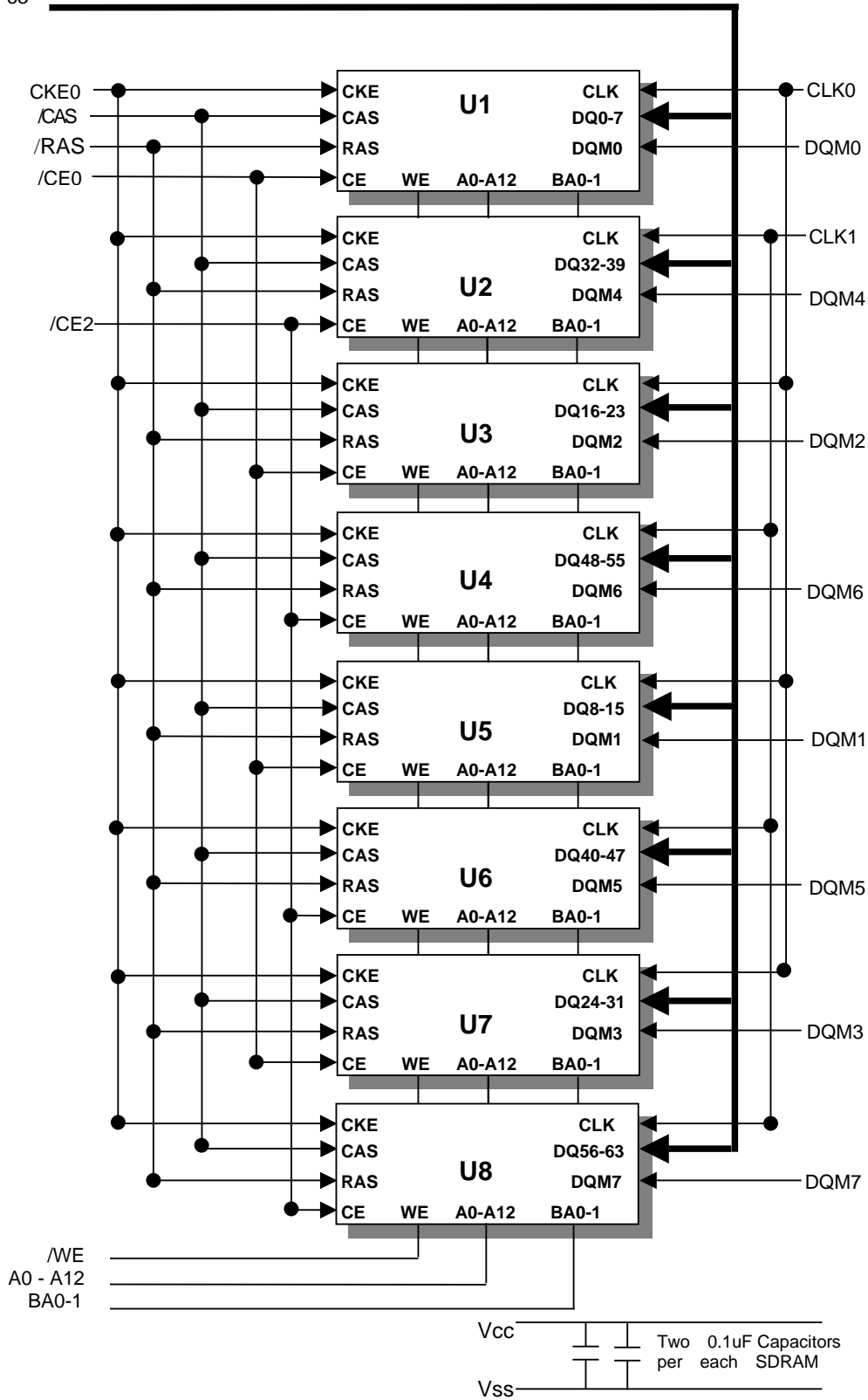
PIN ASSIGNMENT

| 60-PIN P1 Connector | | | | 60-PIN P2 Connector | | | |
|---------------------|--------|-----|--------|---------------------|--------|-----|--------|
| PIN | Symbol | PIN | Symbol | PIN | Symbol | PIN | Symbol |
| 1 | Vcc | 31 | Vss | 1 | Vss | 31 | Vcc |
| 2 | DQ32 | 32 | DQ0 | 2 | DQ16 | 32 | DQ48 |
| 3 | DQ33 | 33 | DQ1 | 3 | DQ17 | 33 | DQ49 |
| 4 | DQ34 | 34 | DQ2 | 4 | DQ18 | 34 | DQ50 |
| 5 | DQ35 | 35 | DQ3 | 5 | DQ19 | 35 | DQ51 |
| 6 | DQ36 | 36 | DQ4 | 6 | DQ20 | 36 | DQ52 |
| 7 | DQ37 | 37 | DQ5 | 7 | DQ21 | 37 | DQ53 |
| 8 | DQ38 | 38 | DQ6 | 8 | DQ22 | 38 | DQ54 |
| 9 | DQ39 | 39 | DQ7 | 9 | DQ23 | 39 | DQ55 |
| 10 | Vcc | 40 | Vss | 10 | Vss | 40 | Vcc |
| 11 | DQ40 | 41 | DQ8 | 11 | DQ24 | 41 | DQ56 |
| 12 | DQ41 | 42 | DQ9 | 12 | DQ25 | 42 | DQ57 |
| 13 | DQ42 | 43 | DQ10 | 13 | DQ26 | 43 | DQ58 |
| 14 | DQ43 | 44 | DQ11 | 14 | DQ27 | 44 | DQ59 |
| 15 | DQ44 | 45 | DQ12 | 15 | DQ28 | 45 | DQ60 |
| 16 | DQ45 | 46 | DQ13 | 16 | DQ29 | 46 | DQ61 |
| 17 | DQ46 | 47 | DQ14 | 17 | DQ30 | 47 | DQ62 |
| 18 | DQ47 | 48 | DQ15 | 18 | DQ31 | 48 | DQ63 |
| 19 | Vcc | 49 | Vss | 19 | Vss | 49 | Vcc |
| 20 | DQM4 | 50 | DQM0 | 20 | DQM2 | 50 | DQM6 |
| 21 | DQM5 | 51 | DQM1 | 21 | DQM3 | 51 | DQM7 |
| 22 | NC | 52 | /WE | 22 | NC | 52 | A12 |
| 23 | CKE0 | 53 | CLK0 | 23 | BA0 | 53 | A11 |
| 24 | CKE1 | 54 | CLK1 | 24 | BA1 | 54 | A9 |
| 25 | Vcc | 55 | Vss | 25 | A10/AP | 55 | A8 |
| 26 | NC | 56 | /CAS | 26 | A0 | 56 | A7 |
| 27 | NC | 57 | /RAS | 27 | A1 | 57 | A6 |
| 28 | /CE2 | 58 | /CE0 | 28 | A2 | 58 | A5 |
| 29 | NC | 59 | NC | 29 | A3 | 59 | A4 |
| 30 | Vcc | 60 | Vss | 30 | Vss | 60 | Vcc |

Stackable Memory Module TOP VIEW

FUNCTIONAL BLOCK DIAGRAM

DQ0-63



PIN FUNCTION DESCRIPTION

| Pin | Name | Input Function |
|-----------|------------------------|---|
| CLK | System clock | Active on the positive going edge to sample all inputs. |
| /CE | Chip enable | Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM |
| CKE | Clock enable | Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command. |
| A0 ~ A12 | Address | Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9 |
| BA0 ~ BA1 | Bank select address | Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time. |
| /RAS | Row address strobe | Latches row addresses on the positive going edge of the CLK with RAS low. Enables row access & precharge. |
| /CAS | Column address strobe | Latches column addresses on the positive going edge of the CLK with CAS low. Enables column access. |
| /WE | Write enable | Enables write operation and row precharge. Latches data in starting from CAS, WE active. |
| DQM0 ~ 7 | Data input/output mask | Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking) |
| DQ0 ~ 63 | Data input/output | Data inputs/outputs are multiplexed on the same pins. |
| Vcc/Vss | Power supply/ground | Power and ground for the input buffers and the core logic. |

ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATING |
|---------------------------------------|--------------|----------------|
| Voltage on Any Pin Relative to Vss | $V_{IN,OUT}$ | -1V to 4.6V |
| Voltage on Vcc Supply Relative to Vss | Vcc | -1V to 4.6V |
| Power Dissipation | P_D | 8W |
| Storage Temperature | T_{STG} | -55°C to 150°C |
| Short Circuit Output Current | I_{OS} | 400mA |

Notes :

Permanent device damage may occur if " Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC OPERATING CONDITIONS

(Recommended operating conditions (Voltage referenced to VSS = 0V, TA = 0 to 70°C))

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNIT | NOTE |
|-----------------------|-----------------|------|------|----------------------|------|------------------------|
| Supply Voltage | V _{CC} | 3.0 | 3.3 | 3.6 | V | |
| Input High Voltage | V _{IH} | 2.0 | 3.0 | V _{CC} +0.3 | V | 1 |
| Input Low Voltage | V _{IL} | -0.3 | 0 | 0.8 | V | 2 |
| Output High Voltage | V _{OH} | 2.4 | - | - | V | I _{OH} = -2mA |
| Output Low Voltage | V _{OL} | - | - | 0.4 | V | I _{OL} = 2mA |
| Input leakage current | I _{LI} | -10 | - | 10 | uA | 3 |

Notes :

- V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
- V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
- Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE

(VCC = 3.3V, TA = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

| DESCRIPTION | SYMBOL | MIN | MAX | UNITS |
|--------------------------------|------------------|-----|-----|-------|
| Clock | C _{CLK} | 20 | 32 | pF |
| Address | C _{ADD} | 20 | 40 | pF |
| /RAS, /CAS, /WE, /CS, CKE, DQM | C _{IN} | 20 | 40 | pF |
| DQ (DQ0 ~ DQ15) | C _{OUT} | 32 | 52 | pF |

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

| PARAMETER | SYMBOL | TEST CONDITION | VERSION | | | | UNIT | NOTE |
|---|--------------------|---|---------|------|------|------|------|------|
| | | | -13 | -12 | -10 | -10L | | |
| Operating current (One bank active) | I _{CC1} | Burst length = 1 t _{RC} ≥ t _{RC(min)} I _O = 0mA | 960 | 960 | 880 | 880 | mA | 1 |
| Precharge standby current in power-down mode | I _{CC2P} | CKE ≤ V _{IL(max)} t _{CC} =10ns | 16 | | | | mA | |
| | I _{CC2PS} | CKE & CLK ≤ V _{IL(max)} t _{CC} =∞ | 16 | | | | mA | |
| Precharge standby current in non power-down mode | I _{CC2N} | CKE ≥ V _{IH(min)} CS* ≥ V _{IH(min)} , t _{CC} =10ns Input signals are changed one time during 20ns | 128 | | | | mA | |
| | I _{CC2NS} | CKE ≥ V _{IH(min)} CLK ≤ V _{IL(max)} , t _{CC} =∞ Input signals are stable | 112 | | | | | |
| Active standby current in power-down mode | I _{CC3P} | CKE ≤ V _{IL(max)} , t _{CC} =10ns | 48 | | | | mA | |
| | I _{CC3PS} | CKE&CLK ≤ V _{IL(max)} t _{CC} =∞ | 48 | | | | | |
| Active standby current in non power-down mode (One bank active) | I _{CC3N} | CKE ≥ V _{IH(min)} , CS* ≥ V _{IH(min)} , t _{CC} =10ns Input signals are changed one time during 20ns | 240 | | | | mA | |
| | I _{CC3NS} | CKE ≥ V _{IH(min)} CLK ≤ V _{IL(max)} , t _{CC} =∞ Input signals are stable | 200 | | | | | |
| Operating current (Burst mode) | I _{CC4} | I _O = 0 mA Page burst 4Banks Activated t _{CCD} = 2CLKs | 1120 | 1120 | 920 | 920 | mA | 1 |
| Refresh current | I _{CC5} | t _{RC} ≥ t _{RC(min)} | 1680 | 1680 | 1600 | 1600 | mA | 2 |
| Self refresh current | I _{CC6} | CKE ≤ 0.2V | 40 | | | | mA | |
| | | | 16 | | | | mA | |

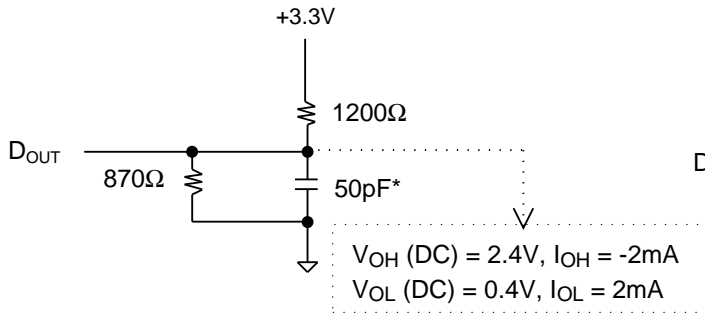
Notes :

1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noticed, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}).

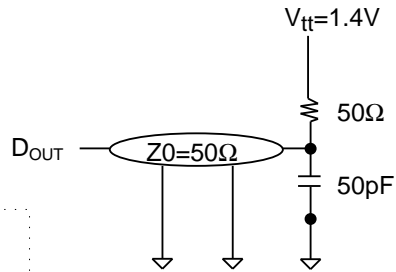
AC OPERATING TEST CONDITIONS

(vcc = 3.3V ± 0.3V, TA = 0 to 70°C)

| PARAMETER | Value | UNIT |
|---|-------------|------|
| AC Input levels (Vih/Vil) | 2.4/0.4 | V |
| Input timing measurement reference level | 1.4 | V |
| Input rise and fall time | tr/tf = 1/1 | ns |
| Output timing measurement reference level | 1.4 | V |
| Output load condition | See Fig. 2 | |



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

| PARAMETER | SYMBOL | VERSION | | | | UNIT | NOTE |
|--|------------------------|---------------|-----|-----|------|------|------|
| | | -13 | -12 | -10 | -10L | | |
| Row active to row active delay | t _{RRD} (min) | 15 | 16 | 20 | 20 | ns | 1 |
| RAS to CAS delay | t _{RP} (min) | 20 | 20 | 20 | 20 | ns | 1 |
| Row precharge time | t _{RP} (min) | 20 | 20 | 20 | 20 | ns | 1 |
| Row active time | t _{RAS} (min) | 45 | 48 | 50 | 50 | ns | 1 |
| | t _{RAS} (max) | 100 | | | | ns | |
| Row cycle time | t _{RC} (min) | 65 | 68 | 70 | 70 | ns | 1 |
| Last data in to row precharge | t _{RDL} (min) | 2 | | | | CLK | 2.5 |
| Last data in to Active delay | t _{DAL} (min) | 2 CLK + 20 ns | | | | - | 5 |
| Last data in to new col. address delay | t _{CDL} (min) | 1 | | | | CLK | 2 |
| Last data in to burst stop | t _{BDL} (min) | 1 | | | | CLK | 2 |
| Col. address to col. address delay | t _{CCD} (min) | 1 | | | | CLK | 3 |
| Number of valid output data | CAS latency=3 | 2 | | | | ea | 4 |
| | CAS latency=2 | - | | 1 | | | |

Notes :

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -8/H/L, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
(Recommend : tRDL=2CLK and tDAL=2CLK & 20ns.)

AC CHARACTERISTICS

(AC operating conditions unless otherwise noted)

| PARAMETER | | SYMBOL | -13 | | -12 | | -10 | | -10L | | UNIT | NOTE |
|------------------------------|------------------|------------------|-----|------|-----|------|-----|------|------|------|------|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | |
| CLK cycle time | CAS latency=3 | t _{CC} | 7.5 | 1000 | 8 | 1000 | 10 | 1000 | 10 | 1000 | ns | 1 |
| | CAS latency=2 | | - | - | 10 | 12 | | | | | | |
| CLK to valid output delay | CAS latency=3 | t _{SAC} | | 5.4 | | 6 | | 6 | | 6 | ns | 1,2 |
| | CAS latency=2 | | | - | | - | | 6 | | 7 | | |
| Output data hold time | CAS latency=3 | t _{OH} | 2.7 | | 3 | | 3 | | 3 | | ns | 2 |
| | CAS latency=2 | | - | - | | 3 | | 3 | | | | |
| CLK high pulse width | | t _{CH} | 2.5 | | 3 | | 3 | | 3 | | ns | 3 |
| CLK low pulse width | | t _{CL} | 2.5 | | 3 | | 3 | | 3 | | ns | 3 |
| Input setup time | | t _{SS} | 1.5 | | 2 | | 2 | | 2 | | ns | 3 |
| Input hold time | | t _{SH} | 0.8 | | 1 | | 1 | | 1 | | ns | 3 |
| CLK to output in Low-Z | | t _{SLZ} | 1 | | 1 | | 1 | | 1 | | ns | 3 |
| CLK to output in Hi-Z | CAS latency=3 | t _{SHZ} | | 5.4 | | 6 | | 6 | | 6 | ns | 2 |
| | CAS latency=2 | | | - | | - | | 6 | | 7 | ns | |

Notes :

1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered, ie., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

| COMMAND | | CKE n-1 | CKE n | /C S | /R A S | /C A S | /W E | D Q M | BA 0,1 | A10/ AP | A11,A12, A9~A0 | NOTE |
|------------------------------------|------------------------|---------|-------|------|--------|--------|------|-------|---------|-------------|--------------------------|------|
| Register | Mode register set | H | X | L | L | L | L | X | OP code | | | 1,2 |
| Refresh | Auto refresh | H | H | L | L | L | H | X | X | | | 3 |
| | Self refresh | | Entry | | | | | | L | X | | |
| | | Exit | L | H | L | H | H | H | X | X | | |
| | H | | | | X | X | X | 3 | | | | |
| Bank active & row addr. | | H | X | L | L | H | H | X | V | Row address | | |
| Read & column address | Auto precharge disable | H | X | L | H | L | H | X | V | L | Column Address (A0 ~ A9) | 4 |
| | Auto precharge disable | | | | | | | | | H | | 4,5 |
| Write & column address | Auto precharge disable | H | X | L | H | L | L | X | V | L | Column Address (A0 ~ A9) | 4 |
| | Auto precharge disable | | | | | | | | | H | | 4,5 |
| Burst Stop | | H | X | L | L | H | L | X | X | | | 6 |
| Precharge | Bank selection | H | X | L | L | H | L | X | V | L | X | |
| | All banks | | | | | | | | X | H | | |
| Clock suspend or active power down | Entry | H | L | H | X | X | X | X | X | | | |
| | Exit | | | L | H | X | X | | X | X | | |
| Precharge power down mode | Entry | H | L | H | X | X | X | X | X | | | |
| | | | | L | H | H | H | | | | | |
| | Exit | L | H | H | X | X | X | X | X | | | |
| | | | | L | V | V | V | | | | | |
| DQM | | H | X | | | | | V | X | | 7 | |
| No operation command | | H | X | H | X | X | X | X | X | | | |
| | | | | L | H | H | H | | | | | |

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes :

- OP Code : Operand code
A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)
- MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.
- Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
- BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
- During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at tRP after the end of burst.
- Burst stop command is valid at every burst length.
- DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

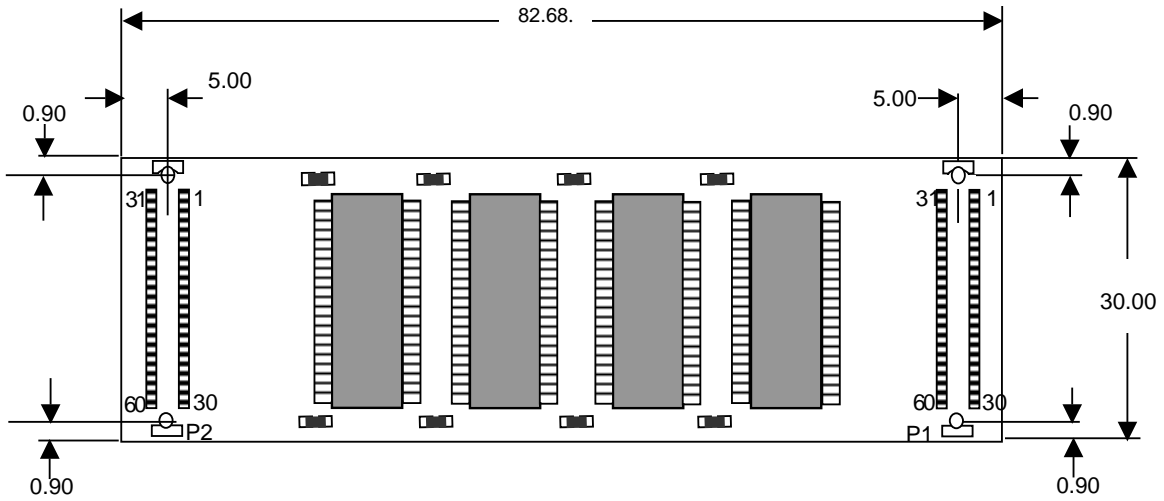
TIMING DIAGRAMS

Please refer to timing diagram chart (II)

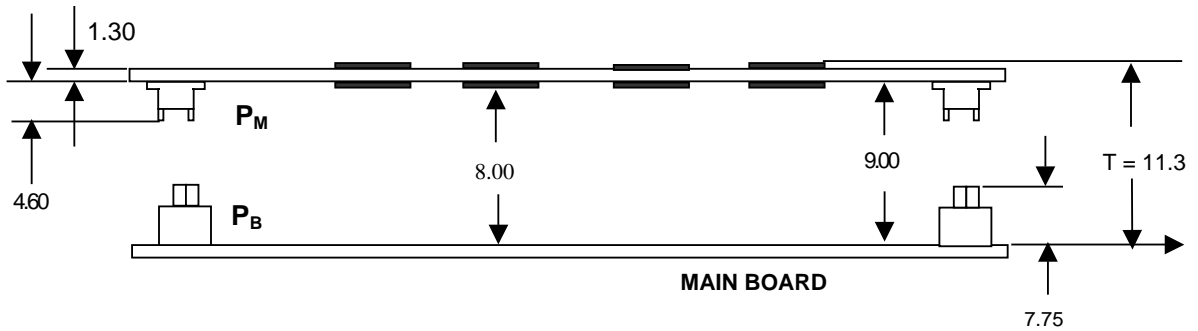
PACKAGING INFORMATION

Unit : mm

HSD32M64F8V



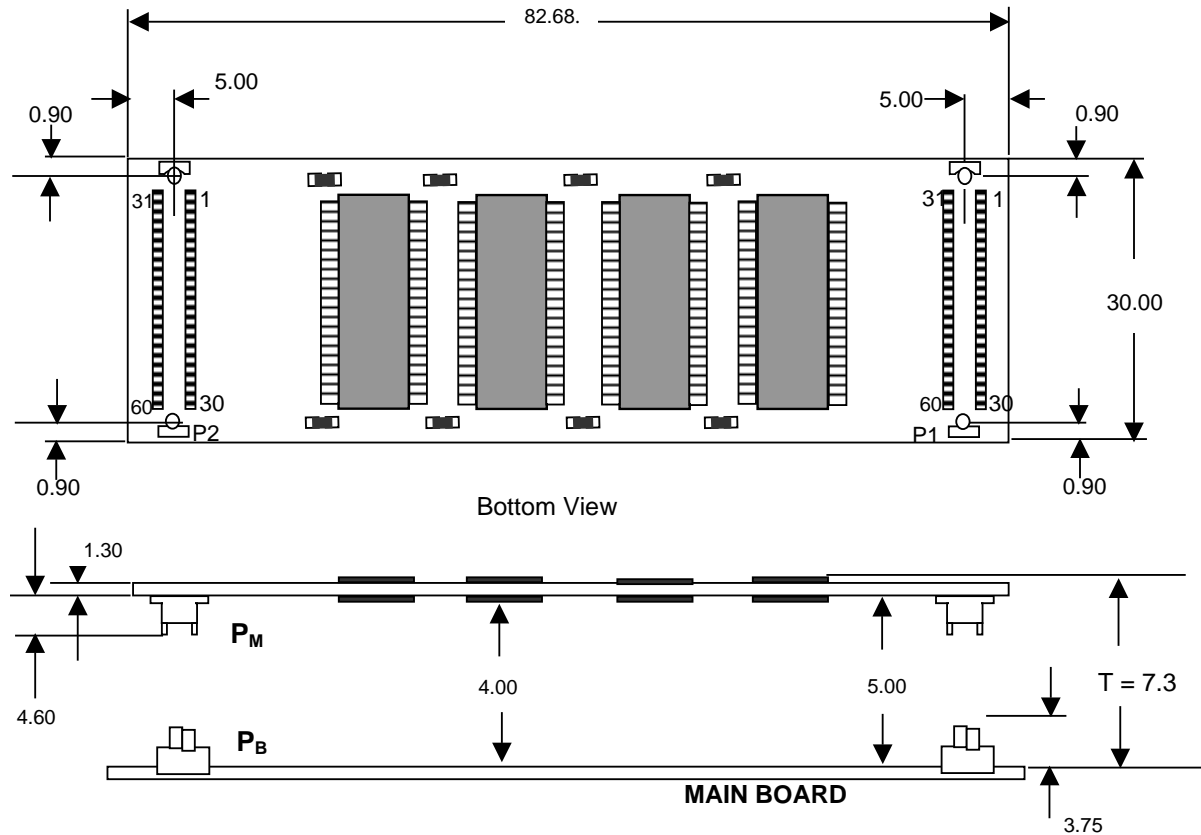
Bottom View



Connector Configuration

- Module PCB Bottom (P_M) : 177986-2, 0.8mm Free Height Plugs, 60pins
- Main Board top (P_B) : 5-179180-2,0.8mm Free Height Receptacles , 60pins

HSD32M64F8VA



Connector Configuration

- Module PCB Bottom (P_M) : 177984-2, 0.8mm Free Height Plugs, 60pins
- Main Board top (P_B) : 177983-2, 0.8mm Free Height Receptacles , 60pins

ORDERING INFORMATION

| Part Number | Density | Org. | Package | Ref. | Vcc | Feature | MAX.frq |
|------------------|----------|---------|----------------|------|------|--------------|------------------|
| HSD32M64F8V-13 | 256MByte | 32Mx 64 | 120 Pin SMM | 8K | 3.3V | | 133MHz (CL=3) |
| HSD32M64F8V-F13 | 256Mbyte | 32Mx 64 | 120 Pin SMM | 8K | 3.3V | Low Power | 133MHz (CL=3) |
| HSD32M64F8V-12 | 256Mbyte | 32Mx 64 | 120 Pin SMM | 8K | 3.3V | | 125MHz (CL=3) |
| HSD32M64F8V-F12 | 256Mbyte | 32Mx 64 | 120 Pin SMM | 8K | 3.3V | Low Power | 125MHz (CL=3) |
| HSD32M64F8V-10 | 256Mbyte | 32Mx 64 | 120 Pin SMM | 8K | 3.3V | | 100MHz (CL=2) |
| HSD32M64F8V-F10 | 256Mbyte | 32Mx 64 | 120 Pin SMM | 8K | 3.3V | Low Power | 100MHz (CL=2) |
| HSD32M64F8VA-13 | 256MByte | 32Mx 64 | 120 Pin SMM | 8K | 3.3V | | 133MHz (CL=3) |
| HSD32M64F8VA-F13 | 256Mbyte | 32Mx 64 | 120 Pin SMM | 8K | 3.3V | Low Power | 133MHz (CL=3) |
| HSD32M64F8VA-12 | 256Mbyte | 32Mx 64 | 120 Pin SMM | 8K | 3.3V | | 125MHz (CL=3) |
| HSD32M64F8VA-F12 | 256Mbyte | 32Mx 64 | 120 Pin SMM | 8K | 3.3V | Low Power | 125MHz (CL=3) |
| HSD32M64F8VA-10 | 256Mbyte | 32Mx 64 | 120 Pin SMM | 8K | 3.3V | | 100MHz (CL=2) |
| HSD32M64F8VA-F10 | 256Mbyte | 32Mx 64 | 120 Pin SMM | 8K | 3.3V | Low Power | 100MHz (CL=2) |

* F means Auto & Self refresh with Low-Power (3.3V)

* HSD32M64F8V : T = 11.3mm

* HSD32M64F8VA : T = 7.3mm