HYUNDAI

HY62V8400 Series

512K x 8-bit CMOS SRAM

PRELIMINARY

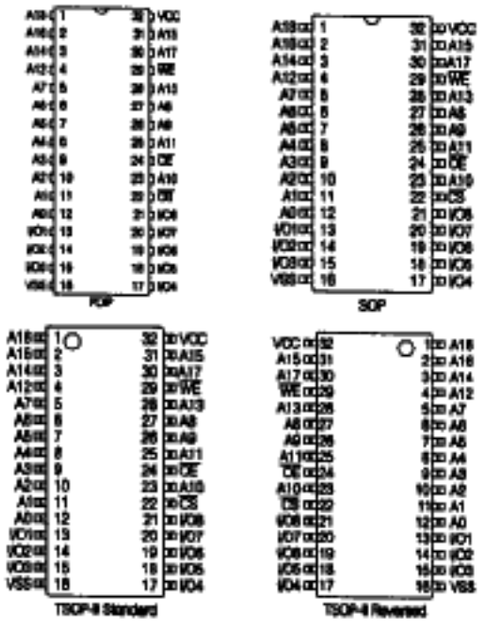
DESCRIPTION

The HY62V8400 is a high-speed, low power and 524,288 x 8-bits CMOS static RAM fabricated using Hyundai's high perfromance twin tub CMOS process technology. The HY62V8400 has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0 volt. Using COMS technology, supply voltages from 2.0 to 5.5 volt have little effect on supply current in data retention mode. The HY62V8400 is suitable for use in low voltage (2.7V - 5.5V) operation and battery back-up applications.

FEATURES

- **Extended operating voltage : 2.7V - 5.5V**
- **High speed**
  - **55/70/85/100ns at 5V**
  - **100/120/150/200ns at 3V**
- **Low power consumption**
  - **Operating : 25mW (typ.) at 5V**
    : 9mW (typ.) at 3V
  - **Standby (CMOS) : 5μW (typ.) at 5V**
    : 1.5 μW (typ.) at 3V
- **Battery backup**
  - **2.0V (min.) data retention**
- **Fully static operation**
  - **No clock or refresh required**
- **TTL compatible inputs and outputs**
- **Tri-state output**
- **Standard pin configuration**
  - **32 pin 600 mil PDIP**
  - **32 pin 525 mil SOP**
  - **32 pin 400 mil TSOP - II**

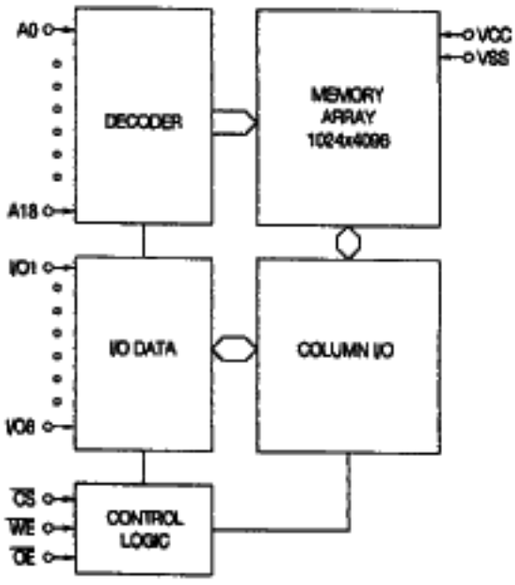
PIN CONNECTION



PIN DESCRIPTION

Pin Name	Pin Function
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
A0-A18	Address Inputs
I/O1-I/O8	Data Input/Output
Vcc	Power(2.7V - 5.5V)
Vss	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}, V_{IN}, V_{OUT}	Power Supply,Input/Output Voltage	-0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	-0 to 70	°C
T_{BIAS}	Temperature Under Bias	-10 to 125	°C
T_{STG}	Storage Temperature	-65 to 150	°C
P_D	Power Dissipation	1.0	W
I_{OUT}	Data Output Current	50	mA
T_{SOLDER}	Lead Soldering Temperature & Time	260 • 10	°C • sec

Note:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Power Supply Voltage	2.7	3.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	Vcc+0.5	V
V_{IL}	Input Low Voltage	-0.5[1]	-	0.4	V

Note:
1. V_{IL} = -3.0V for pulse width less than 50ns

TRUTH TABLE

MODE	I/O OPERATION	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$
Standby	High-Z	H	X	X
Output Disabled	High-Z	L	H	H
Read	Data Out	L	H	L
Write	Data in	L	L	X

Note:
1.H=V_{IH}, L=V_{IL}, X=Don't Care

DC CHARACTERISTICS

(T_A = 0°C to 70°C, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	VOLTAGE	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$		-1	-	1	μA
I_{LO}	Output Leakage Current	$V_{SS} \le V_{OUT} \le V_{CC}$ $\overline{CS}$ = V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$ = V_{IL}		-1	-	1	μA
I_{CC}	Operating Power Supply Current	$\overline{CS}$=V_{IL} V_{IN}= V_{IH} or V_{IL}, $I_{I/O}$=0mA	5V	-	5	10	mA
			3V	-	3	5	mA
I_{CC1}	Average Operating Current	$\overline{CS}$=V_{IL} Min. Duty Cycle=100% $I_{I/O}$=0mA	5V	-	50	70	mA
			3V	-	20	30	mA
I_{SB}	TTL Standby Current (TTL Inputs)	$\overline{CS}$=V_{IH}	5V	-	0.4	2	mA
			3V	-	-	0.5	mA
I_{SB1}	CMOS Standby Current (CMOS Inputs)	$\overline{CS}$ ≥ Vcc-0.2V	5V	-	1	30	μA
			3V	-	0.5	15	μA
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0mA	5V	2.4	-	-	V
			3V	2.2	-	-	V

Note:
1. Typical values are at V_{CC}=5.0V, T_A=25°C

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{CC}=5V ±10%, unless otherwise noted.)

#	SYMBOL	PARAMETER	-55		-70		-85		-10		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
	READ CYCLE										
1	t_{RC}	Read Cycle Time	55	-	70	-	85	-	100	-	ns
2	t_{AA}	Address Access Time	-	55	-	70	-	85	-	100	ns
3	t_{ACS}	Chip Select Access Time	-	55	-	70	-	85	-	100	ns
4	t_{OE}	Output Enable to Output Valid	-	25	-	35	-	45	-	50	ns
5	t_{CLZ}	Chip Select to Low -Z Output	10	-	10	-	10	-	10	-	ns
6	t_{OLZ}	Output Enable to Low-Z Output	5	-	5	-	5	-	5	-	ns
7	t_{CHZ}	Chip Disable to High -Z Output	0	20	0	25	0	30	0	30	ns
8	t_{OHZ}	Output Disable to High -Z Output	0	20	0	25	0	30	0	30	ns
9	t_{OH}	Output Hold from Address Change	10	-	10	-	10	-	10	-	ns
	WRITE CYCLE										
10	t_{WC}	Write Cycle Time	55	-	70	-	85	-	100	-	ns
11	t_{CW}	Chip Select to End of Write	45	-	60	-	70	-	80	-	ns
12	t_{AW}	Address Valid to End of Write	45	-	60	-	70	-	80	-	ns
13	t_{AS}	Address Set-up Time	0	-	0	-	0	-	0	-	ns
14	t_{WP}	Write Pluse Width	40	-	50	-	55	-	60	-	ns
15	t_{WR}	Write Recovery Time	0	-	0	-	0	-	0	-	ns
16	t_{WHZ}	Write to High-Z Output	0	20	0	25	0	30	0	30	ns
17	t_{DW}	Data to Write Time Overlap	25	-	30	-	35	-	40	-	ns
18	t_{DH}	Data Hold from Write Time	0	-	0	-	0	-	0	-	ns
19	t_{OW}	Output Active from End of Write	5	-	5	-	5	-	5	-	ns

AC CHARACTERISTICS

(TA=0°C to 70°C, Vcc=3V ±10%, unless otherwise noted.)

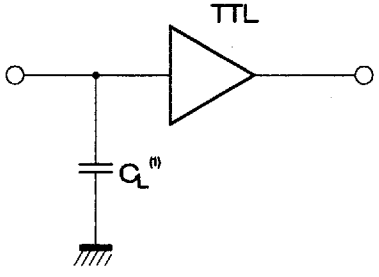
#	SYMBOL	PARAMETER	-10		-12		-15		-20		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE											
1	tRC	Read Cycle Time	100	-	120	-	150	-	200	-	ns
2	tAA	Address Access Time	-	100	-	120	-	150	-	200	ns
3	tACS	Chip Select Access Time	-	100	-	120	-	150	-	200	ns
4	tOE	Output Enable to Output Valid	-	50	-	60	-	75	-	100	ns
5	tCLZ	Chip Select to Low -Z Output	20	-	20	-	20	-	20	-	ns
6	tOLZ	Output Enable to Low-Z Output	10	-	10	-	10	-	10	-	ns
7	tCHZ	Chip Disable to High -Z Output	0	30	0	40	0	50	0	70	ns
8	tOHZ	Output Disable to High -Z Output	0	30	0	40	0	50	0	70	ns
9	tOH	Output Hold from Address Change	20	-	20	-	20	-	20	-	ns
WRITE CYCLE											
10	tWC	Write Cycle Time	100	-	120	-	150	-	200	-	ns
11	tCW	Chip Select to End of Write	80	-	100	-	120	-	150	-	ns
12	tAW	Address Valid to End of Write	80	-	100	-	120	-	150	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	0	-	ns
14	tWP	Write Pluse Width	75	-	85	-	100	-	140	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	0	-	ns
16	tWHZ	Write to High-Z Output	0	35	0	40	0	50	0	60	ns
17	tDW	Data to Write Time Overlap	45	-	50	-	60	-	80	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	0	-	0	-	ns
19	tOW	Output Active from End of Write	10	-	10	-	10	-	10	-	ns

AC TEST CONDITIONS

(T_A=0°C to 70°C, unless otherwise specified.)

PARAMETER	VOLTAGE	VALUE
Input Pulse Level	5V	0.8V to 2.4V
	3V	0.4V to 2.2V
Input Rise and Fall Time		5ns
Input and Output Timing Reference levels		1.5V
Output Load		C_L=100pF + 1TTL Load

AC TEST LOADS



NOTE:
1. Including jig and scope capacitance.

CAPACITANCE

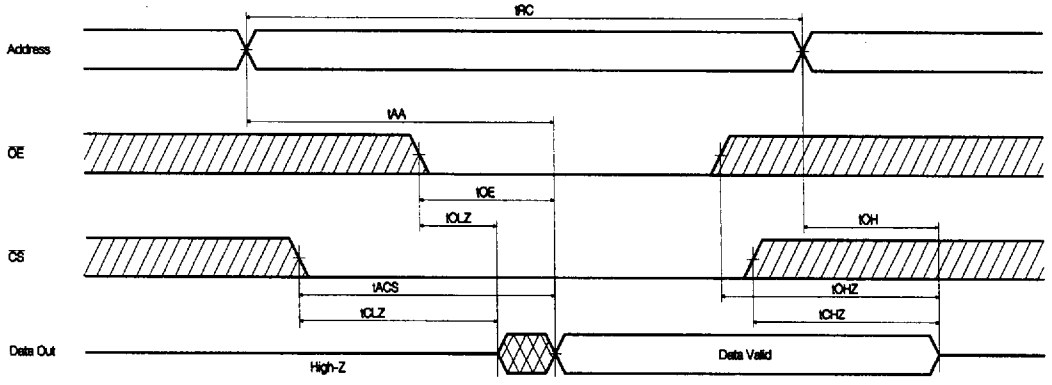
(T_A=25°C, f= 1MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$=0V	8	pF

Note:
1. This parameter is sampled and not 100% tested.

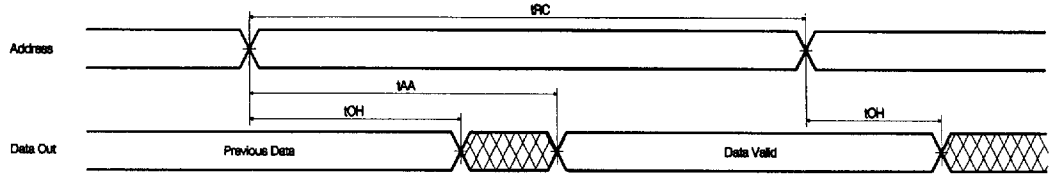
TIMING DIAGRAM

READ CYCLE 1



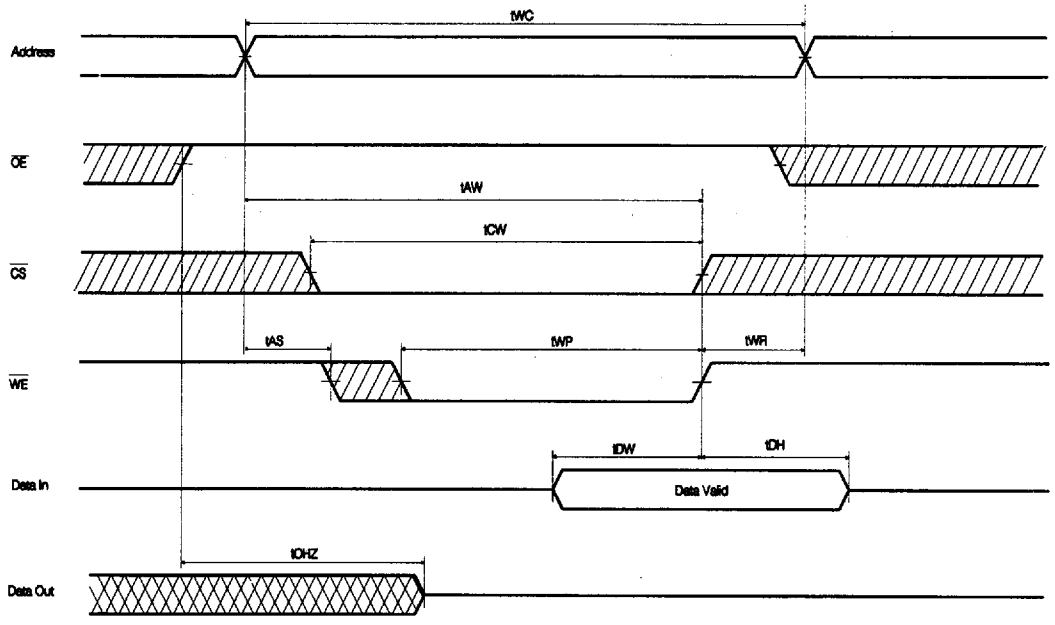
Note (READ CYCLE):
1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{CHZ} max. is less than t_{CLZ} min. both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.

READ CYCLE 2

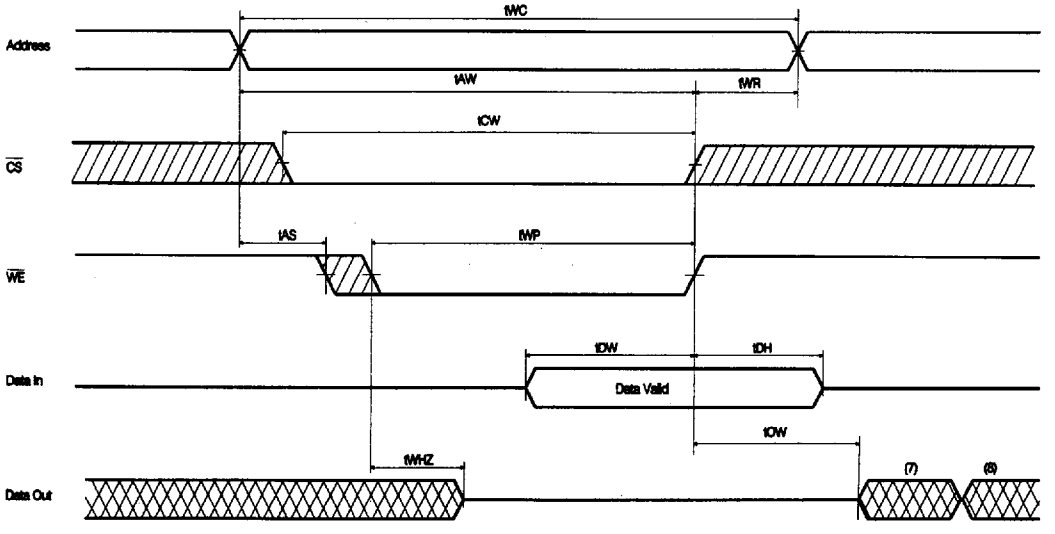


Note(READ CYCLE):
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected $\overline{CS}$=V_{IL}.
3. $\overline{OE}$=V_{IL}.

WRITE CYCLE 1 ($\overline{OE}$ Clocked))



WRITE CYCLE 2($\overline{OE}$ Low Fixed)



Note (WRITE CYCLE):

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low, and $\overline{WE}$ going low: A write ends at the earlist transition among $\overline{CS}$ going high $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
5. If $\overline{OE}$ and $\overline{WE}$ are in the read mode during this period, the I/O pins are in the output low-Z state, inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. D_{OUT} is the same phase of lastest written data in this write cycle.
8. D_{OUT} is the read data of the new address.

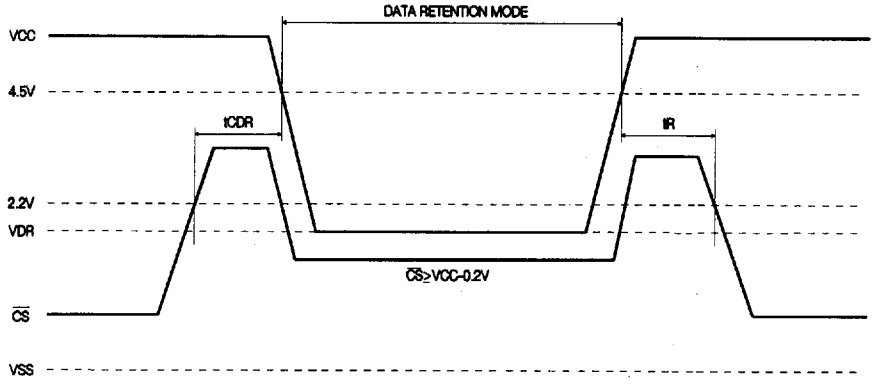
DATA RETENTION CHARACTERISTICS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX	UNIT
t_{DR}	V_{CC} for Data Petention	$\overline{CS} \geq V_{CC}$-0.2, $V_{SS} \leq V_{IN} \leq V_{CC}$	2.0	-	-	V
t_{CCDR}	Data Retention Current	V_{CC}=0.3V, $\overline{CS} \geq V_{CC}$-0.2V $V_{SS} \leq V_{IN} \leq V_{CC}$	-	0.5	15(2)	µA
t_{CDR}	Chip Disable to Data Retention Time	See Data Retention Timing Diagram	0	-	-	ns
t_R	Operating Recovery Time		t_{RC}(3)			ns

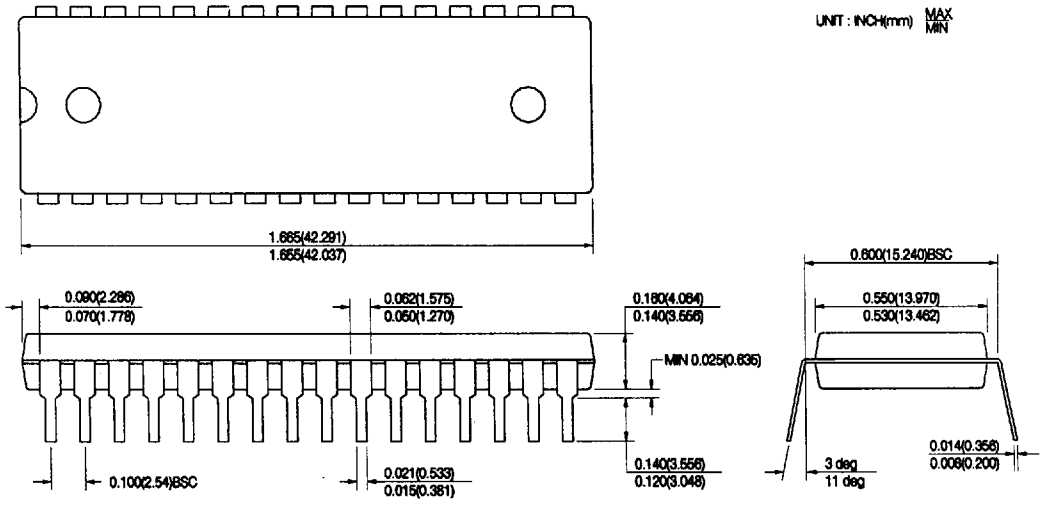
Notes :
1. Typical values are at the condition of T_A=25°C.
2. 3µA max. at T_A= 0°C to 40°C.
3. t_{RC} is read cycle time.

DATA RETENTION TIMING DIAGRAM 1

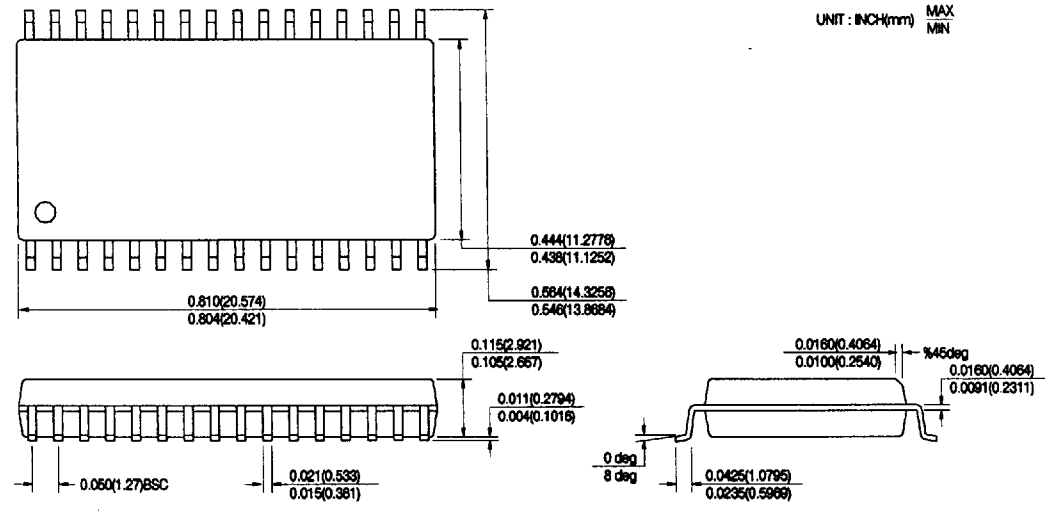


PACKAGE INFORMATION

600 mil 32 pin Plastic Dual In-line Package(P)



525mil 32 pin Small Outline Package (G)



ORDERING INFORMATION

PART NO.	SPEED	POWER	PACKAGE
HY62V8400LP	100/120/150/200	2.7V - 5.5V	PDIP
HY62V8400LG	100/120/150/200	2.7V - 5.5V	SOP
HY62V8400LT2	100/120/150/200	2.7V - 5.5V	TSOP-II Standard
HY62V8400LR2	100/120/150/200	2.7V - 5.5V	TSOP-II Standard