Document Title

512K x 8bit 3.0 ~ 3.6V Super low Power FCMOS Slow SRAM

Revision History

Revision No	History	Draft Date	Remark
00	Initial Draft	Dec.18.2000	Final
01	Changed Logo	Mar.23.2001	Final
02	Changed Isb1 values	Jun.07.2001	Final

DESCRIPTION

The HY62VF08401C is a high speed, super low power and 4Mbit full CMOS SRAM organized as 512K words by 8bits. The HY62VF08401C uses high performance full CMOS process technology and is designed for high speed and low power circuit technology. It is particularly well-suited for the high density low power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 1.2V.

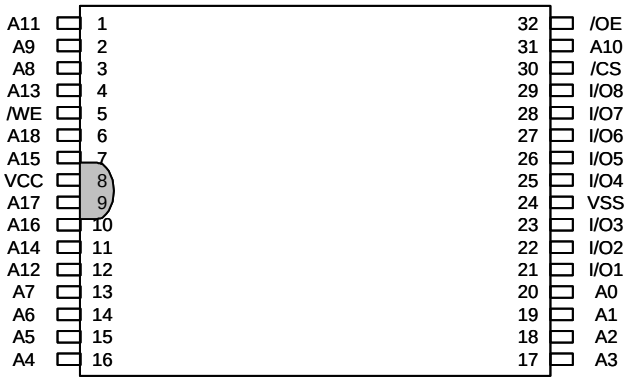
FEATURES

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Battery backup
  -. 1.2V(min) data retention
- Standard pin configuration
  -. 32 - sTSOP - 8X13.4(Standard)

Product No.	Voltage (V)	Speed (ns)	Operation Current/Icc(mA)	Standby Current(uA)		Temperature (°C)
				LL	SL	
HY62VF08401C-I	3.0~3.6	55/70	5	15	6	-40~85

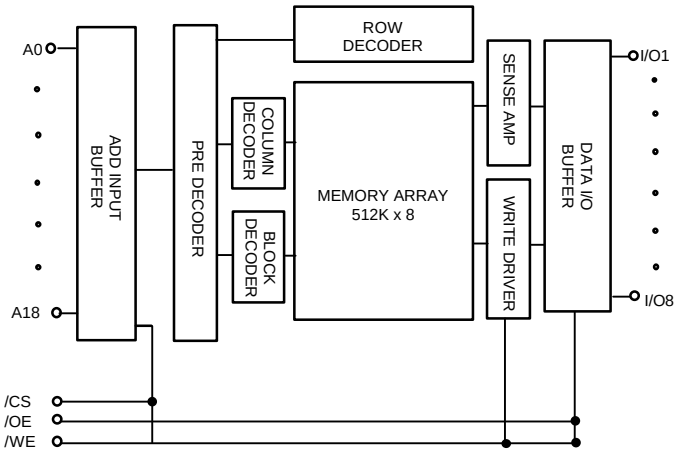
Note 1. I : Industrial
2. Current value is max.

PIN CONNECTION



32-sTSOP Forward

BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Function	Pin Name	Pin Function
/CS	Chip Select	I/O1 ~ I/O8	Data Input/Output
/WE	Write Enable	Vcc	Power (3.0V~3.6V)
/OE	Output Enable	Vss	Ground
A0 ~ A18	Address Input		

ORDERING INFORMATION

Part No.	Speed	Power	Temp[1]	Package
HY62VF08401C-DS(I)	55/70	LL-part	I	sTSOP
HY62VF08401C-SS(I)	55/70	SL-part	I	sTSOP

Note 1. I : Industrial

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Rating	Unit	Remark
V_{IN}, V_{OUT}	Input/Output Voltage	-0.3 to 4.0	V	
Vcc	Power Supply	-0.3 to 4.6	V	
T_A	Operating Temperature	-40 to 85	°C	HY62VF08401C-I
T_{STG}	Storage Temperature	-55 to 150	°C	
P_D	Power Dissipation	1.0	W	
T_{SOLDER}	Ball Soldering Temperature & Time	260 • 10	°C•sec	

Note
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

TRUTH TABLE

/CS	/WE	/OE	MODE	I/O OPERATION	Supply Current
H	X	X	Deselected	High-Z	Standby
L	H	H	Output Disabled	High-Z	Active
		L	Read	Dout	Active
	L	X	Write	Din	

Note:
1. H=V_{IH}, L=V_{IL}, X=don't care (V_{IL} or V_{IH})

RECOMMENDED DC OPERATING CONDITION

Symbol	Parameter	Min.	Typ	Max.	Unit
Vcc	Supply Voltage	3.0	3.3	3.6	V
Vss	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	Vcc+0.3	V
V_{IL}	Input Low Voltage	-0.3[1.]	-	0.6	V

Note : 1. Undershoot : VIL = -1.5V for pulse width less than 30ns
2. Undershoot is sampled, not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = -40°C to 85°C

Sym	Parameter	Test Condition		Min	Typ[1.]	Max	Unit
I_{LI}	Input Leakage Current	Vss ≤ V_{IN} ≤ Vcc		-1	-	1	uA
I_{LO}	Output Leakage Current	Vss ≤ V_{OUT} ≤ Vcc, /CS = V_{IH} or /OE = V_{IH} or /WE = V_{IL}		-1	-	1	uA
Icc	Operating Power Supply Current	/CS = V_{IL}, V_{IN} = V_{IH} or V_{IL}, $I_{I/O}$ = 0mA				5	mA
I_{CC1}	Average Operating Current	/CS = V_{IL}, V_{IN} = V_{IH} or V_{IL}, Cycle Time = Min, 100% Duty, $I_{I/O}$ = 0mA				45	mA
		/CS ≤ 0.2V, V_{IN} ≤ 0.2V or V_{IN} ≥ Vcc-0.2V, Cycle Time = 1us, 100% Duty, $I_{I/O}$ = 0mA				5	mA
I_{SB}	Standby Current (TTL Input)	/CS = V_{IH} or V_{IN} = V_{IH} or V_{IL}				0.5	mA
I_{SB1}	Standby Current (CMOS Input)	/CS ≥ Vcc - 0.2V or V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ Vss + 0.2V	SL		0.2	6	uA
			LL		0.2	15	uA
V_{OL}	Output Low	I_{OL} = 2.1mA		-	-	0.4	V
V_{OH}	Output High	I_{OH} = -1.0mA		2.4	-	-	V

Note
1. Typical values are at Vcc = 3.3V T_A = 25°C
2. Typical values are not 100% tested

CAPACITANCE

(Temp = 25°C, f= 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance (Add, /CS, /WE, /OE)	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance (I/O)	$V_{I/O}$ = 0V	10	pF

Note : These parameters are sampled and not 100% tested

AC CHARACTERISTICS

T_A = -40°C to 85°C, unless otherwise specified

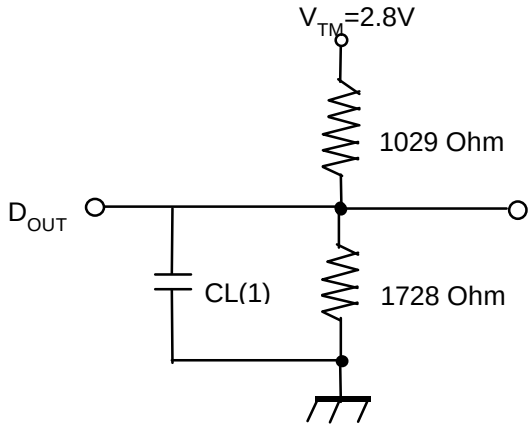
#	Symbol	Parameter	55ns		70ns		Unit
			Min.	Max.	Min.	Max.	
	READ CYCLE						
1	tRC	Read Cycle Time	55	-	70	-	ns
2	tAA	Address Access Time	-	55	-	70	ns
3	tACS	Chip Select Access Time	-	55	-	70	ns
4	tOE	Output Enable to Output Valid	-	30	-	35	ns
5	tCLZ	Chip Select to Output in Low Z	10	-	10	-	ns
6	tOLZ	Output Enable to Output in Low Z	5	-	5	-	ns
7	tCHZ	Chip Deselection to Output in High Z	0	30	0	30	ns
8	tOHZ	Out Disable to Output in High Z	0	30	0	30	ns
9	tOH	Output Hold from Address Change	10	-	10	-	ns
	WRITE CYCLE						
10	tWC	Write Cycle Time	55	-	70	-	ns
11	tCW	Chip Selection to End of Write	50	-	60	-	ns
12	tAW	Address Valid to End of Write	50	-	60	-	ns
13	tAS	Address Set-up Time	0	-	0	-	ns
14	tWP	Write Pulse Width	45	-	50	-	ns
15	tWR	Write Recovery Time	0	-	0	-	ns
16	tWHZ	Write to Output in High Z	0	20	0	20	ns
17	tDW	Data to Write Time Overlap	25	-	30	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	ns
19	tOW	Output Active from End of Write	5	-	5	-	ns

AC TEST CONDITIONS

T_A = -40°C to 85°C, unless otherwise specified

Parameter		Value
Input Pulse Level		0.4V to 2.2V
Input Rise and Fall Time		5ns
Input and Output Timing Reference Level		1.5V
Output Load	tCLZ, tOLZ, tCHZ, tOHZ, tWHZ, tOW	CL = 5pF + 1TTL Load
	Others	CL = 30pF + 1TTL Load

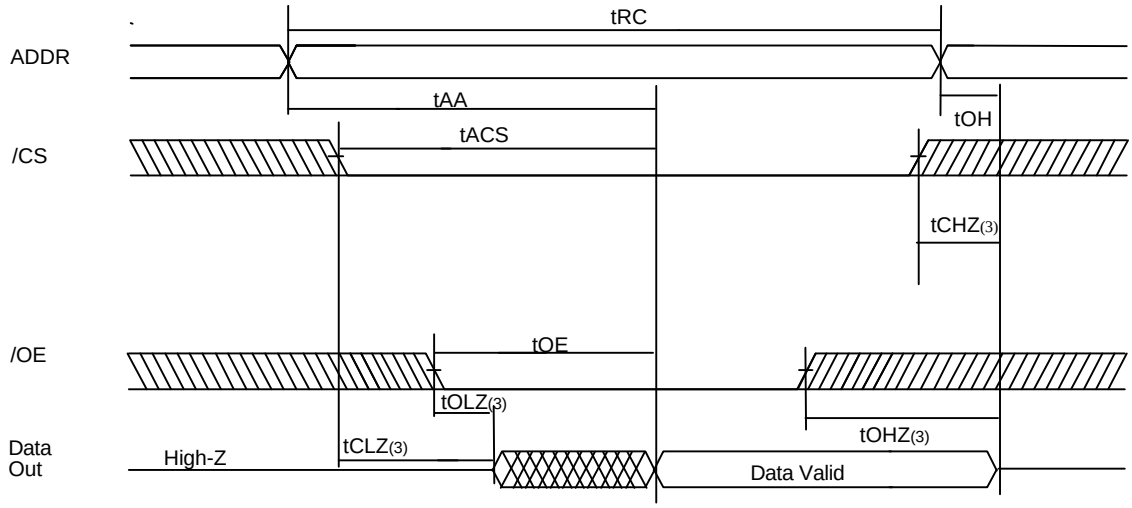
AC TEST LOADS



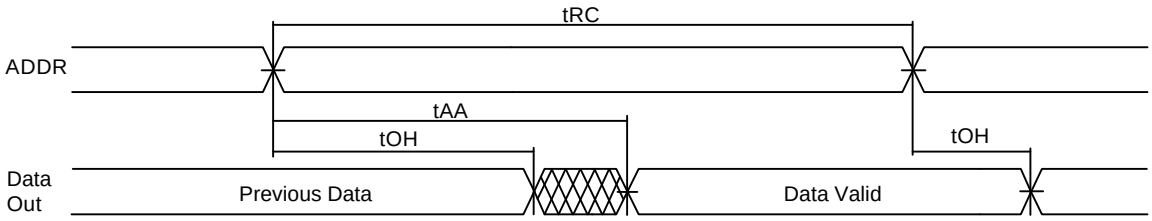
Note
1. Including jig and scope capacitance

TIMING DIAGRAM

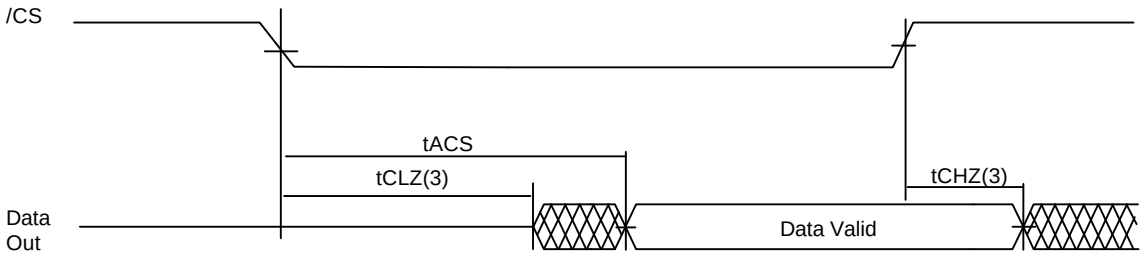
READ CYCLE 1 (Note 1,4)



READ CYCLE 2 (Note 1,2,4)

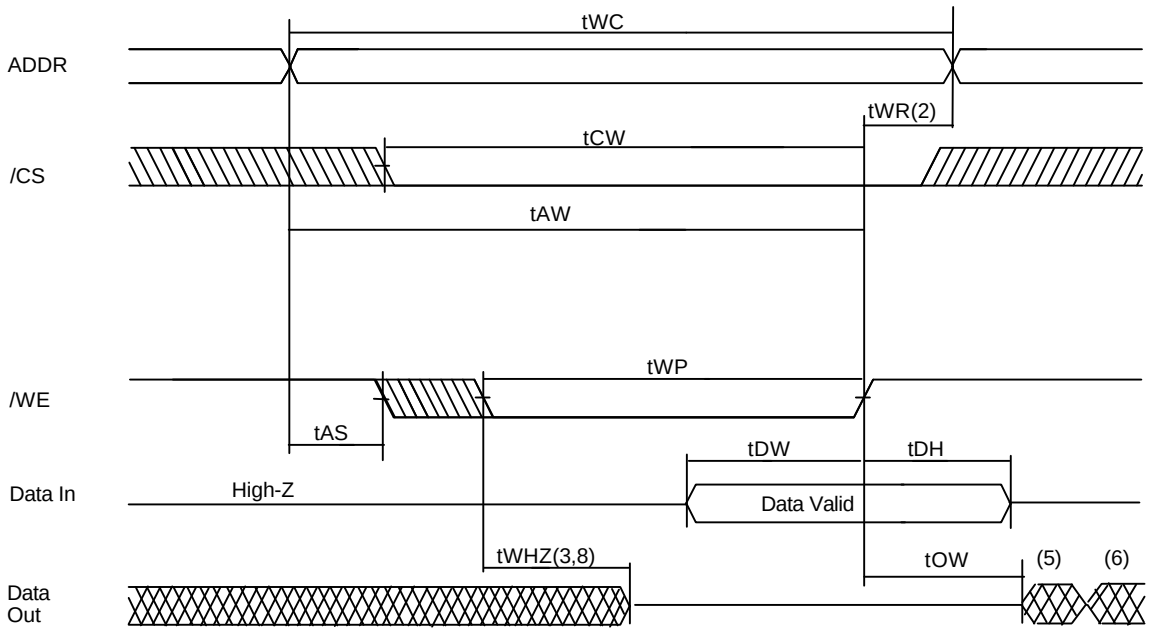


READ CYCLE 3(Note 1,2,4)

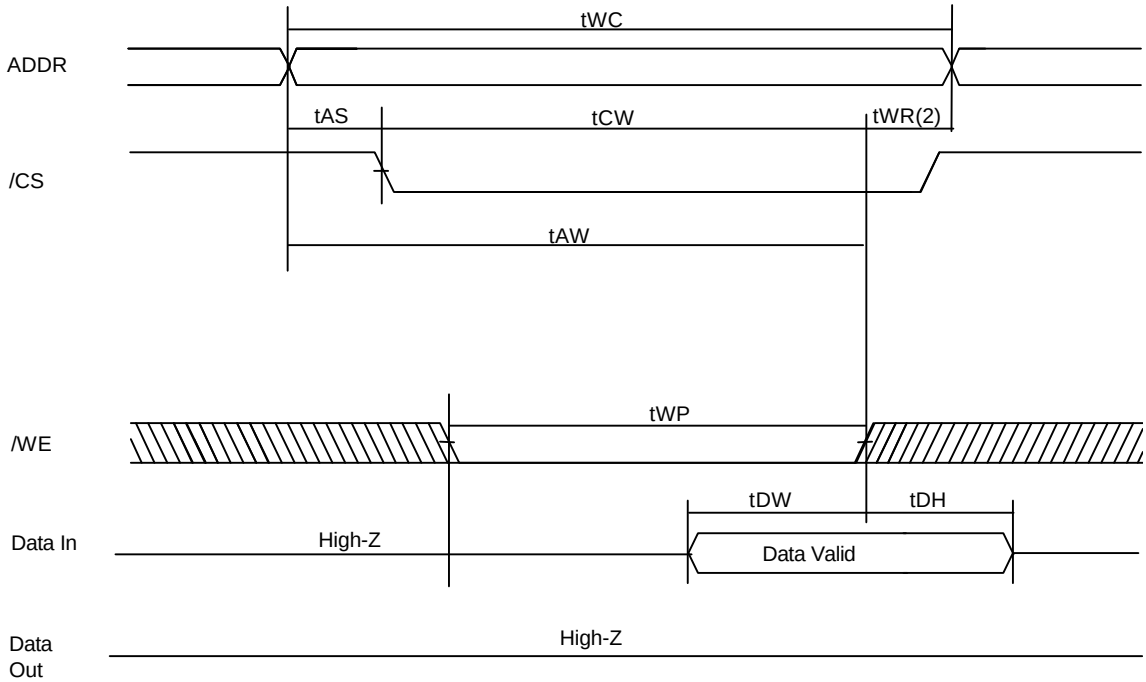


Notes:
1. A read occurs during the overlap of a low /OE, a high /WE and a low /CS.
2. /OE = V_{IL}
3. Transition is measured ± 200mV from steady state voltage.
   This parameter is sampled and not 100% tested.
4. /CS in high for the standby, low for active

WRITE CYCLE 1(1,4,8) (/WE Controlled)



WRITE CYCLE 2 (Note 1,4,8) (/CS Controlled)



Notes:
1. A write occurs during the overlap of a low /WE and a low /CS.
2. tWR is measured from the earlier of /CS or /WE going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the /CS low transition occurs simultaneously with the /WE low transition or after the /WE transition, outputs remain in a high impedance state.
5. Q(data out) is the same phase with the write data of this write cycle.
6. Q(data out) is the read data of the next address.
7. Transition is measured ± 200mV from steady state. This parameter is sampled and not 100% tested.
8. /CS in high for the standby, low for active

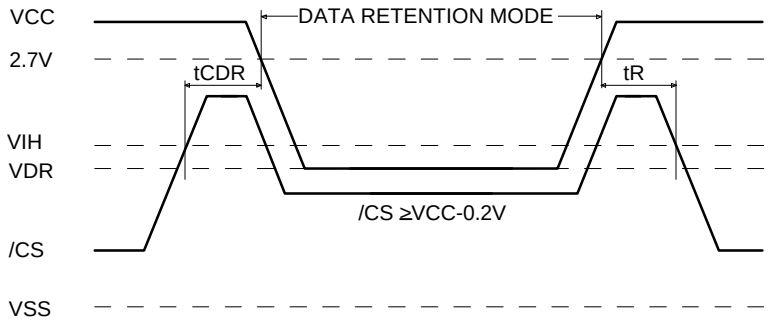
DATA RETENTION ELECTRIC CHARACTERISTIC

T_A = -40°C to 85°C

Symbol	Parameter	Test Condition		Min	Typ[1.]	Max	Unit
V_{DR}	Vcc for Data Retention	/CS ≥ Vcc - 0.2V, V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ Vss + 0.2V		1.2	-	3.6	V
Iccdr	Data Retention Current	Vcc=1.5V, /CS ≥ Vcc - 0.2V or V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ Vss + 0.2V	SL	-	0.1	3	uA
			LL	-	0.1	10	uA
tCDR	Chip Deselect to Data Retention Time	See Data Retention Timing Diagram		0	-	-	ns
tR	Operating Recovery Time			tRC	-	-	ns

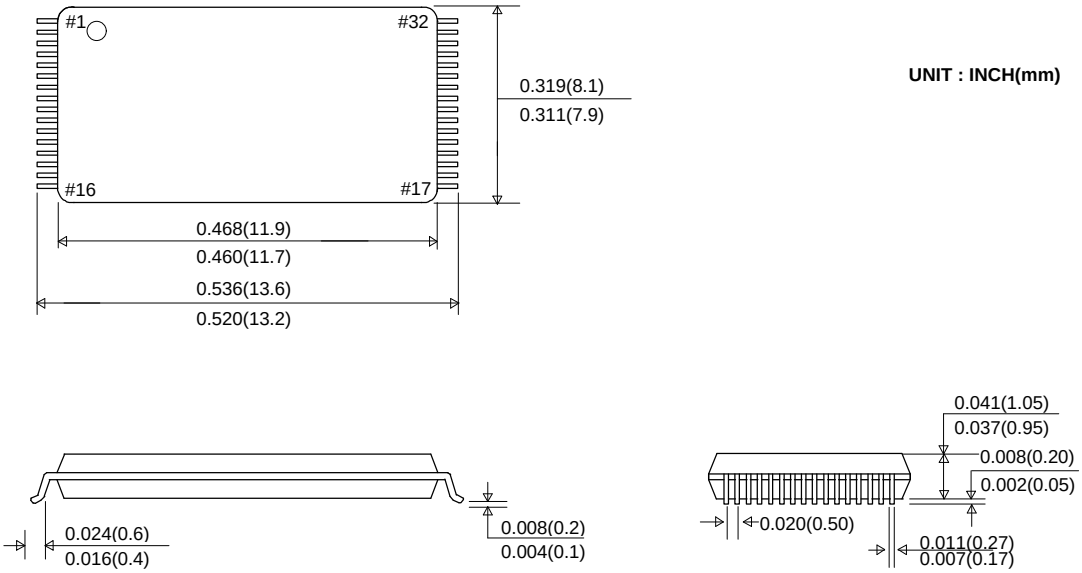
Notes:
1. Typical values are under the condition of T_A = 25°C.
2. Typical value are sampled and not 100% tested

DATA RETENTION TIMING DIAGRAM



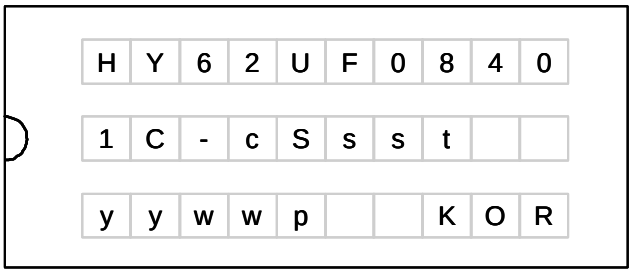
PACKAGE INFORMATION

32pin 8x13.4mm Smaller Thin Small Outline Package Standard(ST)



UNIT : INCH(mm)

MARKING INFORMATION

Package	Marking Example
sTSOP	

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- **HY62UF08401C** : Part Name
- **c** : Power Consumption
  - D : Low Low Power
  - S : Super Low Power
- **S** : Package Type
  - S : sTSOP
- **ss** : Speed
  - 55 : 55ns
  - 70 : 70ns
- **t** : Temperature
  - I : Industrial (-40 ~ 85 °C)
- **yy** : Year (ex : 00 = year 2000, 01 = year 2001)
- **ww** : work week (ex : 12 = ww12)
- **p** : Process Code
- **KOR** : Origin Country

Note

- Capital Letter : Fixed Item
- Small Letter : Non-fixed Item