HYB25L512160AC–7.5

512MBit Mobile-RAM

Standard Temperature Range

Memory Products

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Page	Subjects (major changes since last revision)
all	Delete extended temperature range (HYE25L512160AC–7.5)

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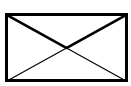

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1 Overview

1.1 Features

- 2 x 4 banks x 4 Mbit x 16 organisation (Two 256MBit chips stacked in multi-chip package)
- Fully synchronous to positive clock edge
- Four internal banks for concurrent operation
- Programmable CAS latency: 2, 3
- Programmable burst length: 1, 2, 4, 8 or full page
- Programmable wrap sequence: sequential or interleaved
- Auto refresh and self refresh modes
- 8192 refresh cycles / 64ms
- Auto precharge
- Operating temperature range
  Commerical (0°C to +70°C)
  54-ball FBGA package (12.0 mm x 8.0 mm x 1.4 mm)

Power Saving Features:

- Low supply voltages:
  V_{DD} = 2.3V .. 3.6V, V_{DDQ} = 1.65V .. 1.95V or 2.3V .. 3.6V
- Optimized self refresh (ICC6) and standby currents (I_{CC2} / I_{CC3})
- Programmable Partial Array Self Refresh (PASR)
- Temperature Compensated Self-Refresh (TCSR), controllable by on-chip temperature sensor
- Power-Down and Deep Power Down modes

Table 1 Performance

Part Number Speed Code		–7.5		Unit
V_{DDQ}		1.65 ...1.95	2.3 ...3.6	V
Clock Frequency (f_{CKmax})		105	133	MHz
Access Time (t_{ACmax})	CL = 2 or 3	8.0	6.0	ns
Clock Cycle Time (t_{CKmin})	CL = 3	9.5	7.5	ns
	CL = 2	9.5	9.5	ns

Table 2 Memory Addressing Scheme

Item	Addresses
Banks	BA0, BA1
Rows	A0 - A12
Columns	A0 - A8

1.2 Description

The HYB25L512160AC consists of two 256MBit high-speed CMOS, dynamic random-access memories each of them containing 268,435,456 bits. Each chip is internally configured as a quad-bank DRAM.

The HYB25L512160AC achieves high speed data transfer rates by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to the system clock. Read and write accesses are burst-oriented; accesses start at a selected location and continue for a programmed number of locations (1, 2, 4, 8 or full page) in a programmed sequence.

The device operation is fully synchronous: all inputs are registered at the positive edge of CLK.

The HYB25L512160AC is especially designed for mobile applications: it adds many features to save power, like low operating voltages. Additionally, current consumption in self refresh mode can further be reduced by using the programmable Partial Array Self Refresh (PASR) and Temperature Compensated Self Refresh (TCSR).

A conventional data-retaining power down (PD) mode is available as well as a non-data-retaining deep power down (DPD) mode.

The HYB25L512160AC is housed in a 54-ball “chip-size” FBGA package. It is available in Commercial (0°C to 70°C) temperature range.

Table 3 Ordering Information

Type[1)]	Description	Package
Commercial Temperature Range		
HYB25L512160AC–7.5	133 MHz 2 × 4 Banks × 4 Mbit × 16 LP-SDRAM	FBGA-54

1) HYB: Designator for memory products (HYB: standard temp. range)
25L: 2.5V Mobile-RAM
512: 512 MBit density
160: 16 bit interface width
A: die revision
C : lead-containing product

2 Pin Configuration

1	2	3		7	8	9
V_{SS}	DQ15	V_{SSQ}	A	V_{DDQ}	DQ0	V_{DD}
DQ14	DQ13	V_{DDQ}	B	V_{SSQ}	DQ2	DQ1
DQ12	DQ11	V_{SSQ}	C	V_{DDQ}	DQ4	DQ3
DQ10	DQ9	V_{DDQ}	D	V_{SSQ}	DQ6	DQ5
DQ8	$\overline{CS1}$	V_{SS}	E	V_{DD}	LDQS	DQ7
UDQM	CLK	CKE	F	$\overline{CAS}$	$\overline{RAS}$	$\overline{WE}$
A12	A11	A9	G	BA0	BA1	$\overline{CS0}$
A8	A7	A6	H	A0	A1	A10/AP
V_{SS}	A5	A4	J	A3	A2	V_{DD}

MPPD0050

Figure 1 Standard Ballout 512M Mobile-RAM

Note

1. 54 - Ball FBGA Package (Top View)

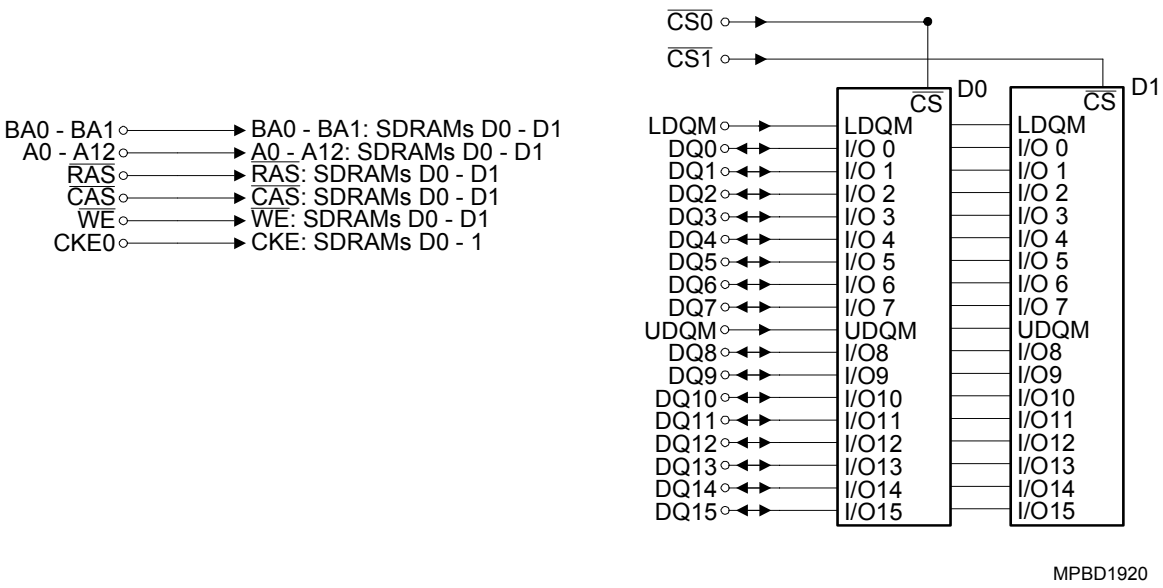


Figure 2 Block Diagram of Stacked Configuration

2.1 Pin Description

Table 4 Pin Description

Symbol	Type	Function
CLK	Input	**Clock:** all inputs are sampled on the positive edge of CLK.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals, device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), ACTIVE POWER-DOWN (row active in any bank) or SUSPEND (access in progress). Input buffers, excluding CLK and CKE are disabled during POWER-DOWN and SELF-REFRESH.
$\overline{CS}$ ($\overline{CS0}$, $\overline{CS1}$)	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple memory banks. $\overline{CS}$ is considered part of the command code
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DQ0 - DQ15	I/O	**Data Inputs/Output:** Bi-directional data bus (16 bit)
DQM (LDQM, UDQM)	Input	**Input/Output Mask:** input mask signal for WRITE cycles and output enable for READ cycles. For WRITEs, DQM acts as a data mask when HIGH. For READs, DQM acts as an output enable and places the output buffers in High-Z state when HIGH (two clocks latency) . LDQM corresponds to DQ0 - DQ7, UDQM corresponds to DQ8 - DQ15.
BA0, BA1	Input	**Bank Address Inputs:** BA0 and BA1 define to which bank an ACTIVATE, READ, WRITE or PRECHARGE command is being applied. BA0, BA1 also determine which mode register is to be loaded during a MODE REGISTER SET command (MRS or EMRS).
A0 - A12	Input	**Address Inputs:** A0 - A12 define the row address during an ACTIVE command cycle. A0 - A8 define the column address during a READ or WRITE command cycle. In addition, A10 (= AP) controls Auto Precharge operation at the end of the burst read or write cycle. During a PRECHARGE command, A10 (= AP) in conjunction with BA0, BA1 controls which bank(s) are to be precharged: if A10 is HIGH, all four banks will be precharged regardless of the state of BA0 and BA1; if A10 is LOW, BA0, BA1 define the bank to be precharged. During MODE REGISTER SET commands, the address inputs hold the op-code to be loaded.
V_{DDQ}	Supply	**I/O Power Supply:** Isolated power for DQ output buffers for improved noise immunity: V_{DDQ} = 1.65V..1.95V; or 2.3V..3.6V
V_{SSQ}	Supply	I/O Ground
V_{DD}	Supply	**Power Supply:** Power for the core logic and input buffers. V_{DD} = 2.3V..3.6V
V_{SS}	Supply	Ground

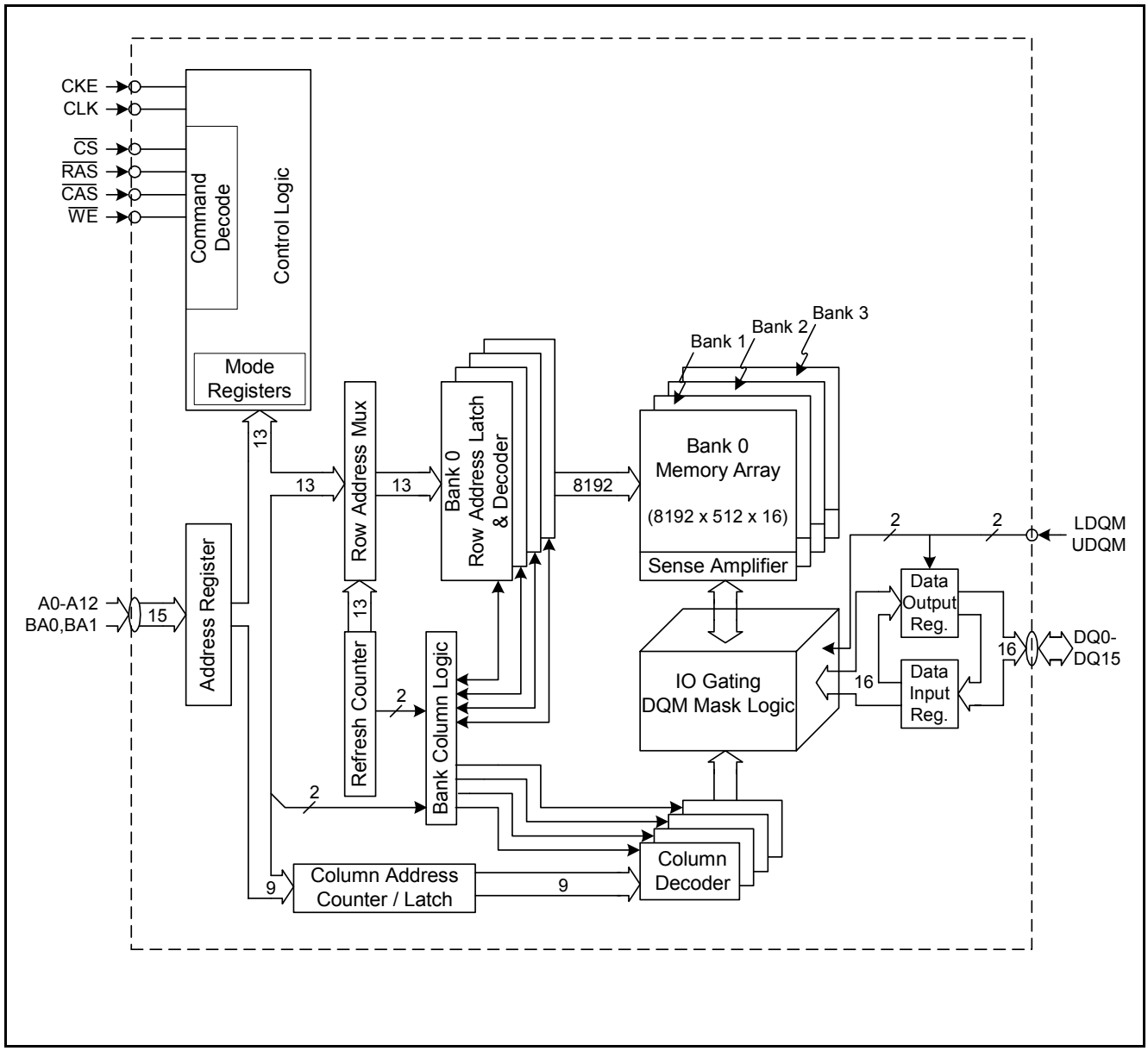


Figure 3 Functional Block Diagram

3 Functional Description

The 512 Mbit Mobile-RAM consists of two 256MBit high-speed CMOS, dynamic random-access memories each of them containing 268,435,456 bits. Each chip is internally configured as a quad-bank DRAM.

READ and WRITE accesses to the Mobile-RAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the banks, A0 - A12 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the Mobile-RAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command description and device operation.

3.1 Power On and Initialization

The Mobile-RAM must be powered up and initialized in a predefined manner (see **Figure 4**). Operational procedures other than those specified may result in undefined operation.

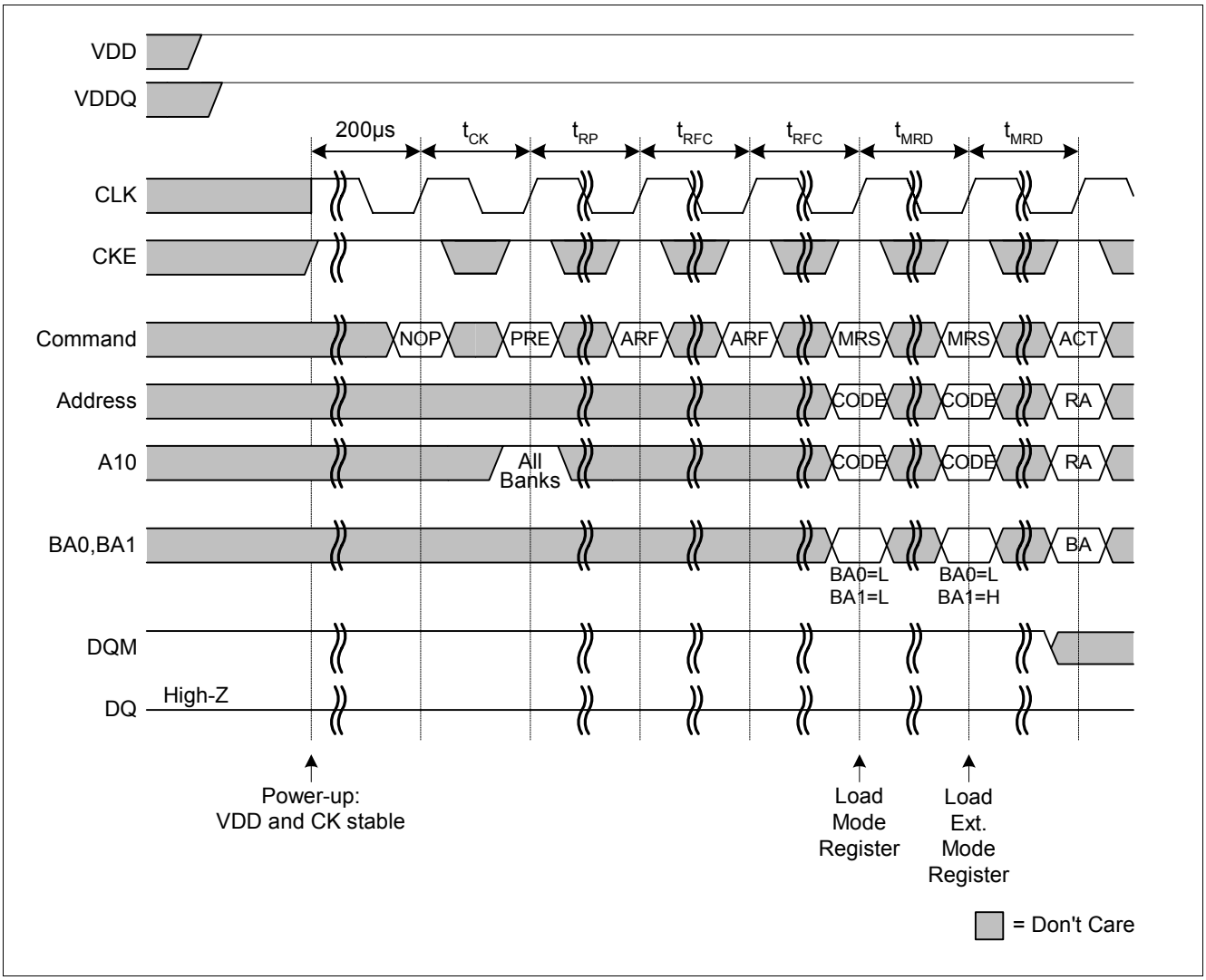


Figure 4 Power-Up Sequence and Mode Register Sets

No power sequencing is specified during power up or power down provided that one of the following two criteria is met:

- V_{DD} and V_{DDQ} are driven from a single power converter output
- V_{DDQ} is driven after or with V_{DD} such that $V_{DDQ} < V_{DD} + 0.3$ V

After all power supply voltages are stable, and the clock is stable, the Mobile-RAM requires a 200µs delay prior to applying a command other than DESELECT or NOP. CKE and DQM must be held high throughout the entire power-up sequence. Once the 200µs delay has been satisfied, the following command sequence shall be applied (see **Figure 4**):

- a PRECHARGE ALL command;
- at least 8 AUTO REFRESH commands;
- two MODE REGISTER SET commands for the Mode Register and Extended Mode Register

Following these cycles, the Mobile-RAM is ready for normal operation.

3.2 Register Definition

3.2.1 Mode Register

The Mode Register is used to define the specific mode of operation of the Mobile-RAM. This definition includes the selection of a burst length, a burst type, a CAS latency, and a write burst mode. The Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power.

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Bus
0	0	0	0	0	WB	0	0	CAS Latency			BT	Burst Length			Mode Register

A9	Write Burst Mode
0	Burst Write
1	Single Write

A3	Burst Type
0	Sequential
1	Interleave

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	
1	1	0	
1	1	1	

A2	A1	A0	Burst Length	
			Sequential	Interleave
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1		
1	1	0		
1	1	1	full page	

Figure 5 Mode Register Definition

Address bits A0-A2 specify the burst length, A3 the burst type, A4-A6 the CAS latency, A9 the write burst mode, while bits A7-A8 and A10-A12 shall be written to zero.

The Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements results in unspecified operation.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

3.2.1.1 Burst Length

READ and WRITE accesses to the Mobile-RAM are burst oriented, with the burst length being programmable. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4, 8 locations are available for both the sequential and interleaved burst types, and a full-page burst mode is available for the sequential burst type.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst wraps within the block if a boundary is reached. The block is uniquely selected by A1-A8 when the burst length is set to two, by A2-A8 when the burst length is set to four and by A3-A8 when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block.

Full page bursts wrap within the page if the boundary is reached. Please note that full page bursts do not self-terminate; this implies that full-page read or write bursts with Auto Precharge are not legal commands.

Table 5 Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
	A2	A1	A0	Sequential	Interleaved
2			0	0 - 1	0 - 1
			1	1 - 0	1 - 0
4		0	0	0 - 1 - 2 - 3	0 - 1 - 2 - 3
		0	1	1 - 2 - 3 - 0	1 - 0 - 3 - 2
		1	0	2 - 3 - 0 - 1	2 - 3 - 0 - 1
		1	1	3 - 0 - 1 - 2	3 - 2 - 1 - 0
8	0	0	0	0 - 1 - 2 - 3 - 4 - 5 - 6 - 7	0 - 1 - 2 - 3 - 4 - 5 - 6 - 7
	0	0	1	1 - 2 - 3 - 4 - 5 - 6 - 7 - 0	1 - 0 - 3 - 2 - 5 - 4 - 7 - 6
	0	1	0	2 - 3 - 4 - 5 - 6 - 7 - 0 - 1	2 - 3 - 0 - 1 - 6 - 7 - 4 - 5
	0	1	1	3 - 4 - 5 - 6 - 7 - 0 - 1 - 2	3 - 2 - 1 - 0 - 7 - 6 - 5 - 4
	1	0	0	4 - 5 - 6 - 7 - 0 - 1 - 2 - 3	4 - 5 - 6 - 7 - 0 - 1 - 2 - 3
	1	0	1	5 - 6 - 7 - 0 - 1 - 2 - 3 - 4	5 - 4 - 7 - 6 - 1 - 0 - 3 - 2
	1	1	0	6 - 7 - 0 - 1 - 2 - 3 - 4 - 5	6 - 7 - 4 - 5 - 2 - 3 - 0 - 1
	1	1	1	7 - 0 - 1 - 2 - 3 - 4 - 5 - 6	7 - 6 - 5 - 4 - 3 - 2 - 1 - 0
Full Page	n	n	n	Cn, Cn+1, Cn+2, ...	not supported

Note:

1. *For a burst length of two, A1-Ai select the two-data-element block; A0 selects the first access within the block.*
2. *For a burst length of four, A2-Ai select the four-data-element block; A0-A1 select the first access within the block.*
3. *For a burst length of eight, A3-Ai select the eight-data-element block; A0-A2 select the first access within the block.*
4. *For a full page burst, A0-Ai select the starting data element.*
5. *Whenever a boundary of the block is reached within a given sequence, the following access wraps within the block.*

3.2.1.2 Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in **Table 5**.

3.2.1.3 CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be programmed to 2 or 3 clocks.

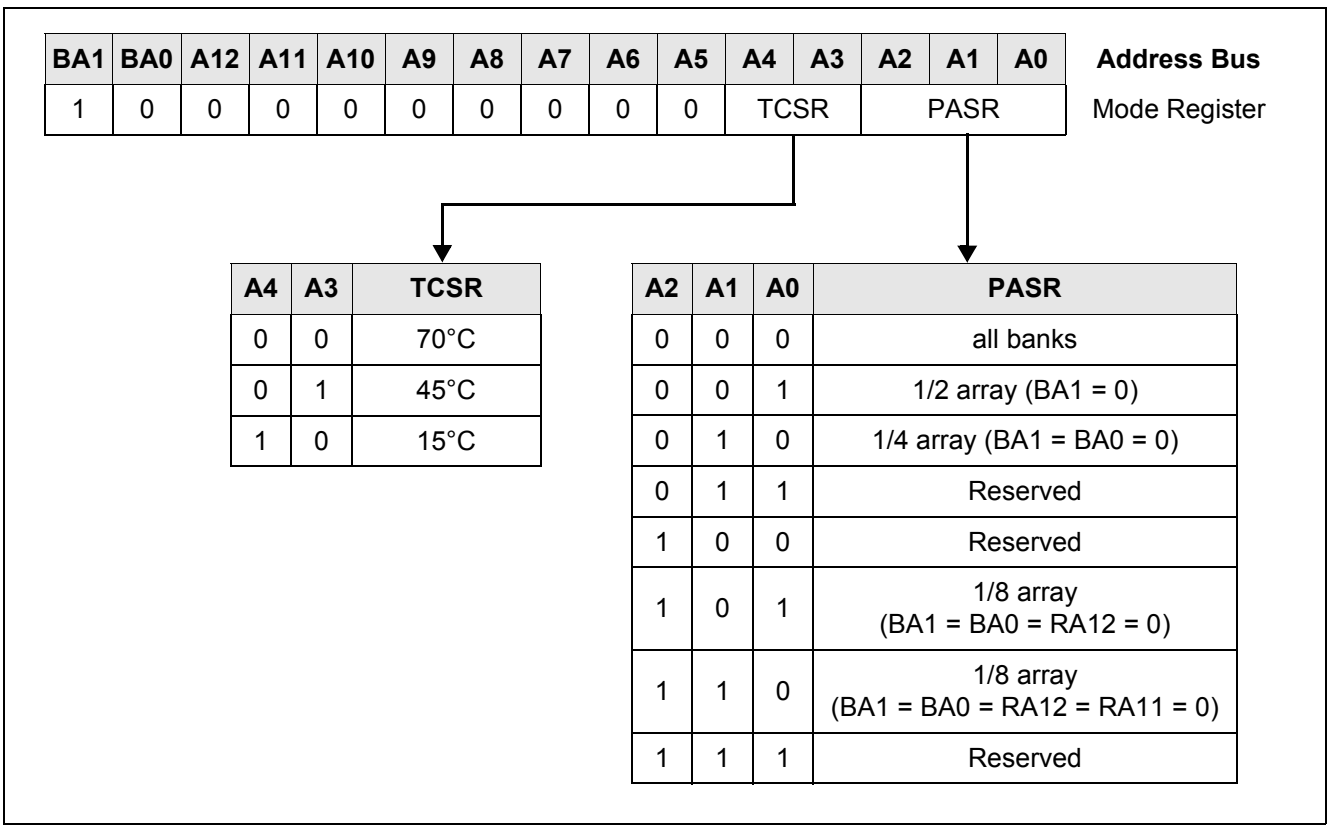
If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available with clock edge *n* + *m* (for details please refer to the READ command description).

3.2.1.4 Write Burst Mode

When A9 = 0, the burst length programmed via A0-A2 applies to both read and write bursts; when A9 = 1, write accesses consist of single data elements only.

3.2.2 Extended Mode Register

The Extended Mode Register controls additional low power features of the device. These include the Partial Array Self Refresh (PASR) and the Temperature Compensated Self Refresh (TCSR). The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 1) and will retain the stored information until it is programmed again or the device loses power. The Extended Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements result in unspecified operation.



BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Bus
1	0	0	0	0	0	0	0	0	0	TCSR		PASR			Mode Register

A4	A3	TCSR
0	0	70°C
0	1	45°C
1	0	15°C

A2	A1	A0	PASR
0	0	0	all banks
0	0	1	1/2 array (BA1 = 0)
0	1	0	1/4 array (BA1 = BA0 = 0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	1/8 array (BA1 = BA0 = RA12 = 0)
1	1	0	1/8 array (BA1 = BA0 = RA12 = RA11 = 0)
1	1	1	Reserved

Figure 6 Extended Mode Register Definition

Address bits A0-A2 specify the Partial Array Self Refresh (PASR) and bits A3-A4 the Temperature Compensated Self Refresh (TCSR), while bits A5-A12 shall be written to zero.

3.2.2.1 Partial Array Self Refresh (PASR)

Partial Array Self Refresh is power-saving feature specific to Mobile-RAMs. With PASR, self refresh may be restricted to variable portions of the total array. The selection comprises all four banks (default), two banks, one bank, half a bank, and a quarter of one bank. Data written to the non activated memory sections will get lost after a period defined by t_{REF} (cf. **Table 13**).

3.2.2.2 Temperature Compensated Self Refresh (TCSR) with On-Chip Temperature Sensor

DRAM devices store data as a electrical charge in tiny capacitors that require a periodic refresh in order to retain the stored information. This refresh requirement heavily depends on the die temperature: high temperature corresponds to short refresh period, and low temperature to long refresh period.

The Mobile-RAM is equipped with an on-chip temperature sensor which continuously monitors the current die temperature and adjusts the refresh period in self refresh mode accordingly. By default the on-chip temperature sensor is enabled (TCSR = 00, see **Figure 6**); the other three TCSR settings use defined temperature values to adjust the self refresh period with the on-chip temperature sensor being disabled.

3.3 State Diagram

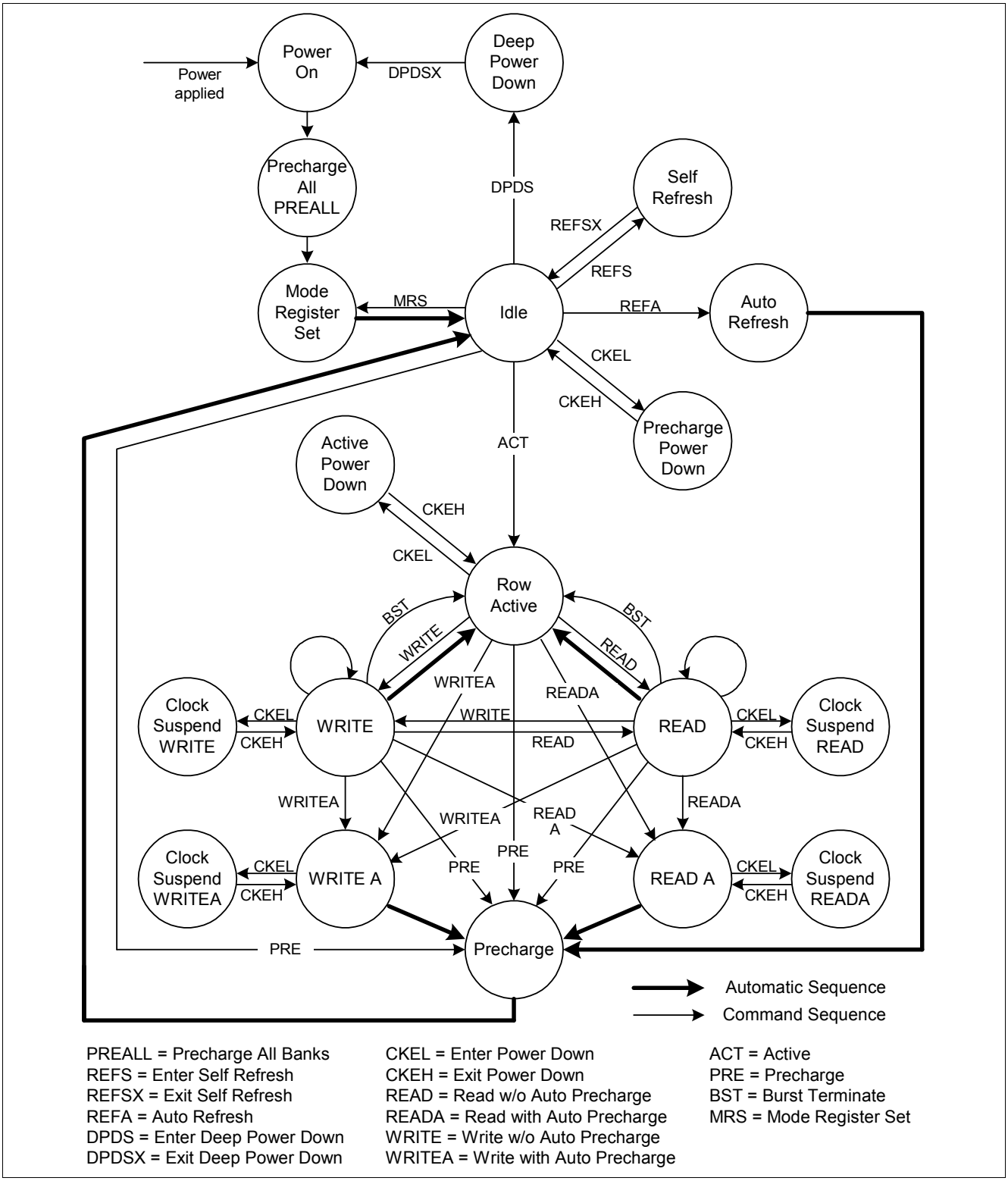


Figure 7 State Diagram

3.4 Commands

Table 6 Command Overview

Command		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	Address	Notes
NOP	DESELECT	H	X	X	X	X	X	1)
	NO OPERATION	L	H	H	H	X	X	1)
ACT	ACTIVE (Select bank and row)	L	L	H	H	X	Bank / Row	2)
RD	READ (Select bank and column and start read burst)	L	H	L	H	L/H	Bank / Col	3)
WR	WRITE (Select bank and column and start write burst)	L	H	L	L	L/H	Bank / Col	3)
BST	BURST TERMINATE or DEEP POWER DOWN	L	H	H	L	X	X	4)
PRE	PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	5)
ARF	AUTO REFRESH or SELF REFRESH (enter self refresh mode)	L	L	L	H	X	X	6)7)
MRS	MODE REGISTER SET	L	L	L	L	X	Op-Code	8)
–	Data Write / Output Enable	—	—	—	—	L	—	9)
–	Write Mask / Output Disable (High-Z)	—	—	—	—	H	—	9)

1) DESELECT and NOP are functionally interchangeable.

2) BA0, BA1 provide bank address, and A0 - A12 provide row address.

3) BA0, BA1 provide bank address, A0 - A8 provide column address; A10 HIGH enables the Auto Precharge feature (nonpersistent), A10 LOW disables the Auto Precharge feature.

4) This command is BURST TERMINATE if CKE is HIGH; DEEP POWER DOWN if CKE is LOW. The BURST TERMINATE command is defined for READ or WRITE bursts with Auto Precharge disabled only.

5) A10 LOW: BA0, BA1 determine which bank is precharged.
A10 HIGH: all banks are precharged and BA0, BA1 are “Don’t Care”.

6) This command is AUTO REFRESH if CKE is HIGH; SELF REFRESH if CKE is LOW.

7) Internal refresh counter controls row and bank addressing; all inputs and I/Os are “Don’t Care” except for CKE.

8) BA0, BA1 select either the Mode Register (BA0 = 0, BA1 = 0) or the Extended Mode Register (BA0 = 0, BA1 = 1); other combinations of BA0, BA1 are reserved; A0 - A12 provide the op-code to be written to the selected mode register.

9) DQM LOW: data present on DQs is written to memory during write cycles; DQ output buffers are enabled during read cycles;
DQM HIGH: data present on DQs are masked and thus not written to memory during write cycles; DQ output buffers are placed in High-Z state (two clocks latency) during read cycles.

Address (A0 - A12, BA0, BA1), write data (DQ0 - DQ15) and command inputs (CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) are all registered on the positive edge of CLK. **Figure 8** shows the basic timing parameters, which apply to all commands and operations.

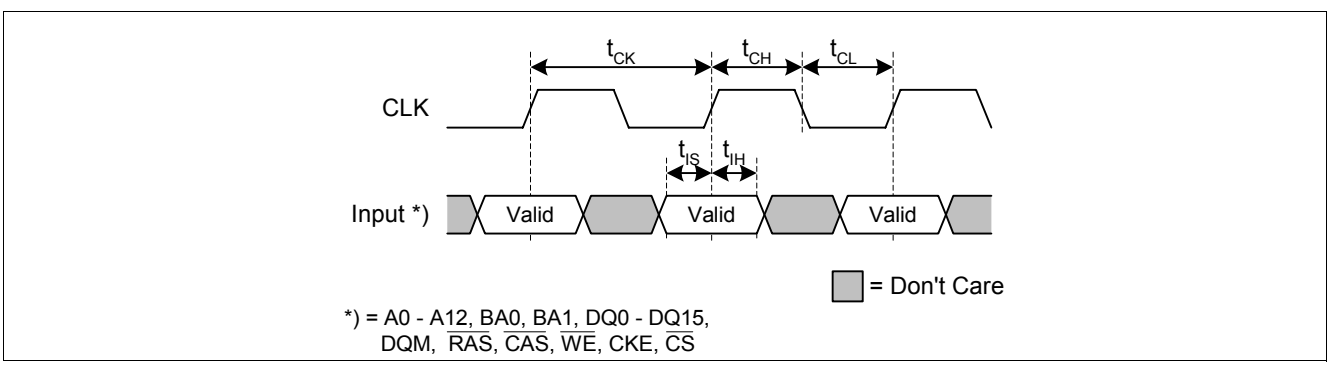


Figure 8 Address / Command Inputs Timing Parameters

Due to shared command, CLK and CKE pins of this stacked configuration, commands issued to one chip may also impact the state of the second chip, even if that chip is actually deselected. Details can be found in the command descriptions below.

Table 7 Inputs Timing Parameters

Parameter			Symbol	–7.5		Unit	Notes
				min	max		
Clock cycle time	V_{DDQ} = 2.3V .. 3.6V	CL = 3	t_{CK}	7.5	—	ns	—
		CL = 2		9.5	—	ns	—
	V_{DDQ} = 1.65V .. 1.95V	CL = 2 or 3		9.5	—	ns	—
Clock frequency	V_{DDQ} = 2.3V .. 3.6V	CL = 3	f_{CK}	—	133	MHz	—
	V_{DDQ} = 1.65V .. 1.95V	CL = 2 or 3	f_{CK}	—	105	MHz	
Clock high-level width			t_{CH}	2.5	—	ns	
Clock low-level width			t_{CL}	2.5	—	ns	
Address, data and command input setup time			t_{IS}	1.5	—	ns	
Address, data and command input hold time			t_{IH}	0.8	—	ns	

3.4.1 No Operation (NOP)

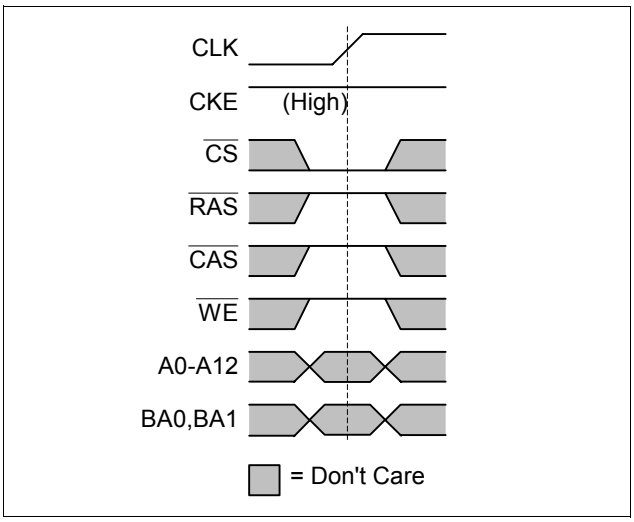


Figure 9 No Operation Command

The NO OPERATION (NOP) command is used to perform a NOP to a Mobile-RAM which is selected ($\overline{CS}$ = LOW). This prevents unwanted commands from being registered during idle states. Operations already in progress are not affected.

3.4.2 DESELECT

The DESELECT function ($\overline{CS}$ = HIGH) prevents new commands from being executed by the Mobile-RAM. The Mobile-RAM is effectively deselected. Operations already in progress are not affected.

When issuing an access command to one chip of this stacked configuration, the other chip shall be deselected by asserting its corresponding $\overline{CS}$ pin HIGH.

3.4.3 MODE REGISTER SET

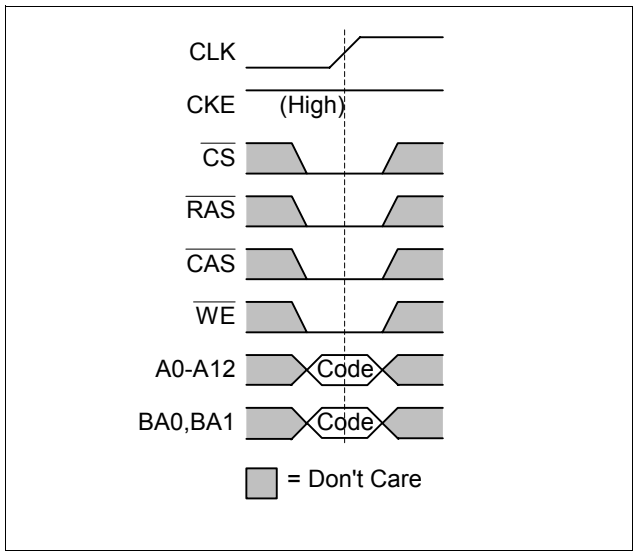


Figure 10 Mode Register Set Command

The mode registers are loaded via inputs A0 - A12 (see mode register descriptions in **Chapter 3.2**). The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress. A subsequent execucommand cannot be issued until t_{MRD} is met. The command may be issued to both chips in parallel ($\overline{CS0}$ = $\overline{CS1}$ = 0).

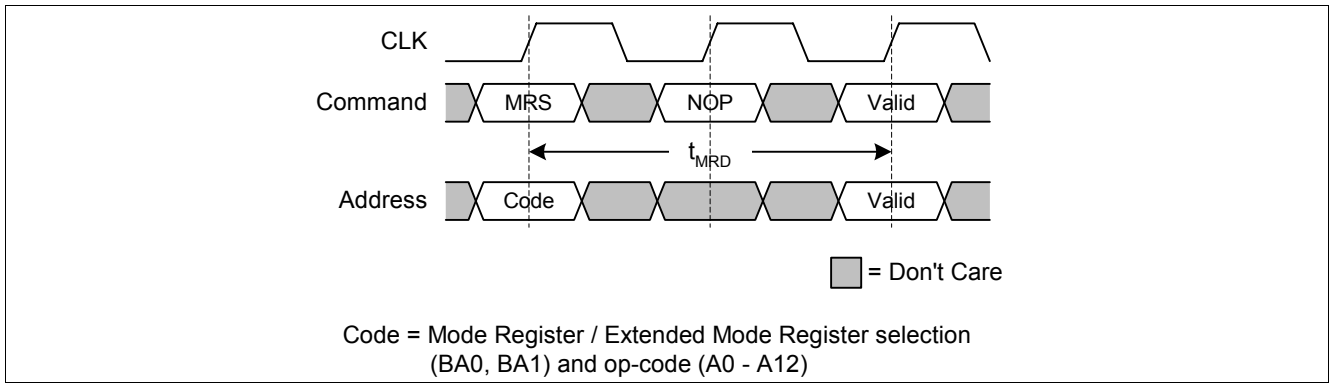


Figure 11 Mode Register Definition

Table 8 Timing Parameters for Mode Register Set Command

Parameter	Symbol	– 7.5		Unit	Notes
		min.	max.		
MODE REGISTER SET command period	t_{MRD}	2	—	t_{CK}	

3.4.4 ACTIVE

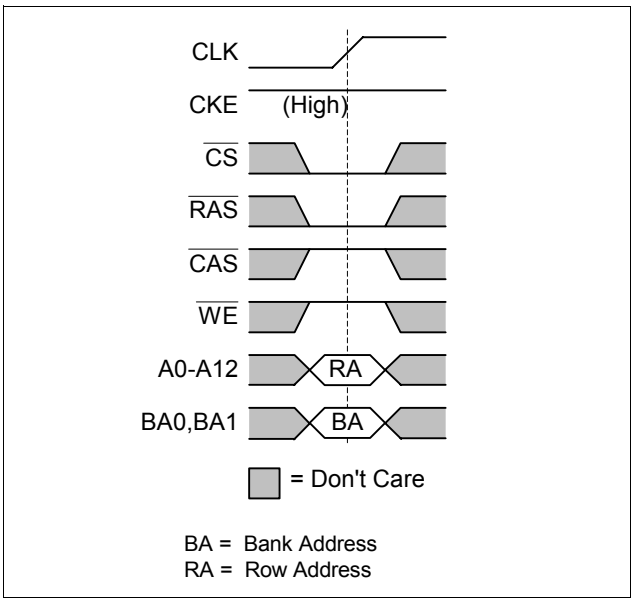


Figure 12 ACTIVE Command

Before any READ or WRITE commands can be issued to a bank within the Mobile-RAM, a row in that bank must be “opened” (activated). This is accomplished via the ACTIVE command and addresses A0 - A12, BA0 and BA1 (see **Figure 12**), which decode and select both the bank and the row to be activated. After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the t_{RCD} specification. A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been “closed” (precharged).

The minimum time interval between successive ACTIVE commands to the same bank is defined by t_{RC}. A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by t_{RRD}.

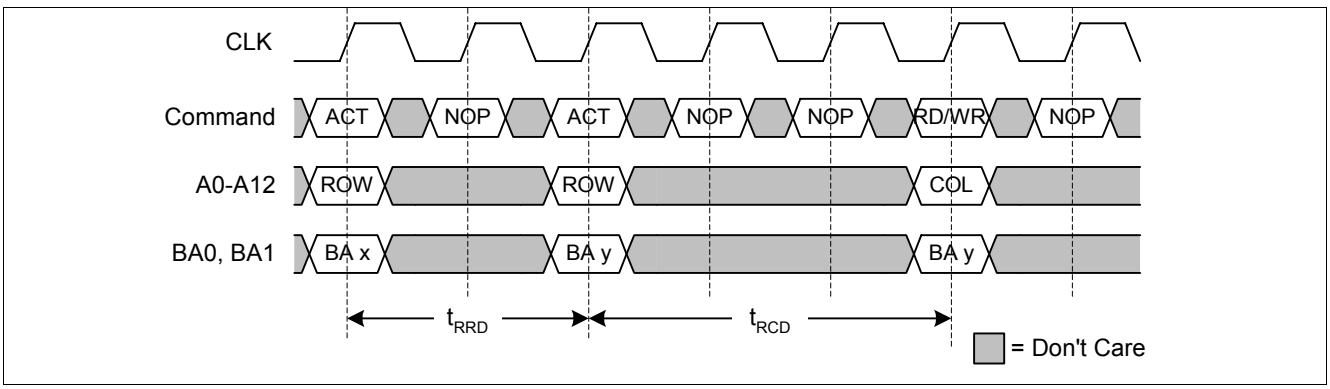


Figure 13 Bank Activate Timings

Table 9 Timing Parameters for Mode Register Set Command

Parameter	Symbol	– 7.5		Unit	Notes
		min.	max.		
ACTIVE to ACTIVE command period	t_{RC}	67	—	ns	1)
ACTIVE to READ or WRITE delay	t_{RCD}	19	—	ns	1)
ACTIVE bank A to ACTIVE bank B delay	t_{RRD}	15	—	ns	1)

1) These parameters account for the number of clock cycles and depend on the operating frequency as follows: no. of clock cycles = specified delay / clock period ; round up to next integer.

3.4.5 READ

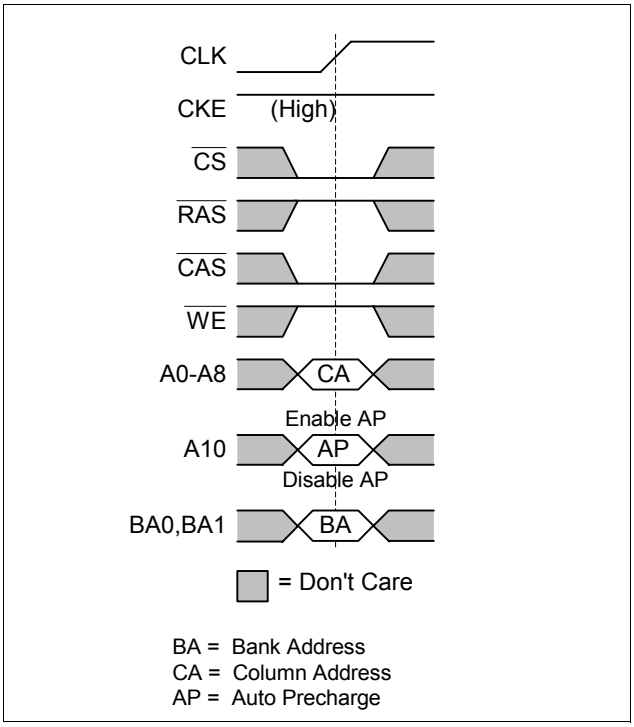


Figure 14 READ Command

Subsequent to programming the mode register with CAS latency and burst length, READ bursts are initiated with a READ command, as shown in Figure 14. Basic timings for the DQs are shown in figure Figure 15; they apply to all read operations and therefore are omitted from all subsequent timing diagrams.

In order to prevent bus contention on the DQs, care must be taken that a READ issued to one chip does not interfere with a READ or WRITE being in progress in the other chip of this stacked configuration.

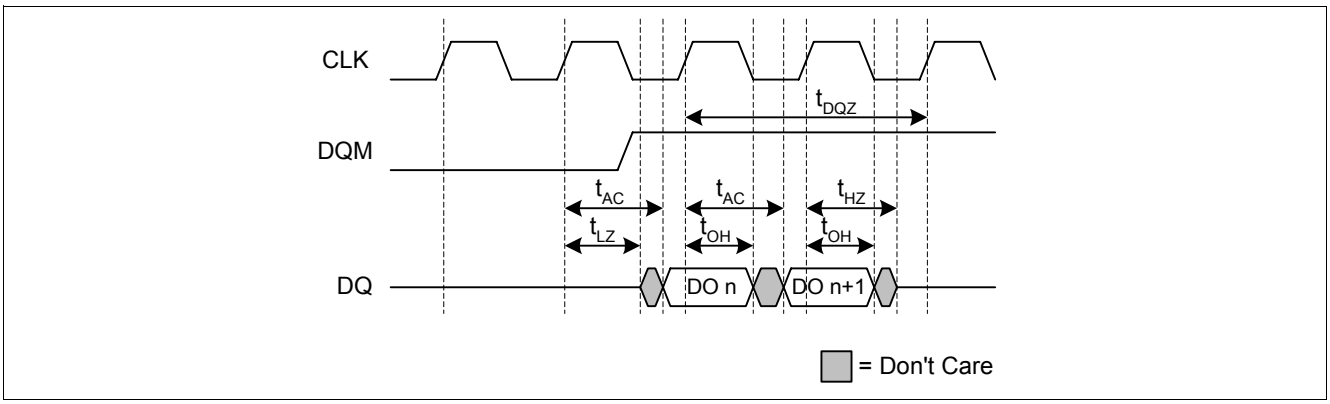


Figure 15 Basic READ Timing Parameters for DQs

Table 10 Timing Parameters for READ

Parameter		Symbol	– 7.5		Unit	Notes
			min.	max.		
Access time from CLK	V_{DDQ} = 2.3V .. 3.6V	t_{AC}	—	6.0	ns	1)
	V_{DDQ} = 1.65V .. 1.95V	t_{AC}	—	8.0	ns	1)
DQ low-impedance time from CLK		t_{LZ}	1.0	—	ns	
DQ high-impedance time from CLK		t_{HZ}	3.0	7.0	ns	
Data out hold time		t_{OH}	3.0	—	ns	
DQM to DQ High-Z delay (READ Commands)		t_{DQZ}	—	2	t_{CK}	
ACTIVE to ACTIVE command period		t_{RC}	67	—	ns	2)
ACTIVE to READ or WRITE delay		t_{RCD}	19	—	ns	2)
ACTIVE to PRECHARGE command period		t_{RAS}	45	100k	ns	2)
PRECHARGE command period		t_{RP}	19	—	ns	2)

1) t_{AC} depends on V_{DDQ} range; no dependency on CAS latency setting

2) These parameters account for the number of clock cycles and depend on the operating frequency as follows: no. of clock cycles = specified delay / clock period ; round up to next integer.

The starting column and bank addresses are provided with the READ command and Auto Precharge is either enabled or disabled for that burst access. If Auto Precharge is enabled, the row being accessed starts precharge at the completion of the burst, provided t_{RAS} has been satisfied. For the generic READ commands used in the following illustrations, Auto Precharge is disabled.

During READ bursts, the valid data-out element from the starting column address is available following the CAS latency after the READ command. Each subsequent data-out element is valid nominally at the next positive clock edge. Upon completion of a READ burst, assuming no other READ command has been initiated, the DQs go to High-Z state.

Figure 16 and **Figure 17** show single READ bursts for each supported CAS latency setting.

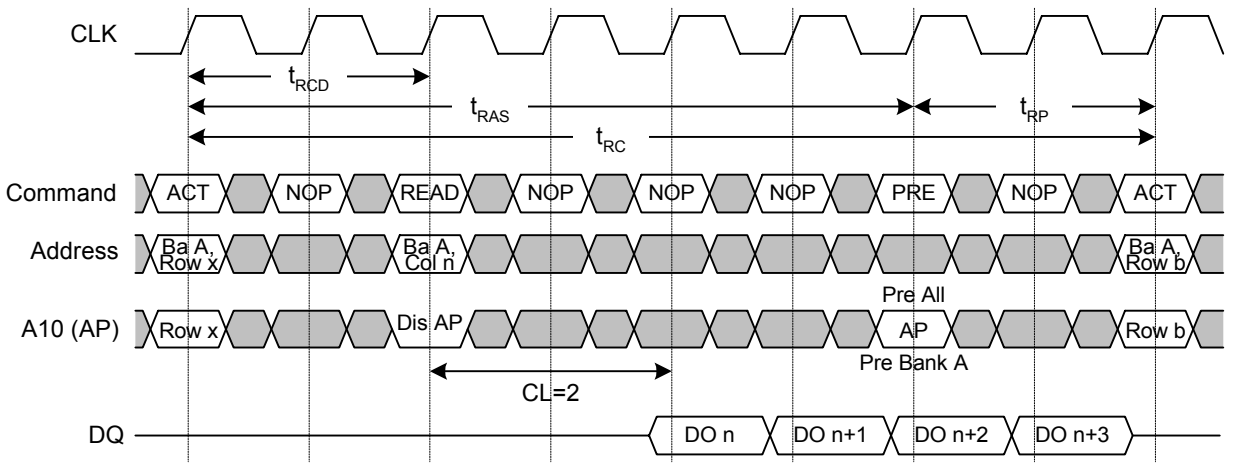


Figure 16 Single READ Burst (CAS Latency = 2)

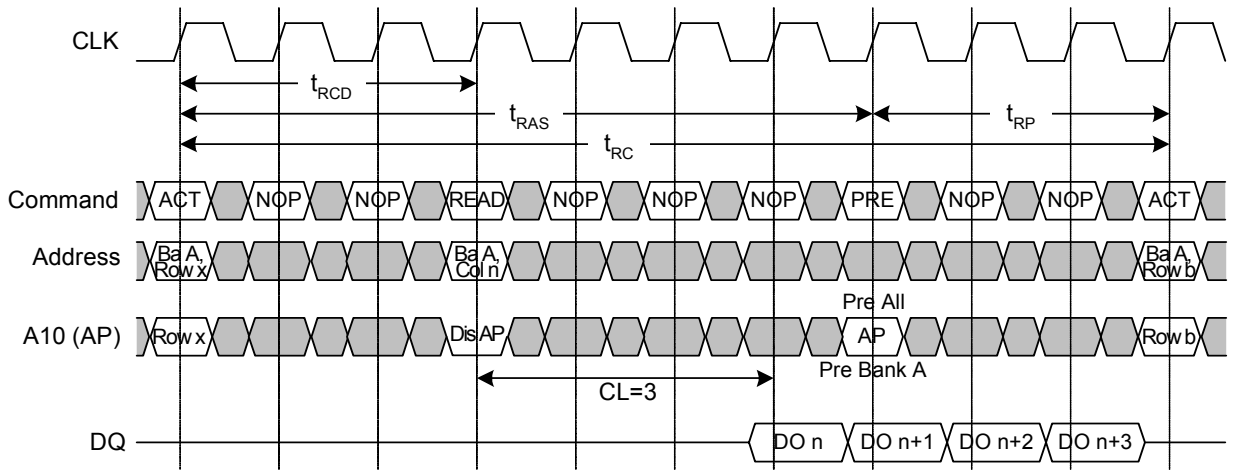


Figure 17 Single READ Burst (CAS Latency = 3)

Data from any READ burst may be concatenated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. A READ command can be initiated on any clock cycle following a previous READ command, and may be performed to the same or a different (active) bank. The first data element from the new burst follows either the last element of a completed burst (**Figure 18**) or the last desired data element of a longer burst which is being truncated (**Figure 19**). The new READ command should be issued x cycles after the first READ command, where x equals the number of desired data elements.

Please note that truncation of a READ burst by a subsequent READ or WRITE is only possible when both commands are issued to the same chip of this stacked configuration.

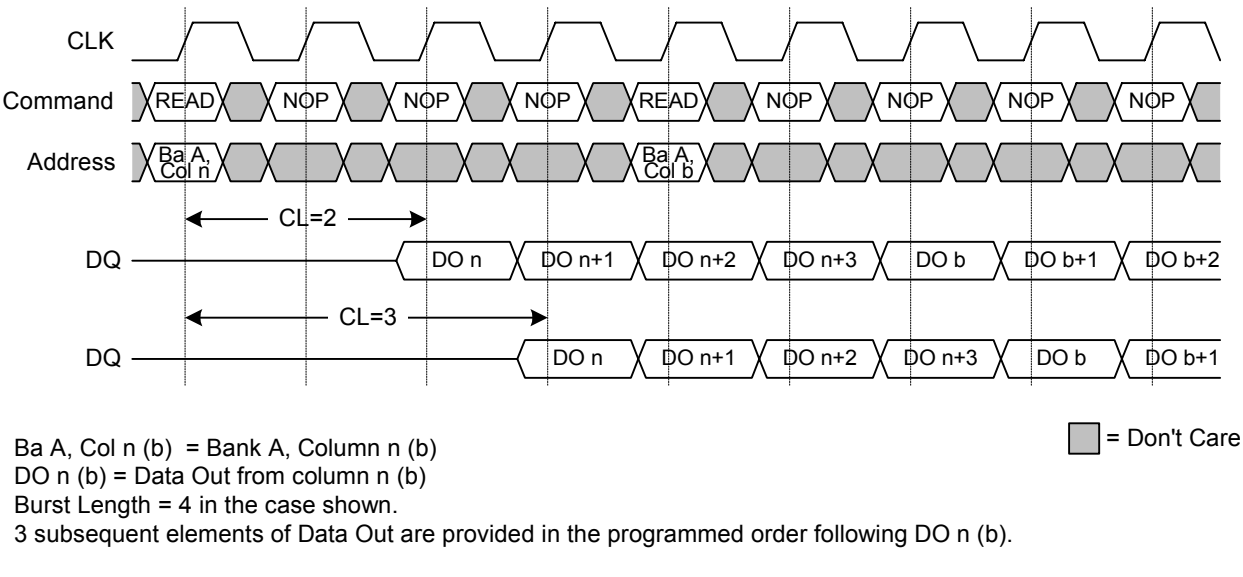
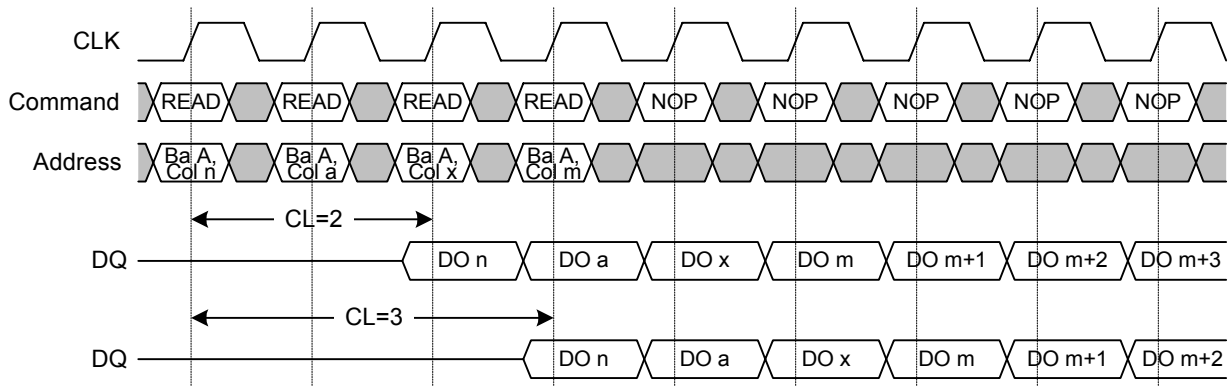


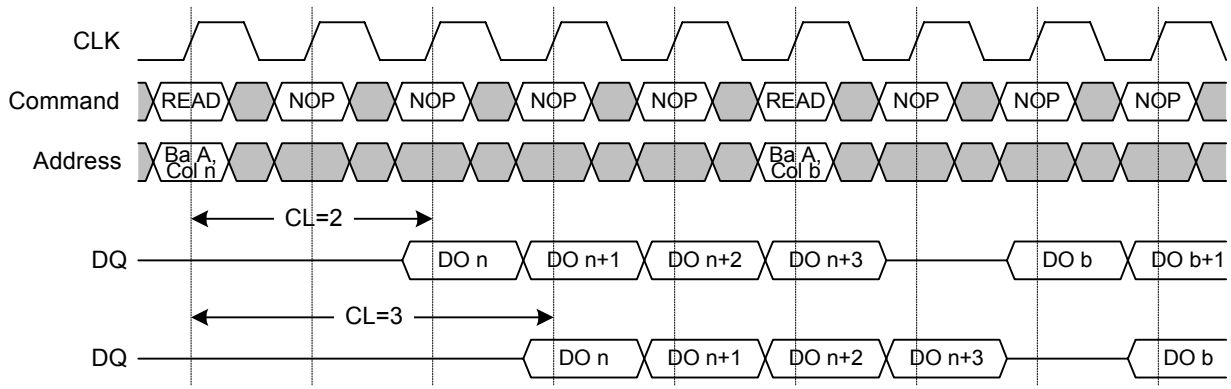
Figure 18 Consecutive READ Bursts



Ba A, Col n etc. = Bank A, Column n etc.
DO n etc. = Data Out from column n etc.
Burst Length = 4 in the case shown; bursts are terminated by consecutive READ commands
3 subsequent elements of Data Out are provided in the programmed order following DO m.

Figure 19 Random READ Bursts

Non-consecutive READ bursts are shown in **Figure 20**.

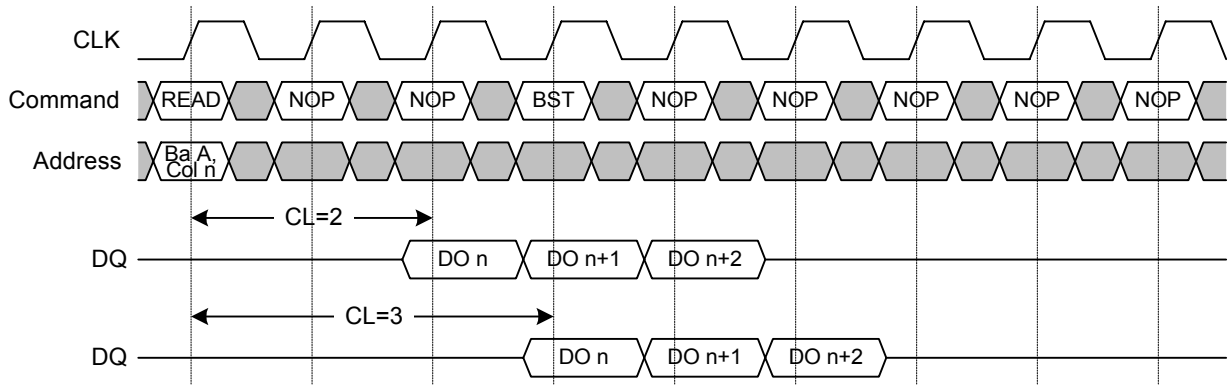


Ba A, Col n (b) = Bank A, Column n (b)
DO n (b) = Data Out from column n (b)
Burst Length = 4 in the case shown.
3 subsequent elements of Data Out are provided in the programmed order following DO n (b).

Figure 20 Non-Consecutive READ Bursts

3.4.5.1 READ Burst Termination

Data from any READ burst may be truncated using the BURST TERMINATE command (see Page 35), provided that Auto Precharge was not activated. The BURST TERMINATE latency is equal to the CAS latency, i.e. the BURST TERMINATE command must be issued x clock cycles before the clock edge at which the last desired data element is valid, where x equals the CAS latency for READ bursts minus 1. This is shown in Figure 21. The BURST TERMINATE command may be used to terminate a full-page READ which does not self-terminate.

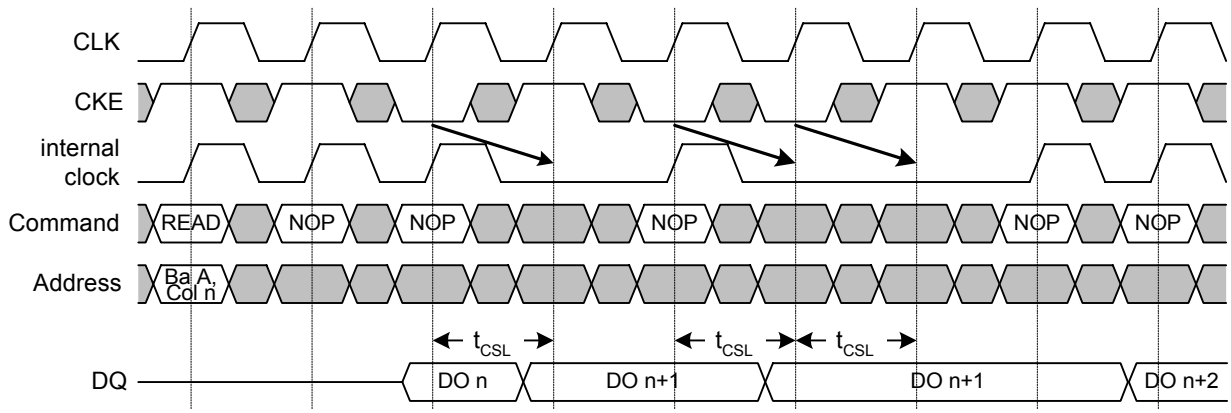


Ba A, Col n = Bank A, Column n
DO n = Data Out from column n
Burst Length = 4 in the case shown.
2 subsequent elements of Data Out are provided in the programmed order following DO n.
The burst is terminated after the 3rd data element.

Figure 21 Terminating a READ Burst

3.4.5.2 Clock Suspend Mode for READ Cycles

Clock suspend mode allows to extend any read burst in progress by a variable number of clock cycles. As long as CKE is registered LOW, the following internal clock pulse(s) will be ignored and data on DQ will remain driven, as shown in Figure 22.



Ba A, Col n etc. = Bank A, Column n etc.
DO n etc. = Data Out from column n etc.
CL = 2 in the case shown
Clock suspend latency t_{CSL} is 1 clock cycle

Figure 22 Clock Suspend Mode for READ Bursts

3.4.5.3 READ - DQM Operation

DQM may be used to suppress read data and place the output buffers into High-Z state. The generic timing parameters as listed in **Table 10** also apply to this DQM operation. The read burst in progress is not affected and will continue as programmed.

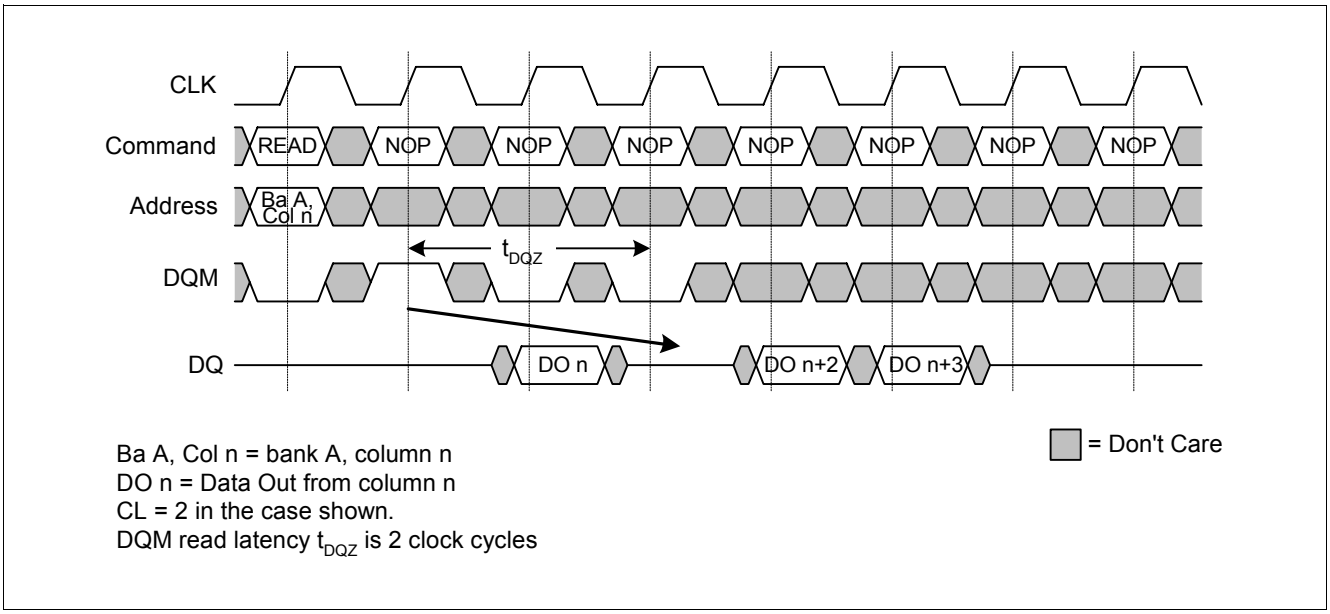
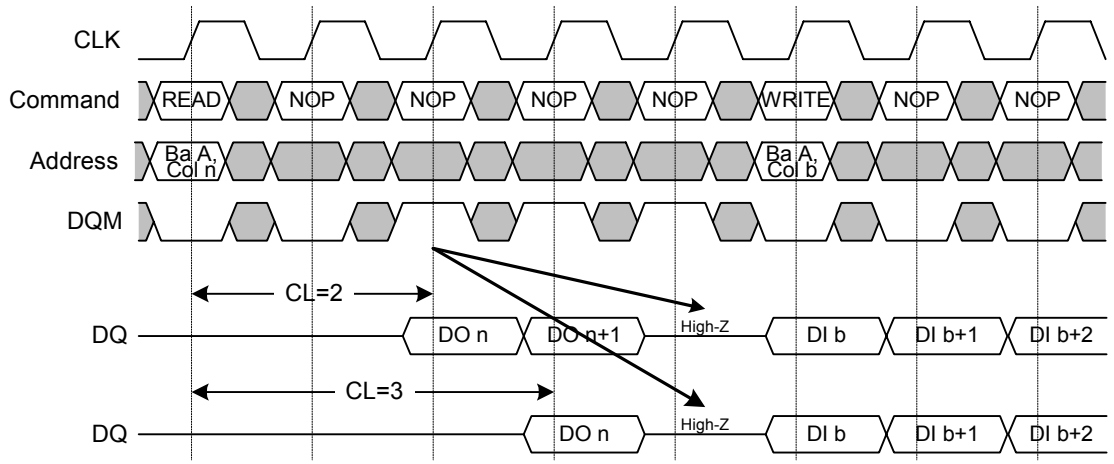


Figure 23 READ Burst - DQM Operation

3.4.5.4 READ to WRITE

A READ burst may be followed by or truncated with a WRITE command. The WRITE command can be performed to the same or a different (active) bank. Care must be taken to avoid bus contention on the DQs; therefore it is recommended that the DQs are held in High-Z state for a minimum of 1 clock cycle. This can be achieved by either delaying the WRITE command, or suppressing the data-out from the READ by pulling DQM HIGH two clock cycles prior to the WRITE command, as shown in **Figure 24**. With the registration of the WRITE command, DQM acts as a write mask: when asserted HIGH, input data will be masked and no write will be performed.

Please note that truncation of a READ burst by a subsequent READ or WRITE is only possible when both commands are issued to the same chip of this stacked configuration.



Ba A, Col n (b) = bank A, column n (b)
DO n = Data Out from column n; DI b = Data In to column b;
DQM is asserted HIGH to set DQs to High-Z state for 1 clock cycle prior to the WRITE command.

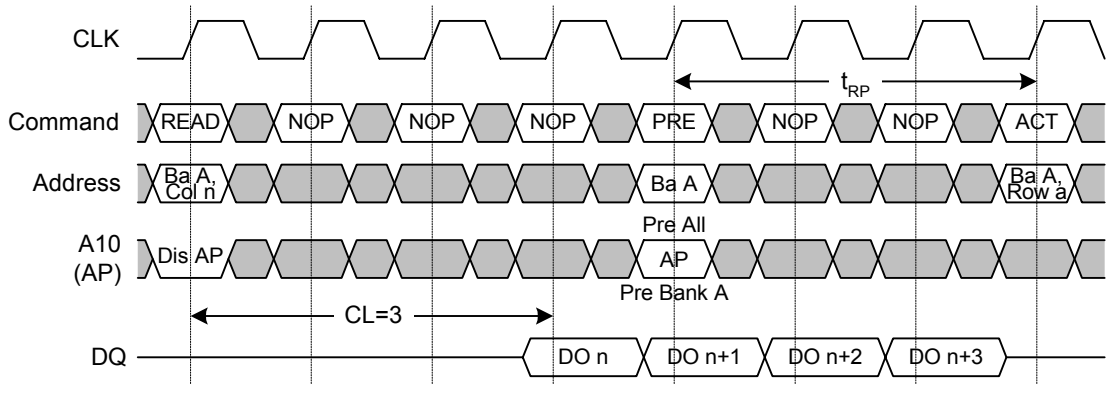
Figure 24 READ to WRITE Timing

3.4.5.5 READ to PRECHARGE

A READ burst may be followed by, or truncated with a PRECHARGE command to the same bank (provided that Auto Precharge was not activated), as shown in **Figure 25**.

The PRECHARGE command should be issued x clock cycles before the clock edge at which the last desired data element is valid, where x equals the CAS latency for READ bursts minus 1. Following the PRECHARGE command, a subsequent ACTIVE command to the same bank cannot be issued until t_{RP} is met. Please note that part of the row precharge time is hidden during the access of the last data elements.

In the case of a READ being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same READ burst with Auto Precharge enabled. The disadvantage of the PRECHARGE command is that it requires that the command and address busses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate bursts.



Ba A, Col n = bank A, column n; BA Am Row = bank A, row x
DO n = Data Out from column n
Burst Length = 4 in the case shown.
CAS latency = 3 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n.

Figure 25 READ to PRECHARGE Timing

3.4.6 WRITE

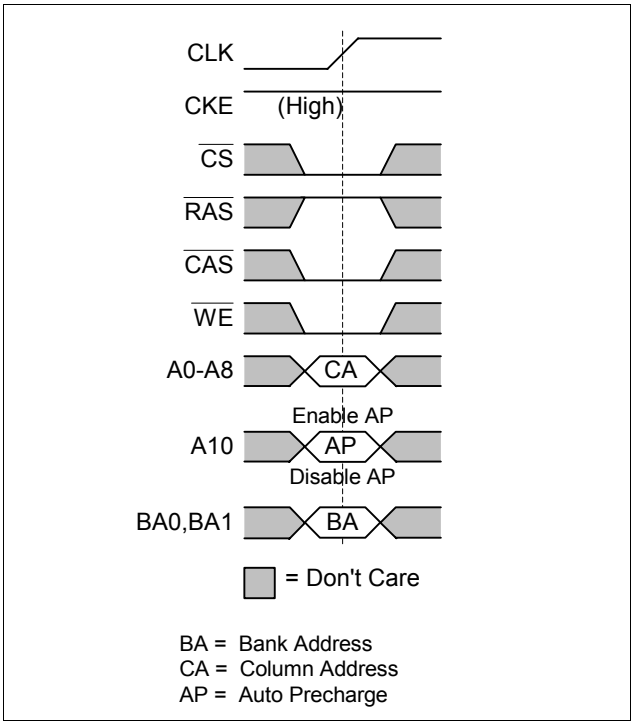


Figure 26 WRITE Command

WRITE bursts are initiated with a WRITE command, as shown in **Figure 26**. Basic timings for the DQs are shown in **Figure 27**; they apply to all write operations.

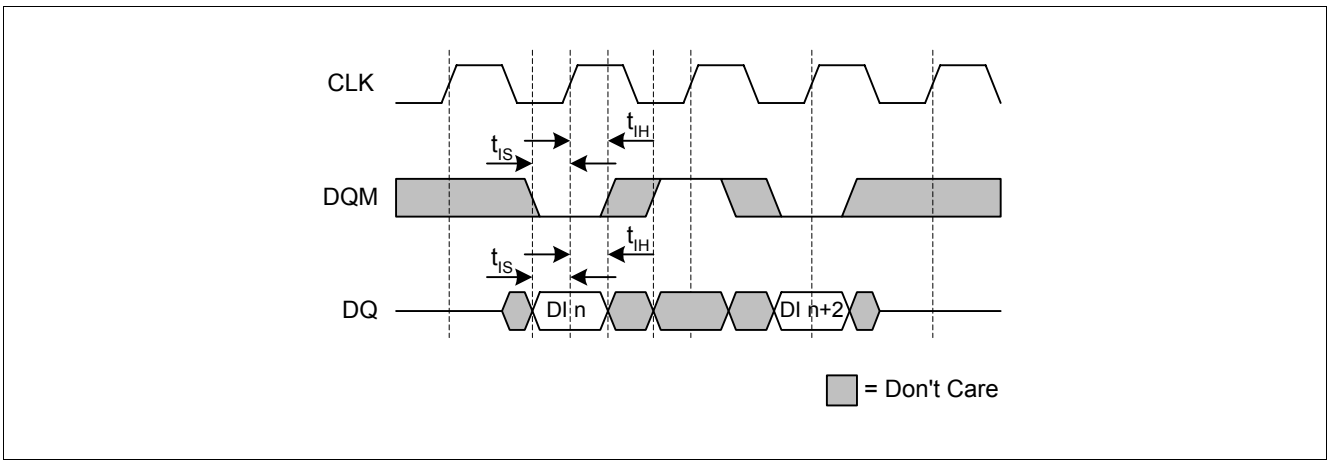


Figure 27 Basic WRITE Timing Parameters for DQs

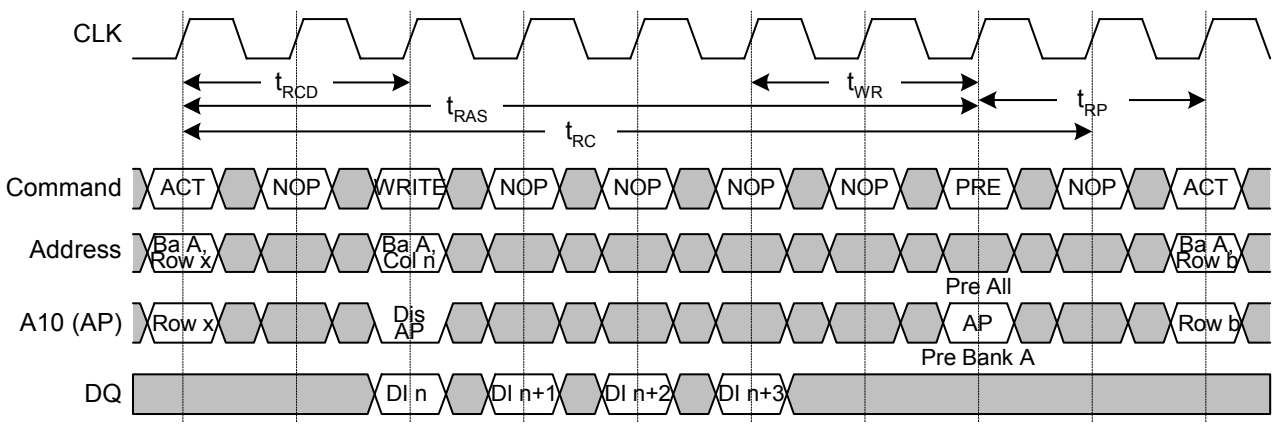
The starting column and bank addresses are provided with the WRITE command, and Auto Precharge is either enabled or disabled for that access. If Auto Precharge is enabled, the row being accessed is precharged at the completion of the write burst. For the generic WRITE commands used in the following illustrations, Auto Precharge is disabled.

During WRITE bursts, the first valid data-in element is registered coincident with the WRITE command, and subsequent data elements are registered on each successive positive edge of CLK. Upon completion of a burst, assuming no other commands have been initiated, the DQs remain in High-Z state, and any additional input data is ignored. **Figure 28** and **Figure 29** show a single WRITE burst for each supported CAS latency setting.

Table 11 Timing Parameters for WRITE

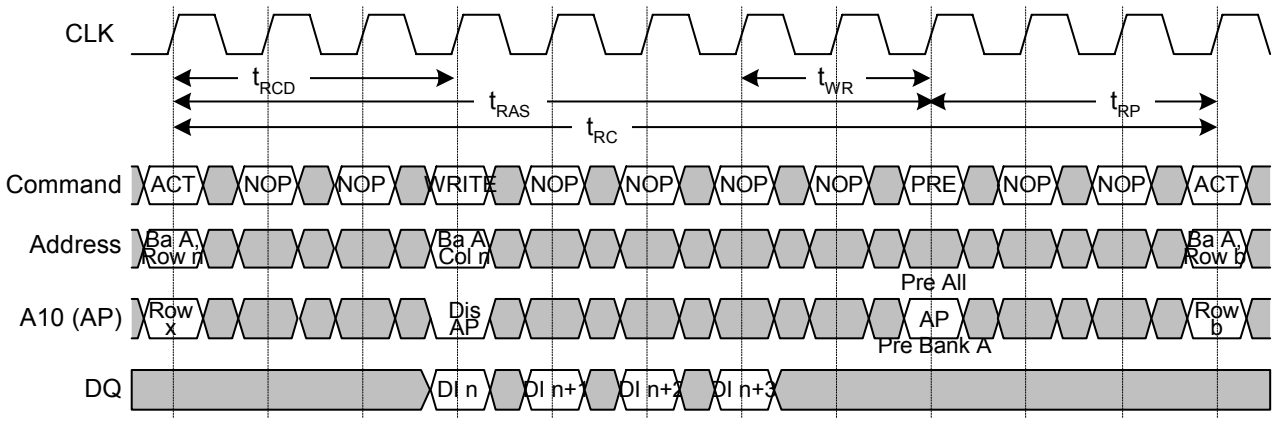
Parameter	Symbol	–7.5		Unit	Notes
		min.	max.		
DQ and DQM input setup time	t_{IS}	1.5	—	ns	—
DQ and DQM input hold time	t_{IH}	0.8	—	ns	—
DQM write mask latency	t_{DQW}	0	—	t_{CK}	—
ACTIVE to ACTIVE command period	t_{RC}	67	—	ns	1)
ACTIVE to READ or WRITE delay	t_{RCD}	19	—	ns	1)
ACTIVE to PRECHARGE command period	t_{RAS}	45	100k	ns	1)
WRITE recovery time	t_{WR}	14	—	ns	1)
PRECHARGE command period	t_{RP}	19	—	ns	1)

1) These parameters account for the number of clock cycles and depend on the operating frequency as follows: no. of clock cycles = specified delay / clock period; round up to next integer.



Ba A, Col n = bank A, column n
DI n = Data In to column n
Burst Length = 4 in the case shown.
3 subsequent elements of Data In are provided in the programmed order following DI n.

Figure 28 WRITE Burst (CAS Latency = 2)

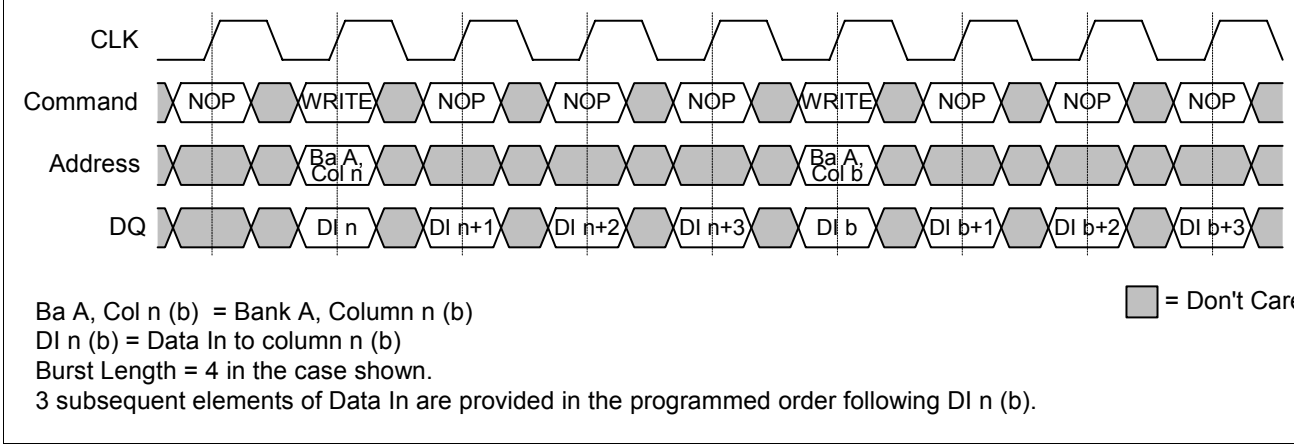


Ba A, Col n = bank A, column n
DI n = Data In to column n
Burst Length = 4 in the case shown.
3 subsequent elements of Data In are provided in the programmed order following DI n.

Figure 29 WRITE Burst (CAS Latency = 3)

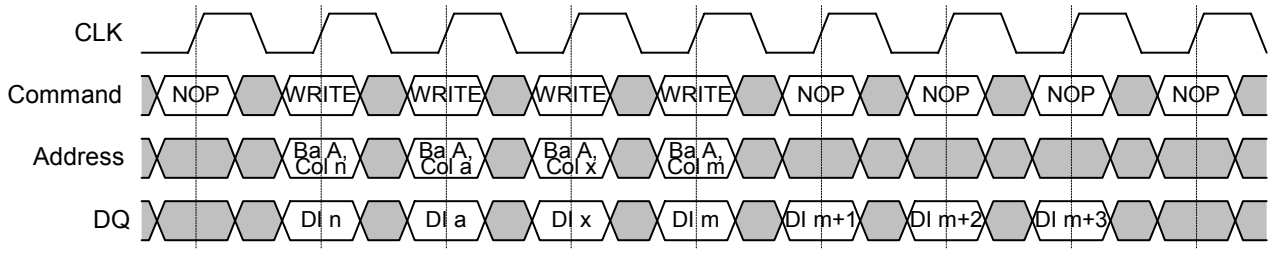
Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data can be maintained. A WRITE command can be issued on any positive edge of clock following the previous WRITE command. The first data element from the new burst is applied after either the last element of a completed burst (**Figure 30**) or the last desired data element of a longer burst which is being truncated (**Figure 31**). The new WRITE command should be issued x cycles after the first WRITE command, where x equals the number of desired data elements.

Please note that truncation of a WRITE burst by a subsequent READ or WRITE is only possible when both commands are issued to the same chip of this stacked configuration.



Ba A, Col n (b) = Bank A, Column n (b)
DI n (b) = Data In to column n (b)
Burst Length = 4 in the case shown.
3 subsequent elements of Data In are provided in the programmed order following DI n (b).

Figure 30 Consecutive WRITE Bursts

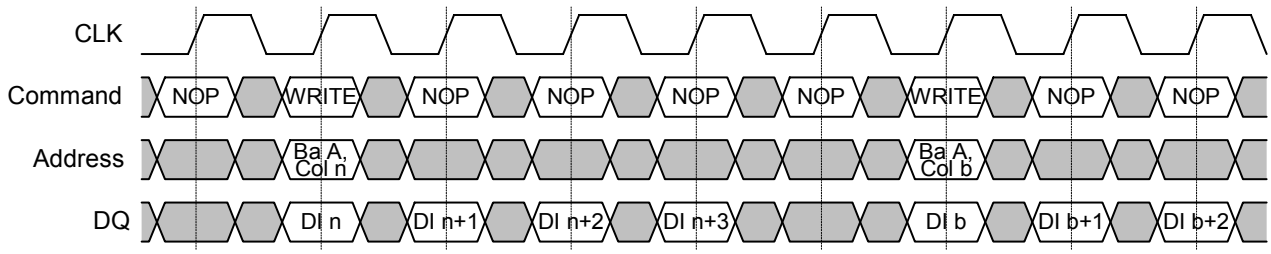


Ba A, Col n etc. = Bank A, Column n etc.
DI n etc. = Data In to column n etc.
Burst Length = 4 in the case shown; bursts are terminated by consecutive WRITE commands.
3 subsequent elements of Data In are provided in the programmed order following DI m .

= Don't Care

Figure 31 Random WRITE Bursts

Non-consecutive WRITE bursts are shown in **Figure 32**



Ba A, Col n (b) = Bank A, Column n (b)
DI n (b) = Data In to column n (b)
Burst Length = 4 in the case shown.
3 subsequent elements of Data In are provided in the programmed order following DI n (b).

= Don't Care

Figure 32 Non-Consecutive WRITE Bursts

3.4.6.1 WRITE Burst Termination

Data from any WRITE burst may be truncated using the BURST TERMINATE command (see **Page 35**), provided that Auto Precharge was not activated. The input data provided coincident with the BURST TERMINATE command will be ignored. This is shown in **Figure 33**. The BURST TERMINATE command may be used to terminate a full-page WRITE which does not self-terminate.

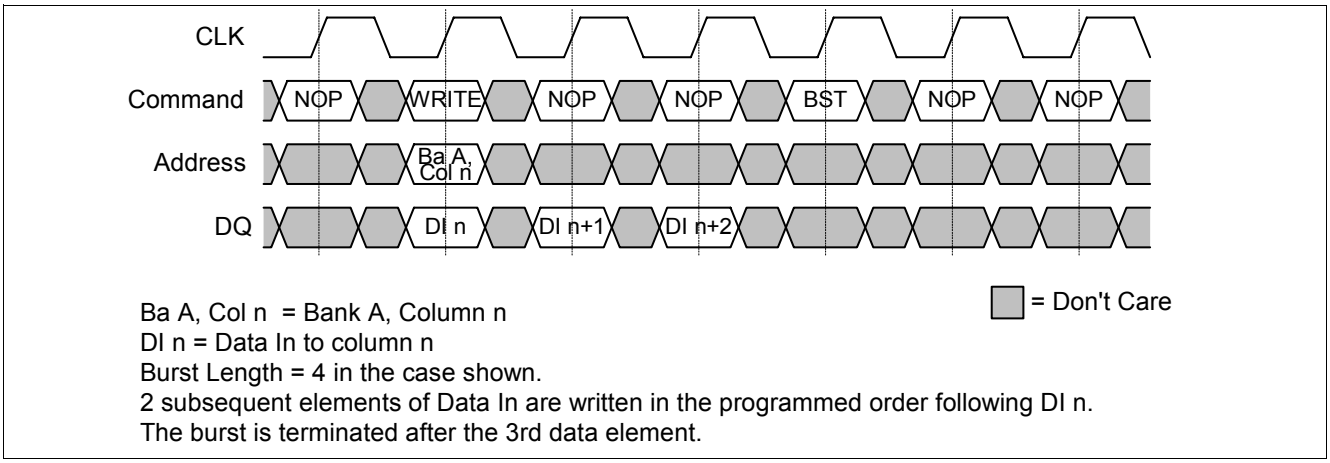


Figure 33 Terminating a WRITE Burs

3.4.6.2 Clock Suspend Mode for WRITE Cycles

Clock suspend mode allows to extend any WRITE burst in progress by a variable number of clock cycles. As long as CKE is registered LOW, the following internal clock pulse(s) will be ignored and no data will be captured, as shown in **Figure 34**.

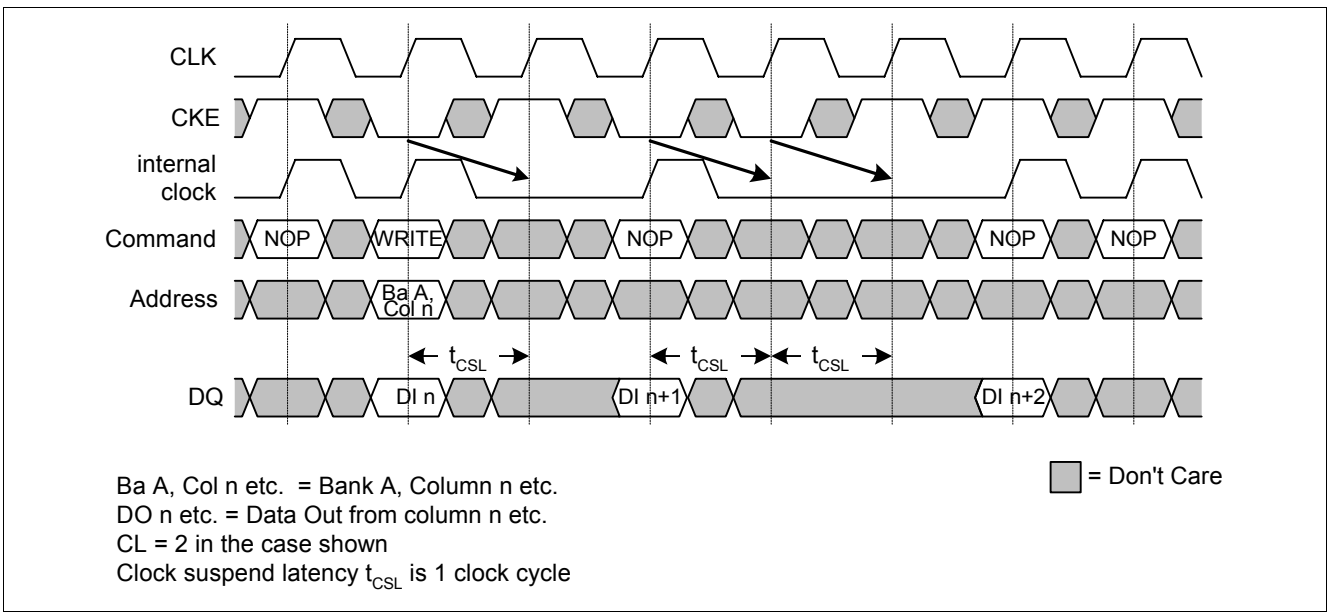
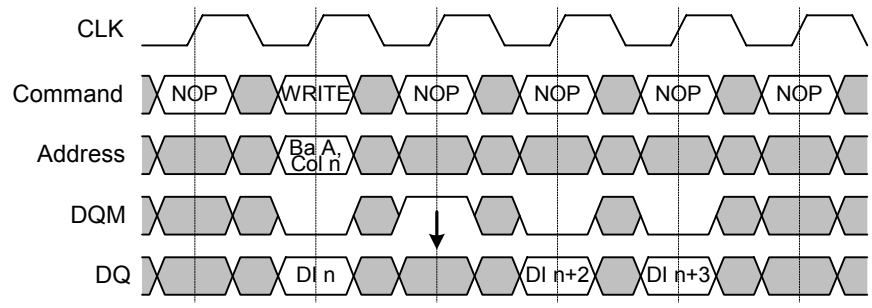


Figure 34 Clock Suspend Mode for WRITE Bursts

3.4.6.3 WRITE - DQM Operation

DQM may be used to mask write data: when asserted HIGH, input data will be masked and no write will be performed. The generic timing parameters as listed in **Table 11** also apply to this DQM operation. The write burst in progress is not affected and will continue as programmed.



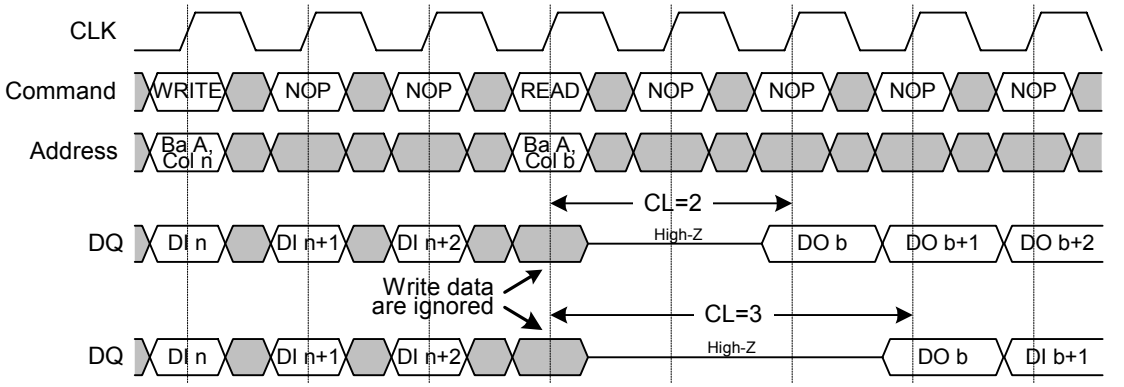
Ba A, Col n = Bank A, Column n
DI n = Data In to column n
Burst Length = 4 in the case shown.
3 subsequent elements of Data In are provided in the programmed order following DI n, with the first element (DI n+1) being masked.
DQM write latency is 0 clock cycles.

Figure 35 WRITE Burst - DQM Operation

3.4.6.4 WRITE to READ

A WRITE burst may be followed by, or truncated with a READ command. The READ command can be performed to the same or a different (active) bank. With the registration of the READ command, data inputs will be ignored and no WRITE will be performed, as shown in **Figure 36**.

Please note that truncation of a WRITE burst by a subsequent READ or WRITE is only possible when both commands are issued to the same chip of this stacked configuration.



Ba A, Col n (b) = bank A, column n (b)
DI n = Data In to column n; DO b = Data Out from column b;
Burst Length = 4 in the case shown.
3 subsequent elements of Data In (Out) are provided in the programmed order following DI n (DO b).
DI n+3 is ignored due to READ command. No DQM masking required at this point.

Figure 36 WRITE to READ Timing

WRITE to PRECHARGE

A WRITE burst may be followed by, or truncated with a PRECHARGE command to the same bank (provided that Auto Precharge was not activated), as shown in **Figure 37**.

The PRECHARGE command should be issued t_{WR} after the clock edge at which the last desired data element of the WRITE burst was registered. Additionally, when truncating a WRITE burst, DQM must be pulled to mask input data presented during t_{WR} prior to the PRECHARGE command. Following the PRE-CHARGE command, a subsequent ACTIVE command to the same bank cannot be issued until t_{RP} is met.

In the case of a WRITE being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same WRITE burst with Auto Precharge enabled. The disadvantage of the PRECHARGE command is that it requires that the command and address busses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate bursts.

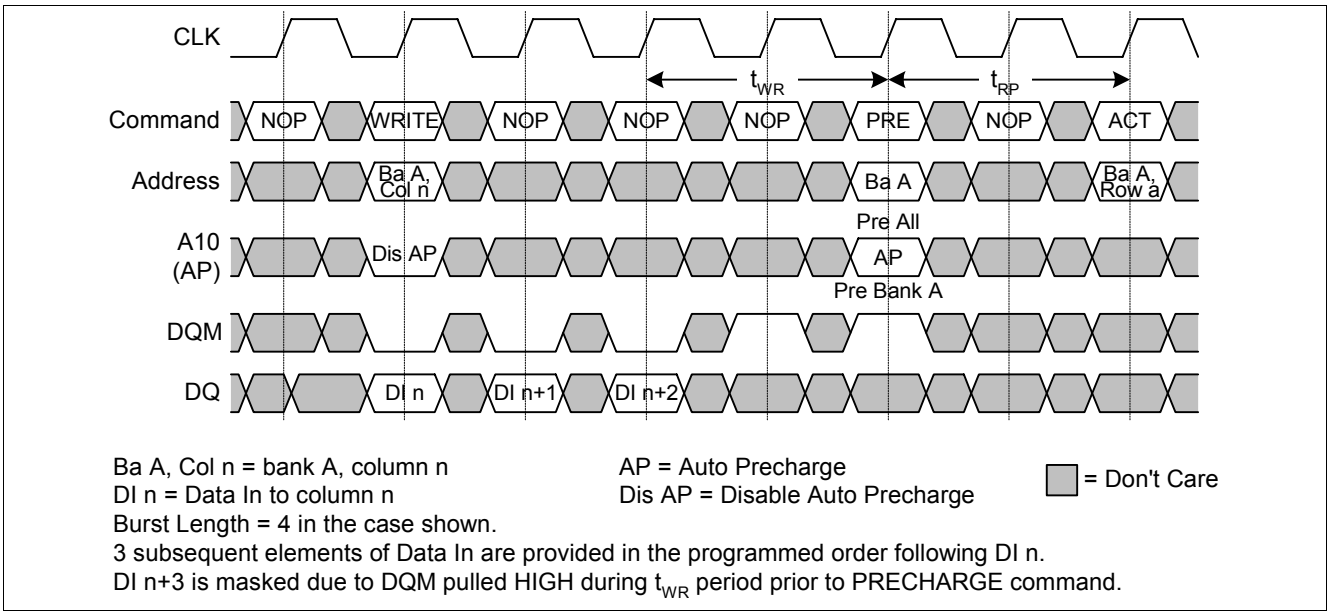


Figure 37 WRITE to PRECHARGE Timing

3.4.7 BURST TERMINATE

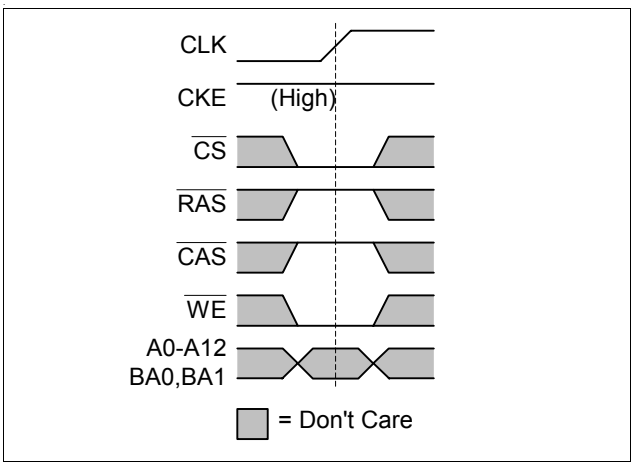


Figure 38 BURST TERMINATE Command

The BURST TERMINATE command is used to truncate READ or WRITE bursts (with Auto Precharge disabled). The most recently registered READ or WRITE command prior to the BURST TERMINATE command will be truncated, as shown in **Figure 21** and **Figure 33**, respectively

3.4.8 PRECHARGE

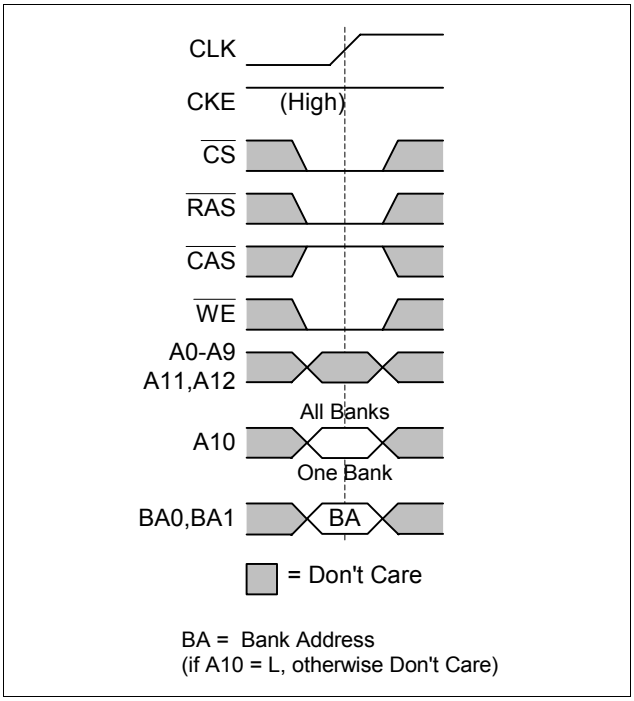


Figure 39 PRECHARGE Command

The PRECHARGE command is used to deactivate (close) the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (t_{RP}) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as “Don’t Care.”

Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

3.4.8.1 AUTO PRECHARGE

Auto Precharge is a feature which performs the same individual-bank precharge functions described above, but without requiring an explicit command. This is accomplished by using A10 to enable Auto Precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto Precharge is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command. Auto Precharge ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge (t_{RP}) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type.

Table 12 Timing Parameters for PRECHARGE

Parameter	Symbol	– 7.5		Units	Notes
		min.	max.		
ACTIVE to PRECHARGE command period	t_{RAS}	45	100k	ns	1)
WRITE recovery time	t_{WR}	14	—	ns	1)
PRECHARGE command period	t_{RP}	19	—	ns	1)

1) These parameters account for the number of clock cycles and depend on the operating frequency as follows: no. of clock cycles = specified delay / clock period; round up to next integer.

3.4.8.2 CONCURRENT AUTO PRECHARGE

A READ or WRITE burst with Auto Precharge enabled can be interrupted by a subsequent READ or WRITE command issued to a different bank.

Figure 40 shows a READ with Auto Precharge to bank n, interrupted by a READ (with or without Auto Precharge) to bank m. The READ to bank m will interrupt the READ to bank n, CAS latency later. The precharge to bank n will begin when the READ to bank m is registered.

Figure 41 shows a READ with Auto Precharge to bank n, interrupted by a WRITE (with or without Auto Precharge) to bank m. The precharge to bank n will begin when the WRITE to bank m is registered. DQM should be pulled HIGH two clock cycles prior to the WRITE to prevent bus contention.

Figure 42 shows a WRITE with Auto Precharge to bank n, interrupted by a READ (with or without Auto Precharge) to bank m. The precharge to bank n will begin t_{WR} after the new command to bank m is registered. The last valid data-in to bank n is one clock cycle prior to the READ to bank m.

Figure 43 shows a WRITE with Auto Precharge to bank n, interrupted by a WRITE (with or without Auto Precharge) to bank m. The precharge to bank n will begin t_{WR} after the WRITE to bank m is registered. The last valid data-in to bank n is one clock cycle prior to the WRITE to bank m.

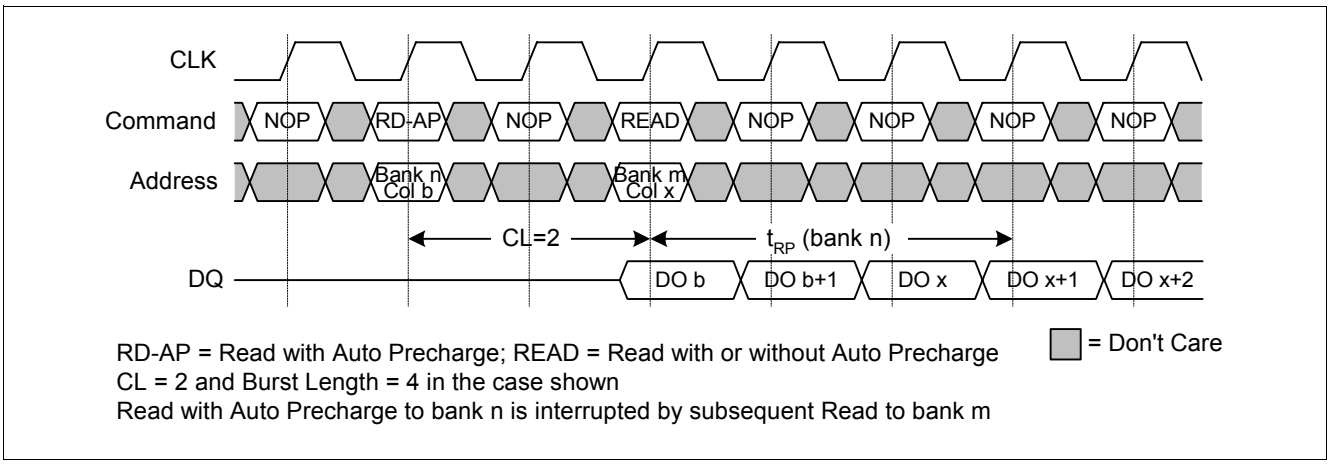


Figure 40 READ with Auto Precharge Interrupted by READ

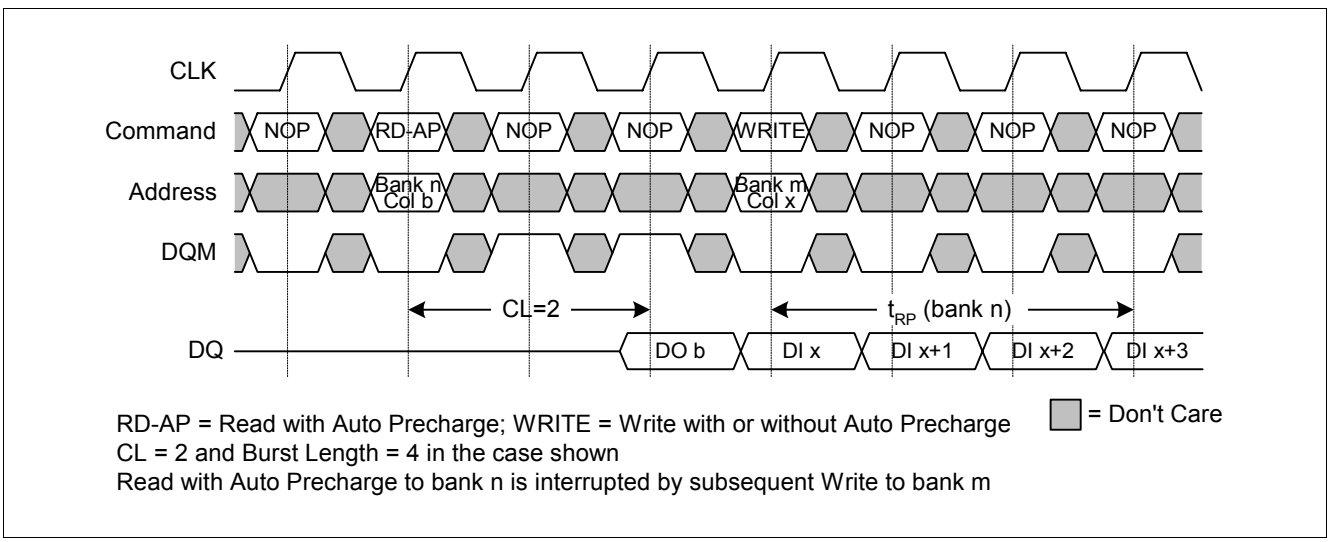


Figure 41 READ with Auto Precharge Interrupted by WRITE

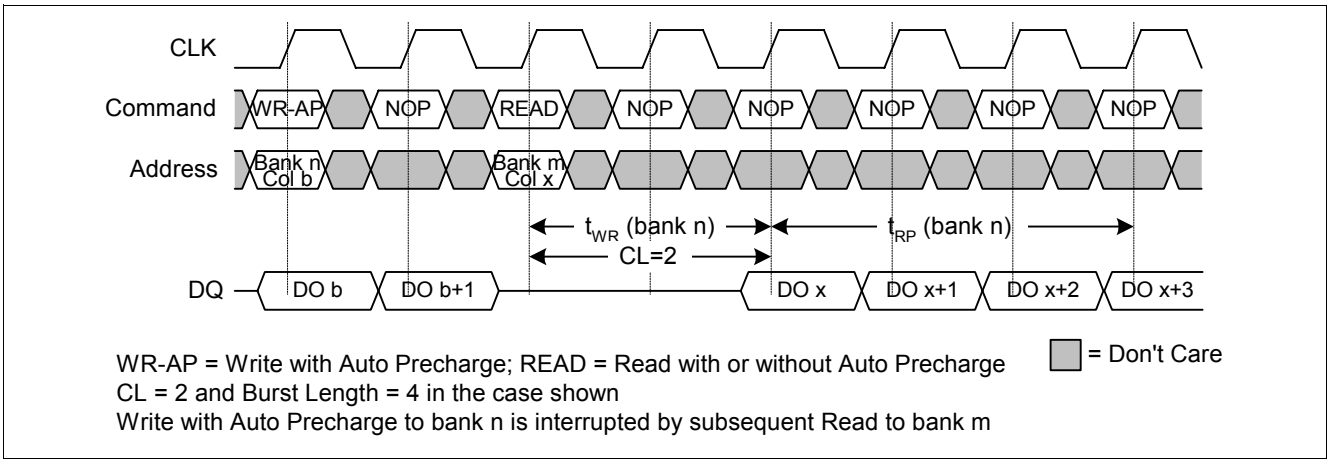


Figure 42 WRITE with Auto Precharge Interrupted by READ

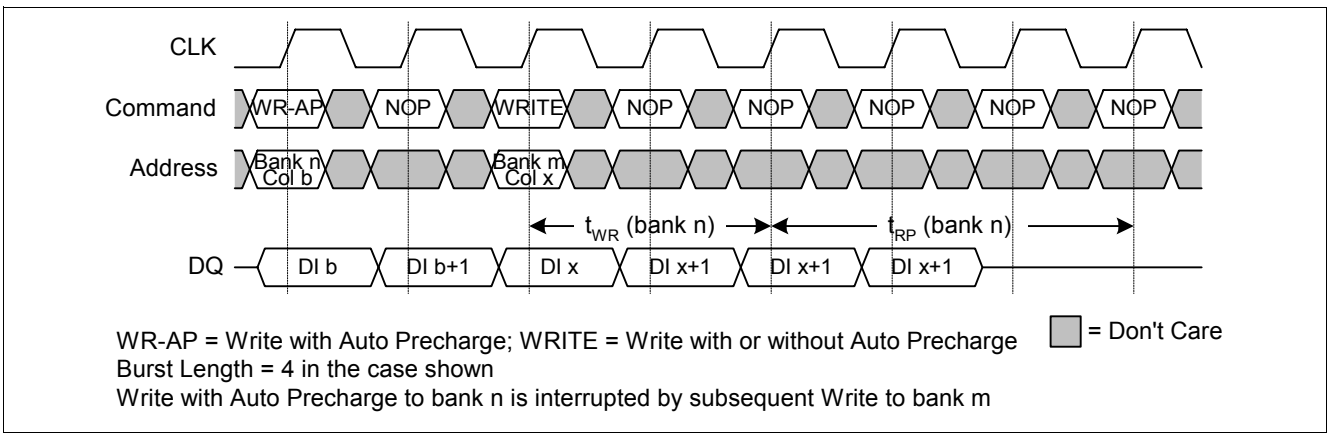


Figure 43 WRITE with Auto Precharge Interrupted by WRITE

3.4.9 AUTO REFRESH and SELF REFRESH

The Mobile-RAM requires a refresh of all rows in a rolling interval. Each refresh is generated in one of two ways: by an explicit AUTO REFRESH command, or by an internally timed event in SELF REFRESH mode.

3.4.9.1 AUTO REFRESH

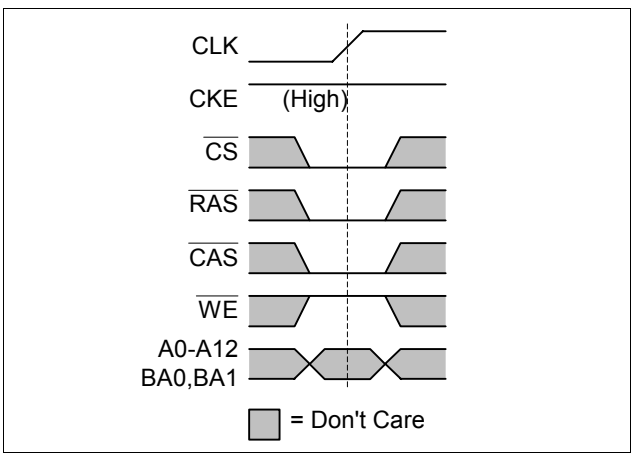


Figure 44 AUTO REFRESH Command

Auto Refresh is used during normal operation of the Mobile-RAM. The command is nonpersistent, so it must be issued each time a refresh is required. A minimum row cycle time (t_{RC}) is required between two AUTO REFRESH commands. The same rule applies to any access command after the auto refresh operation. All banks must be precharged prior to the AUTO REFRESH command.

The refresh addressing is generated by the internal refresh controller. This makes the address bits “Don’t Care” during an AUTO REFRESH command. The Mobile-RAM requires AUTO REFRESH cycles at an average periodic interval of 7.8 µs (max.). Partial array mode has no influence on auto refresh mode.

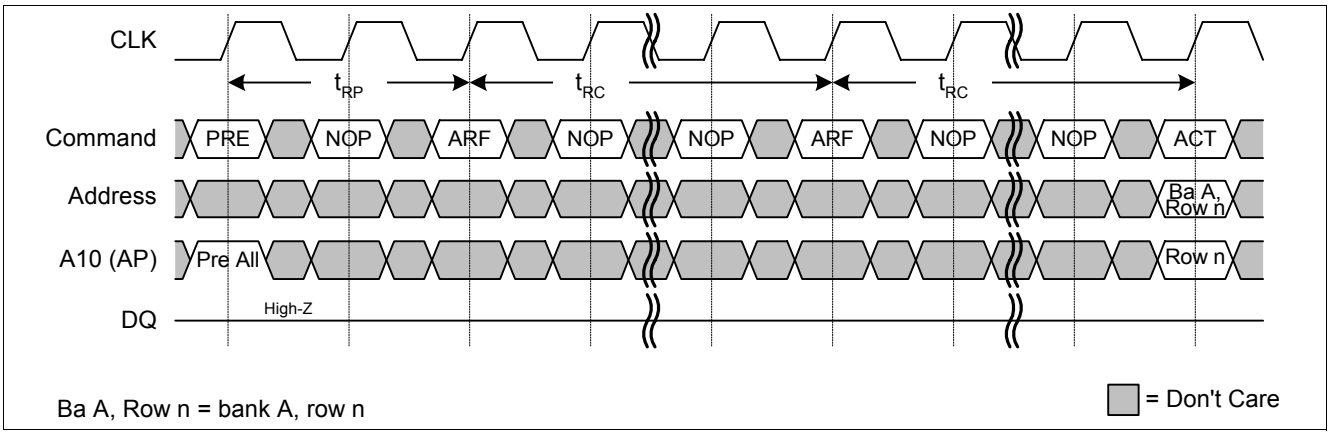


Figure 45 AUTO REFRESH

3.4.9.2 SELF REFRESH

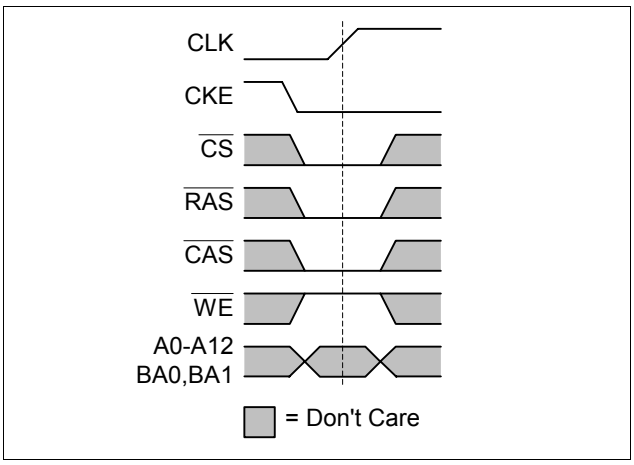


Figure 46 SELF REFRESH Entry Command

The SELF REFRESH command can be used to retain data in the Mobile-RAM, even if the rest of the system is powered down. When in the SELF REFRESH mode, the Mobile-RAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is LOW. Input signals except CKE and CLK are “Don’t Care” during SELF REFRESH. CLK pin may not float.

The SELF REFRESH command may be issued to both chips at the same time ($\overline{CS0}$ = $\overline{CS1}$ = 0).

The procedure for exiting SELF REFRESH requires a stable clock prior to CKE returning HIGH. Once CKE is HIGH, NOP commands must be issued for t_{RC} because time is required for a completion of any internal refresh in progress.

The use of SELF REFRESH mode introduces the possibility that an internally timed event can be missed when CKE is raised for exit from SELF REFRESH mode. Upon exit from SELF REFRESH an extra AUTO REFRESH command is recommended.

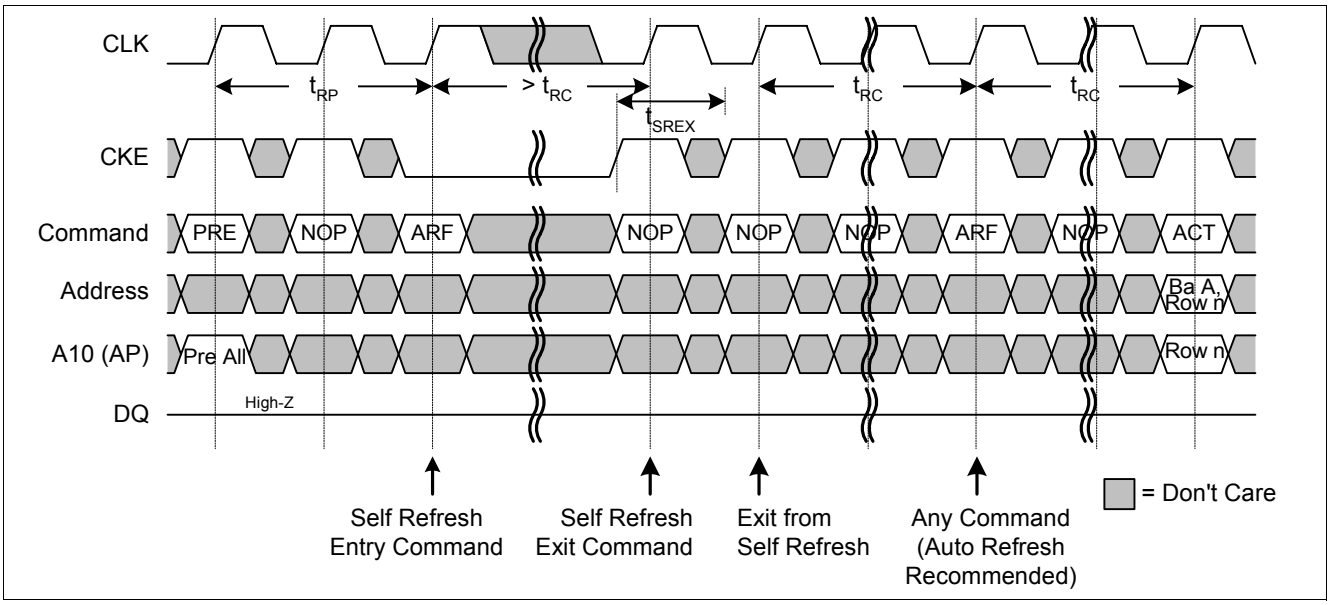


Figure 47 SELF REFRESH Entry and Exit

Table 13 Timing Parameters for AUTO REFRESH and SELF REFRESH

Parameter	Symbol	– 7.5		Units	Notes
		min.	max.		
ACTIVE to ACTIVE command period	t_{RC}	67	—	ns	1)
PRECHARGE command period	t_{RP}	19	—	ns	1)
Refresh period (8192 rows)	t_{REF}	—	64	ms	1)
Self refresh exit time	t_{SREX}	1	—	t_{CK}	1)

1) These parameters account for the number of clock cycles and depend on the operating frequency as follows: no. of clock cycles = specified delay / clock period; round up to next integer.

3.4.10 POWER DOWN

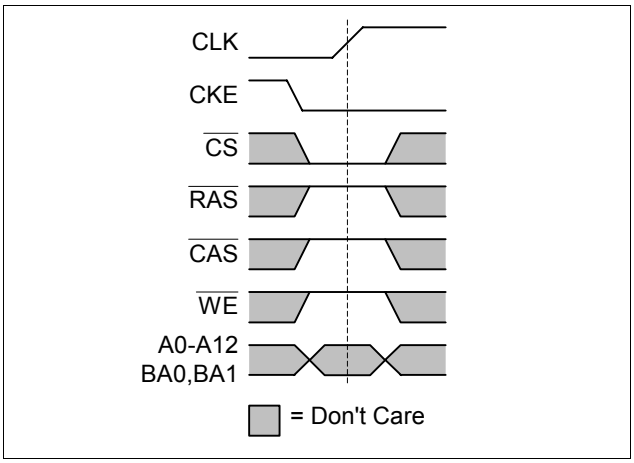


Figure 48 POWER DOWN Entry Command

Power-down is entered when CKE is registered LOW (no accesses can be in progress). If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CKE and CLK. In power-down mode, CKE LOW must be maintained, and all other input signals are “Don’t Care”. However, power-down duration is limited by the refresh requirements of the device (t_{REF}).

The power-down state is synchronously exited when CKE is registered HIGH (along with a NOP or DESELECT command). One clock delay is required for power down entry and exit.

Power-down entry and exit is common to both stacked chips as they share a common CKE signal.

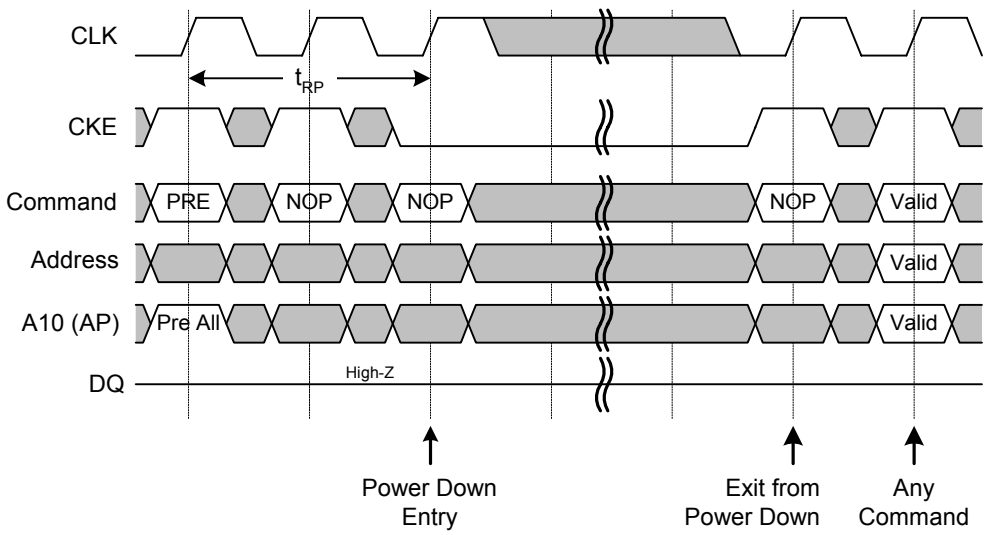


Figure 49 POWER DOWN Entry and Exit

3.4.10.1 DEEP POWER DOWN

The deep power down mode is an unique function on Low Power SDRAM devices with extremly low current consumption. Deep power down mode is entered using the BURST TERMINATE command (cf. **Figure 38**) except that CKE is LOW. All internal voltage generators inside the device are stopped and all memory data is lost in this mode. To enter the deep power down mode all banks must be precharged.

The deep power down mode is asynchronously exited by asserting CKE HIGH. After the exit, the same command sequence as for power-up initialization has to be applied before any other command may be issued (cf. **Figure 4** and **Figure 7**).

3.5 Function Truth Tables

Table 14 Current State Bank n - Command to Bank n

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command / Action	Notes
Any	H	X	X	X	DESELECT (NOP / continue previous operation)	1)2)3)4)5)6)
	L	H	H	H	NO OPERATION (NOP / continue previous operation)	1) to 6)
Idle	L	L	H	H	ACTIVE (select and activate row)	1) to 6)
	L	L	L	H	AUTO REFRESH	1) to 7)
	L	L	L	L	MODE REGISTER SET	1) to 7)
	L	L	H	L	PRECHARGE	1) to 6), 8)
Row Active	L	H	L	H	READ (select column and start READ burst)	1) to 6), 9)
	L	H	L	L	WRITE (select column and start WRITE burst)	1) to 6), 9)
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	1) to 6), 10)
Read (Auto-Precharge Disabled)	L	H	L	H	READ (select column and start new READ burst)	1) to 6), 9)
	L	H	L	L	WRITE (select column and start new WRITE burst)	1) to 6), 9)
	L	L	H	L	PRECHARGE (truncate READ burst, start precharge)	1) to 6), 10)
	L	H	H	L	BURST TERMINATE	1) to 6), 11)
Write (Auto-Precharge Disabled)	L	H	L	H	READ (select column and start READ burst)	1) to 6), 9)
	L	H	L	L	WRITE (select column and start WRITE burst)	1) to 6), 9)
	L	L	H	L	PRECHARGE (truncate WRITE burst, start precharge)	1) to 6), 10)
	L	H	H	L	BURST TERMINATE	1) to 6), 11)

1) This table applies when CKEn-1 was HIGH and CKEn is HIGH and after t_{RC} has been met (if the previous state was self refresh).

2) This table is bank-specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.

3) Current state definitions:
   - Idle: The bank has been precharged, and t_{RP} has been met.
   - Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
   - Read: A READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   - Write: A WRITE burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

4) The following states must not be interrupted by a command issued to the same bank. DESELECT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and according to **Table 15**.
   - Precharging: Starts with registration of a PRECHARGE command and ends when t_{RP} is met. Once t_{RP} is met, the bank is in the “idle” state.
   - Row Activating: Starts with registration of an ACTIVE command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank is in the “row active” state.
   - Read with AP Enabled: Starts with registration of a READ command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.
   - Write with AP Enabled: Starts with registration of a WRITE command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.

5) The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.
   Refreshing: Starts with registration of an AUTO REFRESH command and ends when t_{RC} is met. Once t_{RC} is met, the SDRAM is in the “all banks idle” state.
   Accessing Mode Register: Starts with registration of a MODE REGISTER SET command and ends when t_{MRD} has been met. Once t_{MRD} is met, the SDRAM is in the “all banks idle” state.
   Precharging All: Starts with registration of a PRECHARGE ALL command and ends when t_{RP} is met. Once t_{RP} is met, all banks are in the idle state.
6) All states and sequences not shown are illegal or reserved.
7) Not bank-specific; requires that all banks are idle and no bursts are in progress.
8) Same as NOP command in that state.
9) READs or WRITEs listed in the Command/Action column include READs or WRITEs with Auto Precharge enabled and READs or WRITEs with Auto Precharge disabled.
10) May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
11) Not bank-specific; BURST TERMINATE affects the most recent READ or WRITE burst, regardless of bank.

Table 15 Current State Bank n - Command to Bank m (different bank)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command / Action	Notes
Any	H	X	X	X	DESELECT (NOP / continue previous operation)	1)2)3)4)5)6)
	L	H	H	H	NO OPERATION (NOP / continue previous operation)	1) to 6)
Idle	X	X	X	X	Any command otherwise allowed to bank n	1) to 6)
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	1) to 6)
	L	H	L	H	READ (select column and start READ burst)	1) to 7)
	L	H	L	L	WRITE (select column and start WRITE burst)	1) to 7)
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	1) to 6)
Read (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	1) to 6)
	L	H	L	H	READ (select column and start READ burst)	1) to 7)
	L	H	L	L	WRITE (select column and start WRITE burst)	1) to 8)
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	1) to 6)
Write (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	1) to 6)
	L	H	L	H	READ (select column and start READ burst)	1) to 7)
	L	H	L	L	WRITE (select column and start WRITE burst)	1) to 7)
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	1) to 6)
Read (with Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	1) to 6)
	L	H	L	H	READ (select column and start READ burst)	1) to 7), 9)
	L	H	L	L	WRITE (select column and start WRITE burst)	1) to 9)
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	1) to 6)
Write (with Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	1) to 6)
	L	H	L	H	READ (select column and start READ burst)	1) to 7), 9)
	L	H	L	L	WRITE (select column and start WRITE burst)	1) to 7), 9)
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	1) to 6)

1) This table applies when CKEn-1 was HIGH and CKEn is HIGH and after t_{RC} has been met (if the previous state was Self Refresh).
2) This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.

3) Current state definitions:
   - Idle: The bank has been precharged, and t_{RP} has been met.
   - Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
   - Read: A READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   - Write: A WRITE burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   - Read with AP Enabled: Starts with registration of a READ command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.
   - Write with AP Enabled: Starts with registration of a WRITE command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.
4) AUTO REFRESH, SELF REFRESH and MODE REGISTER SET commands may only be issued when all banks are idle.
5) A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6) All states and sequences not shown are illegal or reserved.
7) READs or WRITEs listed in the Command/Action column include READs or WRITEs with Auto Precharge enabled and READs or WRITEs with Auto Precharge disabled.
8) Requires appropriate DQM masking.
9) Concurrent Auto Precharge: bank n will start precharging when its burst has been interrupted by a READ or WRITE command to bank m.

Table 16 Truth Table - CKE

CKEn-1	CKEn	Current State	Command	Action	Notes
L	L	Power Down	X	Maintain Power Down	1)2)3)4)
		Self Refresh	X	Maintain Self Refresh	1) to 4)
		Clock Suspend	X	Maintain Clock Suspend	1) to 4)
		Deep Power Down	X	Maintain Deep Power Down	1) to 4)
L	H	Power Down	DESELECT or NOP	Exit Power Down	1) to 4)
		Self Refresh	DESELECT or NOP	Exit Self Refresh	1) to 5)
		Clock Suspend	X	Exit Clock Suspend	1) to 4)
		Deep Power Down	X	Exit Deep Power Down	1) to 4)
H	L	All Banks Idle	DESELECT or NOP	Enter Precharge Power Down	1) to 4)
		Bank(s) Active	DESELECT or NOP	Enter Active Power Down	1) to 4)
		All Banks Idle	AUTO REFRESH	Enter Self Refresh	1) to 4)
		All Banks Idle	BURST STOP	Enter Deep Power Down	1) to 4)
		Read / Write burst	(valid)	Enter Clock Suspend	1) to 4)
H	H	see **Table 14** and **Table 15**			1) to 4)

1) CKEn is the logic state of CKE at clock edge n; CKEn-1 was the state of CKE at the previous clock edge.
2) Current state is the state immediately prior to clock edge n.
3) COMMAND n is the command registered at clock edge n; ACTION n is a result of COMMAND n.
4) All states and sequences not shown are illegal or reserved.
5) DESELECT or NOP commands should be issued on any clock edges occurring during t_{RC} period.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 17 Absolute Maximum Ratings

Parameter		Symbol	Values		Unit
			min.	max.	
Power Supply Voltage		V_{DD}	-1.0	4.6	V
Power Supply Voltage for Output Buffer		V_{DDQ}	-1.0	4.6	V
Input Voltage		V_{IN}	-1.0	V_{DDQ} + 0.5	V
Output Voltage		V_{OUT}	-1.0	V_{DDQ} + 0.5	V
Operation Case Temperature	Commercial	T_C	0	+70	°C
	Extended	T_C	-25	+85	°C
Storage Temperature		T_{STG}	-55	+150	°C
Power Dissipation		P_D	—	0.7	W
Short Circuit Output Current		I_{OUT}	—	50	mA

Attention: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

4.2 DC Operation Conditions

Table 18 DC Characteristics[1)]

Parameter	Symbol	Values		Unit	Notes
		min.	max.		
Power Supply Voltage	V_{DD}	2.3	3.6	V	–
Power Supply Voltage for DQ Output Buffer	V_{DDQ}	1.65 or 2.30	1.95 or 3.60	V	2)
Input high voltage	V_{IH}	0.8 × V_{DDQ}	V_{DDQ} + 0.3	V	3)
Input low voltage	V_{IL}	-0.3	0.3	V	3)
Output high voltage	V_{OH}	V_{DDQ} - 0.2	—	V	–
Output low voltage	V_{OL}	—	0.2	V	–
Input leakage current	I_{IL}	-5	5	µA	–
Output leakage current	I_{OL}	-5	5	µA	–

1) 0 °C ≤ T_C ≤ 70 °C (comm.);
All voltages referenced to V_{SS}. V_{SS} and V_{SSQ} must be at same potential.

2) Device is characterized for both ranges of V_{DDQ}; V_{DDQ} < V_{DD} +0.3

3) V_{IH} may overshoot to V_{DD} + 0.8 V for pulse width < 4 ns; V_{IL} may undershoot to -0.8 V for pulse width < 4 ns.
Pulse width measured at 50% with amplitude measured between peak voltage and DC reference level.

4.3 Pin Capacitances

Table 19 Pin Capacitances[1)2)]

Parameter	Symbol	Values		Unit
		min.	max.	
Input capacitance: CLK	C_{I1}	5.0	7.0	pF
Input capacitance: $\overline{CS0}$, $\overline{CS1}$	C_{I2}	3.0	5.0	pF
Input capacitance: all other input pins	C_{I3}	5.0	7.0	pF
Input/Output capacitance: DQ	C_{IO}	7.0	10.0	pF

1) These values are not subject to production test but verified by device characterization.

2) Input capacitance is measured according to JEP147 with VDD, VDDQ applied and all other pins (except the pin under test) floating. DQ's should be in high impedance state. This may be achieved by pulling CKE to low level.

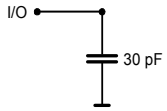
4.4 AC Characteristics

Table 20 AC Characteristics[1)]

Parameter			Symbol	- 7.5		Unit	Notes
				min.	max.		
Clock cycle time	V_{DDQ} = 2.3V .. 3.6V	CL = 3	t_{CK}	7.5	—	ns	—
		CL = 2		9.5	—	ns	—
	V_{DDQ} = 1.65V .. 1.95V	CL = 2 or 3		9.5	—	ns	—
Clock frequency	V_{DDQ} = 2.3V .. 3.6V	CL = 3	f_{CK}	—	133	MHz	—
	V_{DDQ} = 1.65V .. 1.95V	CL = 2 or 3		—	105	MHz	
Access time from CLK	V_{DDQ} = 2.3V .. 3.6V	CL = 2 or 3	t_{AC}	6.0	—	ns	2)3)
	V_{DDQ} = 1.65V .. 1.95V			8.0	—	ns	—
Clock high-level width			t_{CH}	2.5	—	ns	—
Clock low-level width			t_{CL}	2.5	—	ns	—
Address, data and command input setup time			t_{IS}	1.5	—	ns	4)
Address, data and command input hold time			t_{IH}	0.8	—	ns	4)
MODE REGISTER SET command period			t_{MRD}	2	—	t_{CK}	—
DQ low-impedance time from CLK			t_{LZ}	1.0	—	ns	—
DQ high-impedance time from CLK			t_{HZ}	3.0	7.0	ns	—
Data out hold time			t_{OH}	3.0	—	ns	2)5)
DQM to DQ High-Z delay (READ Commands)			t_{DQZ}	—	2	t_{CK}	—
DQM write mask latency			t_{DQW}	0	—	t_{CK}	—
ACTIVE to ACTIVE command period			t_{RC}	67	—	ns	5)
ACTIVE to READ or WRITE delay			t_{RCD}	19	—	ns	5)
ACTIVE bank A to ACTIVE bank B delay			t_{RRD}	15	—	ns	5)
ACTIVE to PRECHARGE command period			t_{RAS}	45	100k	ns	5)
WRITE recovery time			t_{WR}	14	—	ns	6)
PRECHARGE command period			t_{RP}	19	—	ns	5)
Refresh period (8192 rows)			t_{REF}	—	64	ms	—
Self refresh exit time			t_{SREX}	1	—	—	—

1) 0 °C ≤ T_C ≤ 70 °C (comm.); V_{DD} = 2.3V .. 3.6V; V_{DDQ} = 1.8 V ± 0.15 V; or 2.3V .. 3.6V;
All parameters assumes proper device initialization. AC timing tests measured at 0.9 V.
The transition time is measured between V_{IH} and V_{IL}; all AC characteristics assume t_T = 1 ns.

2) Specified t_{AC} and t_{OH} parameters are measured with a 30 pF capacitive load only as shown below:



3) If t_T(CLK) > 1 ns, a value of (t_T/2 - 0.5) ns has to be added to this parameter.

4) If t_T > 1 ns, a value of (t_T - 1) ns has to be added to this parameter.

5) These parameter account for the number of clock cycles and depend on the operating frequency, as follows:
no. of clock cycles = specified delay / clock period; round up to next integer.

6) The write recovery time of t_{WR} = 14 ns allows the use of one clock cycle for the write recovery time when f_{CK} ≤ 72 MHz. With f_{CK} > 72 MHz two clock cycles for t_{WR} are mandatory. Infineon Technologies recommends to use two clock cycles for the write recovery time in all applications..

4.5 Operating Currents

Table 21 Maximum Operating Currents[1)]

Parameter & Test Conditions	Symbol	Values	Unit	Notes
		- 7.5		
Operating Current: one bank: active / read / precharge, $t_{RC} = t_{RCmin}$	I_{CC1}	85	mA	2)3)
Precharge Standby Current in Power-Down Mode: all banks idle, $\overline{CS} \geq V_{IHmin}$, CKE $\leq V_{ILmax}$	I_{CC2P}	1.2	mA	2)
Precharge Standby Current in Non-Power Down Mode: all banks idle, $\overline{CS} \geq V_{IHmin}$, CKE $\geq V_{IHmin}$, inputs changing once per clock cycle	I_{CC2N}	40	mA	2)
Active Standby Current in Power Down Mode: one bank active, $\overline{CS} \geq V_{IHmin}$, CKE $\leq V_{ILmax}$, inputs changing once per clock cycle	I_{CC3P}	7	mA	2)
Active Standby Current in Non-Power Down Mode: one bank active, $\overline{CS} \geq V_{IHmin}$, CKE $\geq V_{IHmin}$, inputs changing once per clock cycle	I_{CC3N}	50	mA	2)
Operating Current for Burst Mode: all banks active; continuous burst read, inputs changing once per 2 clock cycles	I_{CC4}	100	mA	2)3)
Auto-Refresh Current: $t_{RC} = t_{RCmin}$, “burst refresh”	I_{CC5}	175	mA	2)
Deep Power Down Mode current	I_{CC7}	10	µA	–

1) 0 °C ≤ T_C ≤ 70 °C (comm.); V_{DD} = 2.3V .. 3.6V; V_{DDQ} = 1.8 V ± 0.15 V; or 2.3V .. 3.6V; Recommended Operating Conditions unless otherwise noted

2) These values are measured with t_{CK} = 7.5 ns for - 7.5 parts.

3) All parameters measured with no output loads.

Table 22 Self Refresh Currents[1)]

Parameter & Test Conditions	Max. Temperature	Symbol	Values	Units	Notes
			max.		
Self Refresh Current: Self refresh mode, CKE = 0.2 V, clock off, full array activation (PASR = 000)	85 °C	I_{CC6}	1600	µA	2)
	70 °C		1100		
	45 °C		900		
	15 °C		750		
Self Refresh Current: Self refresh mode, CKE = 0.2 V, clock off, half array activation (PASR = 001)	85 °C	I_{CC6}	1150	µA	2)
	70 °C		900		
	45 °C		800		
	15 °C		700		
Self Refresh Current: Self refresh mode, CKE = 0.2 V, clock off, quarter array activation (PASR = 010)	85 °C	I_{CC6}	900	µA	2)
	70 °C		800		
	45 °C		750		
	15 °C		675		

1) 0 °C ≤ T_C ≤ 70 °C (comm.); V_{DD} = 2.3V .. 3.6V; V_{DDQ} = 1.8 V ± 0.15 V; or 2.3V .. 3.6V;

2) Target values, to be verified on final product.

5 Package Outline

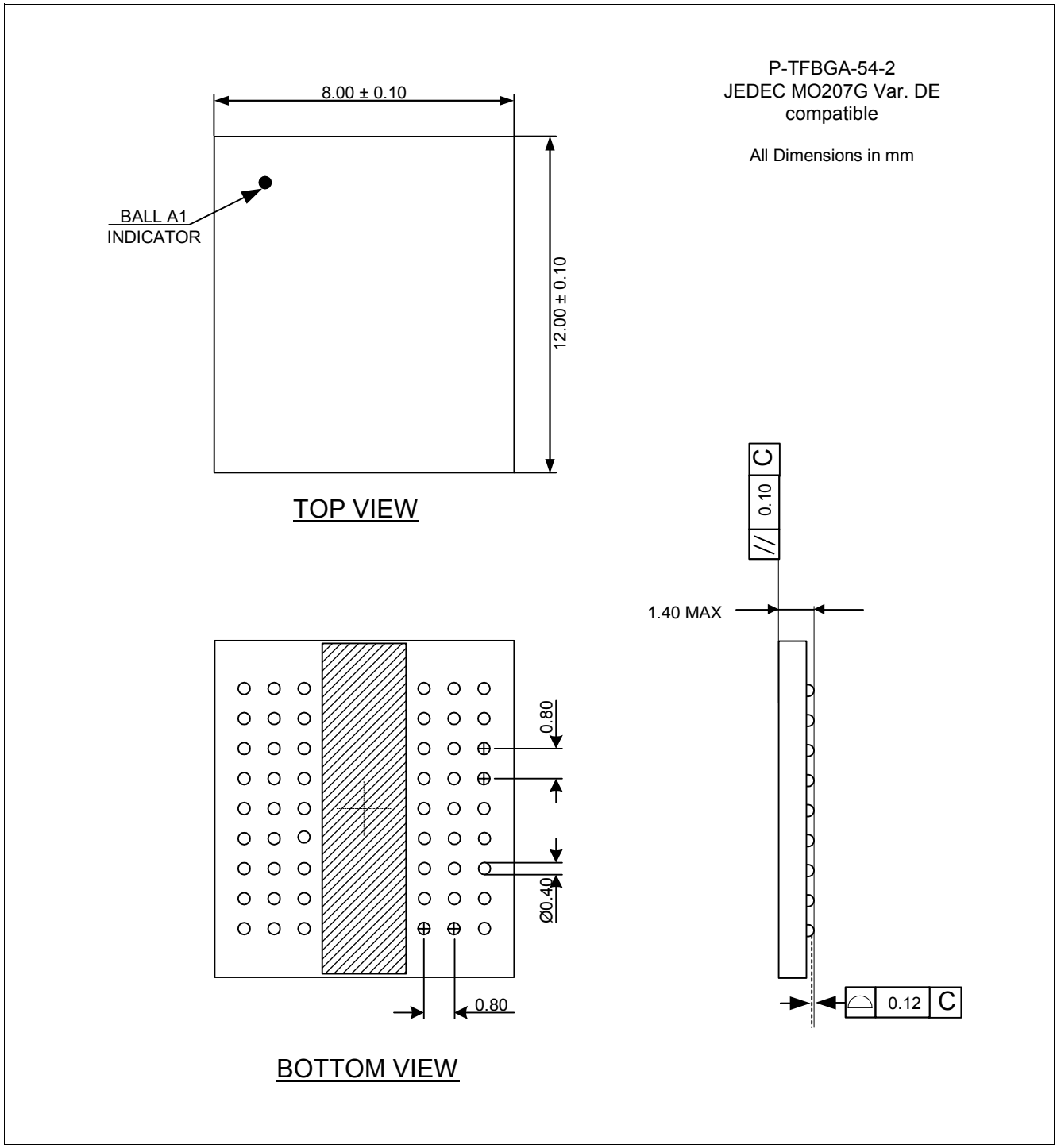


Figure 50 Package FBGA-54

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