Document Title

16M-BIT (1M-WORD BY 16-BIT) Low Power Pseudo SRAM

Revision History

Revision No	History	Draft Date	Remark
0A	Initial Draft	February 05,2004	Preliminary

16M-BIT (1M-WORD BY 16-BIT) Low-Power Pseudo SRAM

FEATURES

- Organization : 1M x 16
- Power Supply Voltage : 2.7~3.3V
- Three state output and TTL Compatible
- Package Type : 48-FBGA-6.00x8.00 mm^2
- Address Acess Time : 70ns

DESCRIPTION

The IC66LV10016AL is a family of low voltage, low power 16Mbit static RAM organized as 1M-words by 16-bit, designed with Pseudo SRAM technology, fabricated with CMOS process technology.

The IC66LV10016AL is designed specifically for low-power applications such as mobile cellular phones, personal digital assistants and other battery-operated products.

The operation modes are determined by a combination of the device control inputs $\overline{CE}$, $\overline{ZZ}$, $\overline{LB}$, $\overline{UB}$, $\overline{WE}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write operation is executed whenever the low level $\overline{WE}$ overlaps with the low level $\overline{LB}$ and/or $\overline{UB}$ and the low level $\overline{CE}$ and the high level $\overline{ZZ}$. The address (A0~A19) must be set up before the write cycle and must be stable during entire cycle.

A read operation is executed by setting $\overline{WE}$ at a high level and $\overline{OE}$ at a low level while $\overline{LB}$ and/or $\overline{UB}$ and $\overline{CE}$ are in an active state, $\overline{ZZ}$ is in a inactive state.

When setting $\overline{LB}$ at the high level and other controls are in an active stage, upper-byte is selected for read and write operations, and lower-byte is not selected. When setting $\overline{UB}$ at a high level and other pins are in an active stage, lower-byte is selected and upper-byte is not.

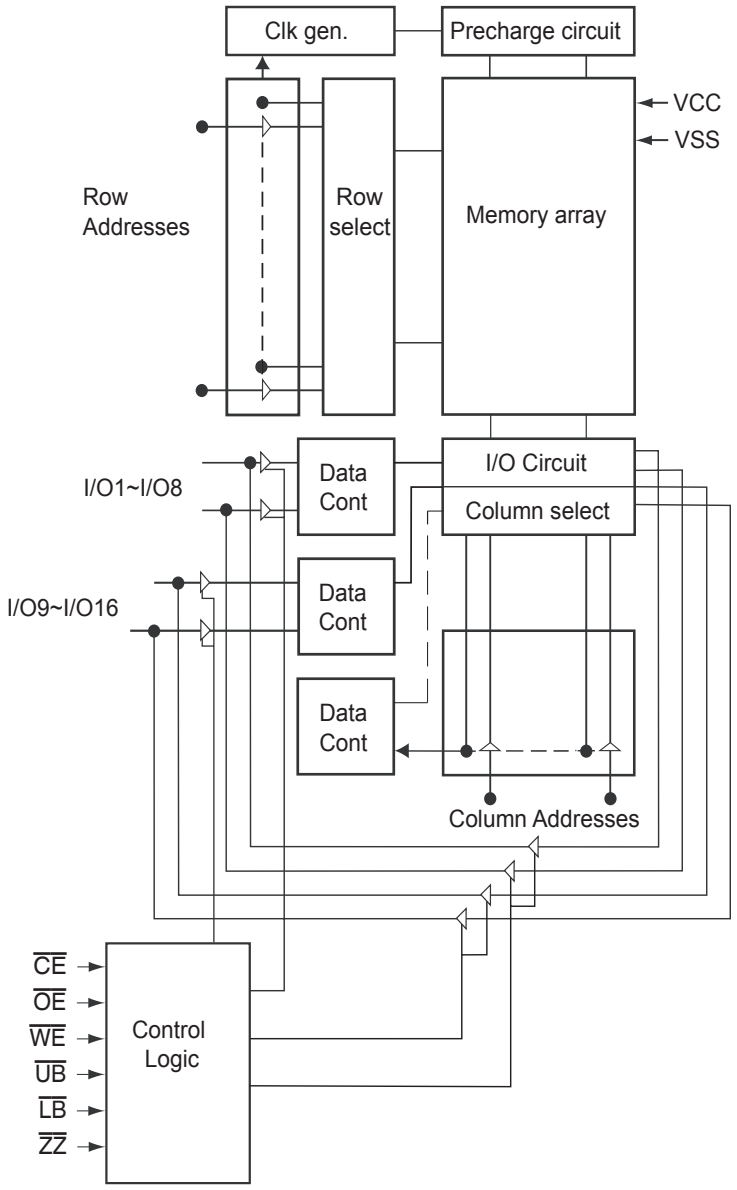
When setting $\overline{LB}$ and $\overline{UB}$ at a high level or $\overline{CE}$ and $\overline{ZZ}$ at a high level or $\overline{ZZ}$ at a low level, the chip is in a non-select mode. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips.

When $\overline{OE}$ is at a high level, the output stage is in a high-impedance state.

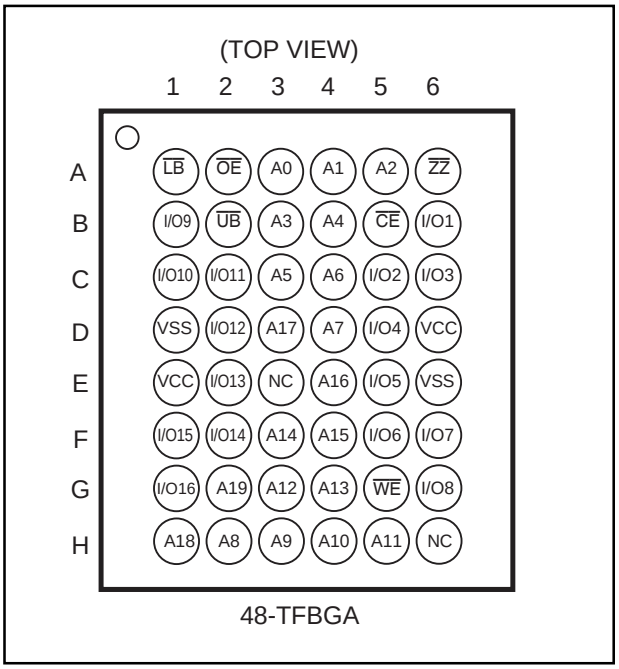
PART NAME TABLE & KEY SPEC SUMMARY

Product Family	Operating Temperature	Operating Voltage (VCC/VCCQ)	Speed	Deep powe down (I_{ZZ},Max)	Standby (I_{SB2},Max)	Operating (I_{CC2},Max)	PKG Type
IC66LV10016AL-70B	Extended (-25-85°C)	2.7-3.3V	70ns	25µA	70µA	20mA	48-TFBGA

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin	Function
A0~A19	Address input
I/O1 ~ I/O16	Data input / output
$\overline{ZZ}$	Low power modes
$\overline{CE}$	Chip select input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
$\overline{UB}$	Upper Byte (I/O9 ~ 16)
$\overline{LB}$	Lower Byte (I/O1 ~ 8)
VCC	Power supply
VSS	Ground supply
NC	No connection

FUNCTION TABLE

$\overline{CE}$	$\overline{ZZ}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1-8	I/O9-16	Mode	Power
H	H	X(1)	X(1)	X(1)	X(1)	High-Z	High-Z	Deselected	Standby
X(1)	L	X(1)	X(1)	X(1)	X(1)	High-Z	High-Z	Deselected	Deep Power Down Mode
L	H	H	H	X(1)	X(1)	High-Z	High-Z	Output disabled	Active
L	H	X(1)	H	H	H	High-Z	High-Z	Output disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower byte read	Active
L	H	L	H	H	L	High-Z	Dout	Upper byte read	Active
L	H	L	H	L	L	Dout	Dout	Word read	Active
L	H	H	L	L	H	Din	High-Z	Lower byte write	Active
L	H	H	L	H	L	High-Z	Din	Upper byte write	Active
L	H	H	L	L	L	Din	Din	Word write	Active

Notes:

1. X means don't-care.(Must be low or hight state)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{IN},V_{OUT}	Voltage on any pin relative to Vss	-0.2 to Vcc+0.3	V
Vcc	Voltage on Vcc supply relative to Vss	-0.2 to 3.6	V
PD	Power Dissipation	1.0	W
T_{STG}	Storage Temperature	-65 to 150	°C
Toper	Operating Temperature	-25 to 85	°C

Note:
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (1)

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Supply Voltage		2.7	3.3	V
V_{IH}	Input High Voltage		Vcc-0.3	Vcc+0.3(2)	V
V_{IL}	Input Low Voltage		-0.3(3)	0.3	V
I_{LI}	Input Leakage current	V_{IN}=Vss to Vcc	-1	1	µA
I_{LO}	Output Leakage current	V_{OUT}=Vss to Vcc Output Disable	-1	1	µA
V_{OL}	Output low Voltage	I_{OL}=0.5mA		0.3	V
V_{OH}	Output high Voltage	I_{OH}=-0.5mA	Vcc-0.3		V

Notes:
1. Toper=-25 to 85°C, otherwise specified.
2. Overshoot : Vcc+1.0V in case of pulse width ≤ 20ns
3. Undershoot : -1.0V in case of pulse width ≤ 20ns
4. Overshoot and undershoot are sampled, not 100% tested.

POWER CONSUMPTION CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Max	Units
$I_{CC}1$	Vcc operating supply current	Cycle time=1µs,100% duty I_{OUT}=0mA,$\overline{CE}$≤0.2V,$\overline{ZZ}$=V_{IH}, V_{IN}≤0.2V or V_{IN}≥Vcc-0.2V	—	3	mA
$I_{CC}2$	Vcc Dynamic operation supply current	Cycle time=tRCmin,100% duty I_{OUT}=0mA,$\overline{CE}$=V_{IL},$\overline{ZZ}$=V_{IH}, V_{IN}=V_{IL} or V_{IH}	—	20	mA
$I_{SB}1$	TTL Standby Current (TTL inputs)	$\overline{CE}$=V_{IH},$\overline{ZZ}$=V_{IH}, Other inputs=V_{IL} or V_{IH}	—	0.3	mA
$I_{SB}2$	CMOS Standby Current (CMOS inputs)	$\overline{CE}$≥Vcc-0.2V,$\overline{ZZ}$≥Vcc-0.2V, V_{IN}≤0.2V or V_{IN}≥Vcc-0.2V	—	70	µA
I_{ZZ}	Deep power down mode	$\overline{ZZ}$≤0.2V, V_{IN}≤0.2V or V_{IN}≥Vcc-0.2V	—	25	µA

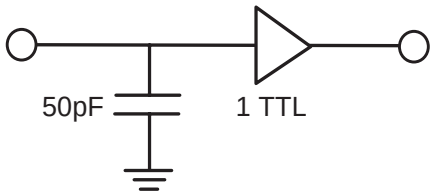
CAPACITANCE

Symbol	Parameter	Test Condition	Min	Max	Notes
C_{IN}	Input Capacitance	V_{IN}=0V	-	8	pF
C_{IO}	Output Capacitance	V_{IO}=0V	-	10	pF

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Input/Output Reference)

Parameter	Value
Input pulse level	0.3 to Vcc-0.3V
Input rise and fall time	5ns
Input and output reference voltage	0.5Vcc
Output loads	CL=50pF+1TTL



AC CHARATERISTICS
READ CYCLE

Symbol	Parameter	-70		
		Min	Max	Units
tRC	Read Cycle Time	70	32K	ns
tAA	Address Access time	—	70	ns
tOHA	Output Hold Time	5	—	ns
tACE	$\overline{CE}$ Access Time	—	70	ns
tDOE	$\overline{OE}$ Access Time	—	40	ns
tBA	$\overline{UB}$, $\overline{LB}$ Access Time	—	25	ns
tASO	Address set up to $\overline{OE}$ Low	-5	—	ns
tASC	Address set up to $\overline{CE}$ Low	0	—	ns
tAHC	Address hold time from $\overline{OE}$ High	0	—	ns
tLZCE	$\overline{CE}$ to Low-Z Output	0	—	ns
tLZB	$\overline{UB}$, $\overline{LB}$ to Low-Z Output	0	—	ns
tLZOE	$\overline{OE}$ to Low-Z Output	0	—	ns
tHZCE	$\overline{CE}$ to High- Z Output	—	15	ns
tHZB	$\overline{UB}$, $\overline{LB}$ to High- Z Output	—	15	ns
tHZOE	$\overline{OE}$ to High-Z Output	—	15	ns

WRITE CYCLE

Symbol	Parameter	-70		
		Min	Max	Units
tWC	Write Cycle Time	70	32K	ns
tSCE	$\overline{CE}$ to Write End	60	—	ns
tSA	Address Setup Time	0	—	ns
tAW	Address Setup Time to Write End	60	—	ns
tASC	Address set up to $\overline{CE}$ Low	0	—	ns
tAHC	Address hold time from $\overline{OE}$ High	0	—	ns
tPWE	$\overline{WE}$ Pulse Width	40	—	ns
tPWB	$\overline{LB}$, $\overline{UB}$ to End of Write	60	—	ns
tHA	Address Hold from Write End	0	—	ns
tSD	Data Setup to Write End	30	—	ns
tHD	Data Hold from Write End	0	—	ns

tCP	$\overline{CE}$ High Pulse width	30	—	ns

Power Down Cycle(Ta = -25~85 °C)

Symbol	Parameter	Min	Max	Units
tSSP	$\overline{CE}$ High set up time for Power Down entry	0	—	ns
tSHP	$\overline{CE}$ High hold time before Power Down exit	0	—	ns
TC2LP	$\overline{ZZ}$ Low pulse width	30	—	ns
tHPD	$\overline{CE}$ High hold time after Power Down exit	300	—	µs

Power Up Timing Requirement(Ta = -25~85 °C)

Symbol	Parameter	Min	Max	Units
tSHU	$\overline{CE}$ $\overline{ZZ}$ set up time after Power Up	0	—	ns
tHPU	Standby hold time after Power Up	300	—	µs

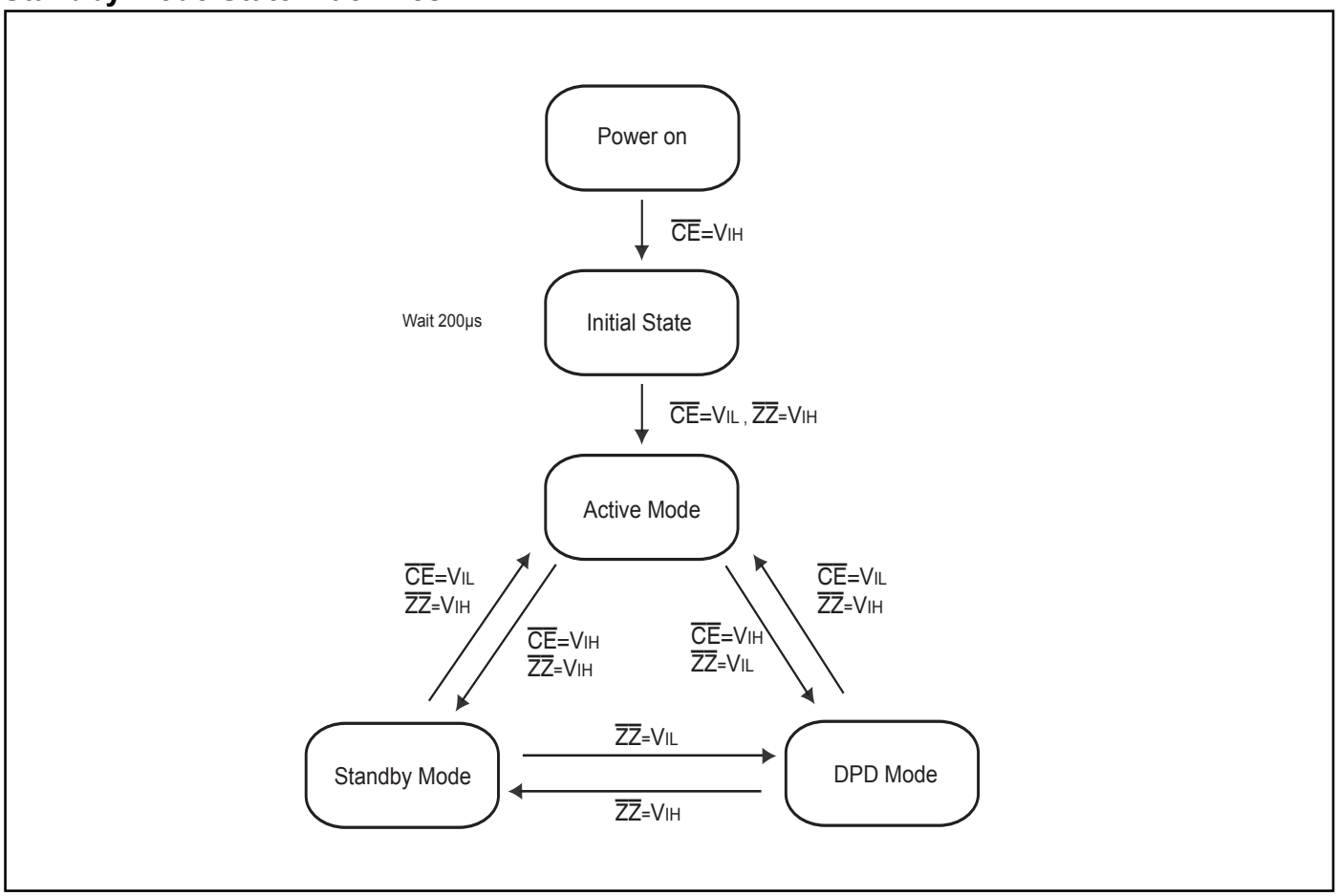
Data Retention Timing Requirement(Ta = -25~85 °C)

Symbol	Parameter	Min	Max	Units
tBAH	A2 to A19 hold time during active	0	—	ns
tCSH	$\overline{CE}$ hold time for A2 to A19 fix	300	—	µs

Address Skew Timing Requirement(Ta = -25~85 °C)

Symbol	Parameter	Min	Max	Units
tSKEW	Maximum address skew	—	10	ns

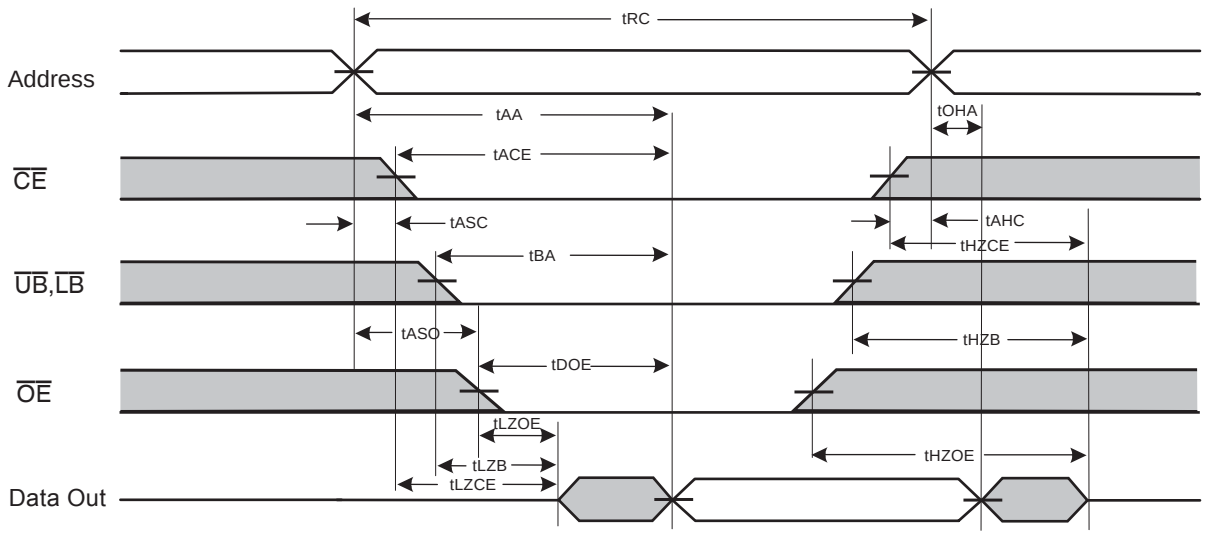
Standby Mode State machines



Standby Mode Characteristics

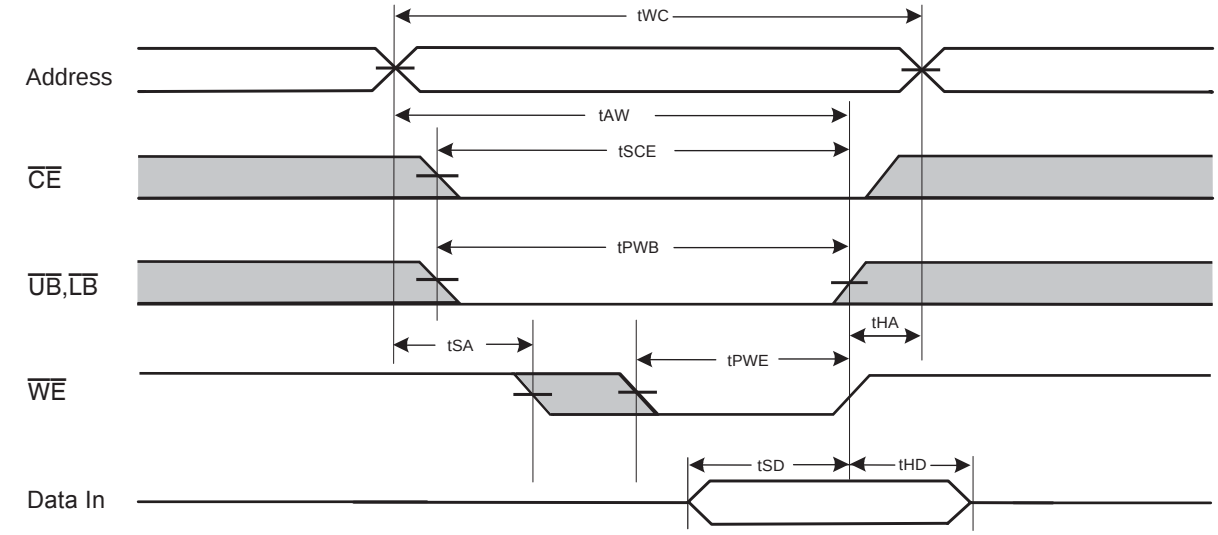
Mode	Memory Cell Data	Standby Current(µA)	Wait Time(µS)
Standby	Valid	70	0
DPD Mode	Invalid	25(I_{ZZ})	300

READ CYCLE



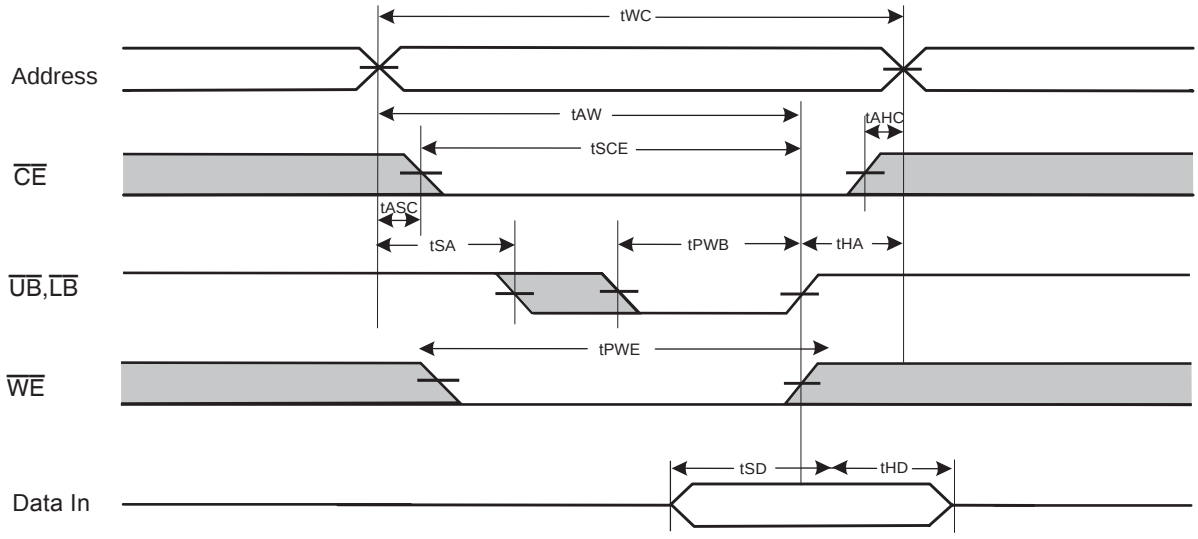
$\overline{ZZ}$ and $\overline{WE}$ must be H level for entire read cycle

WRITE CYCLE ($\overline{WE}$ Control)



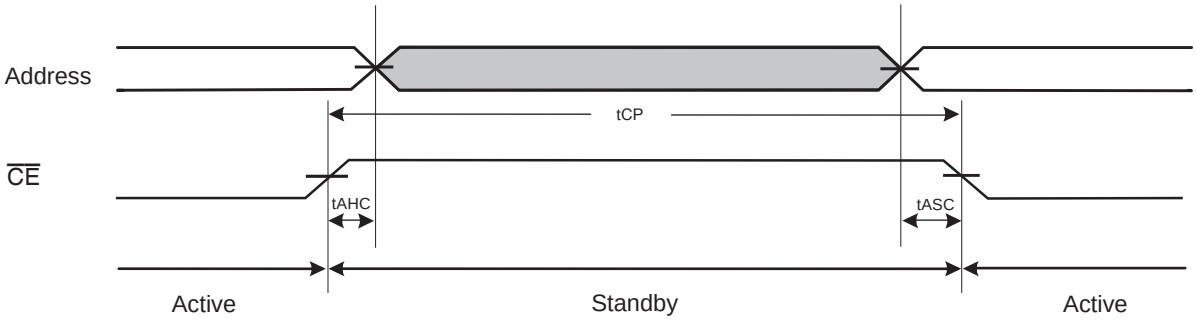
$\overline{ZZ}$ and $\overline{OE}$ must be H level for entire read cycle

WRITE CYCLE ($\overline{LB}$ $\overline{UB}$ Control)

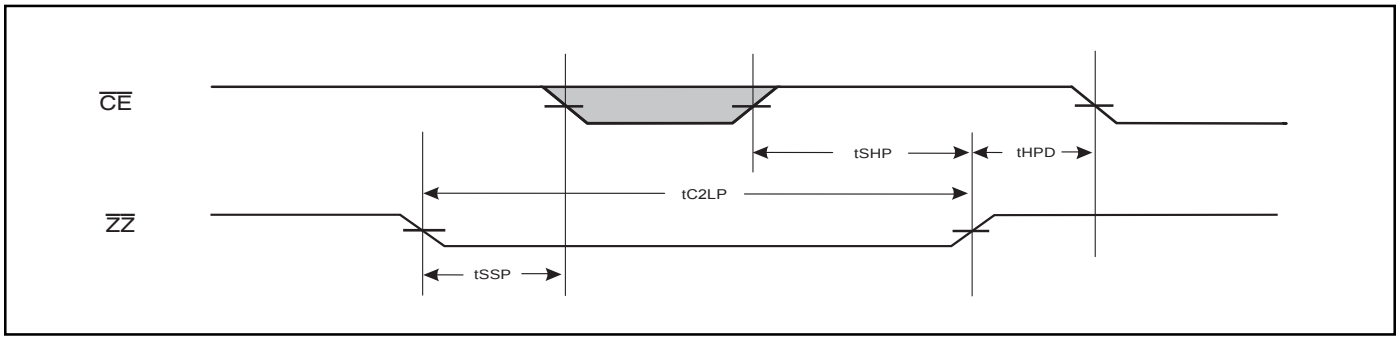


$\overline{ZZ}$ and $\overline{OE}$ must be H level for entire read cycle

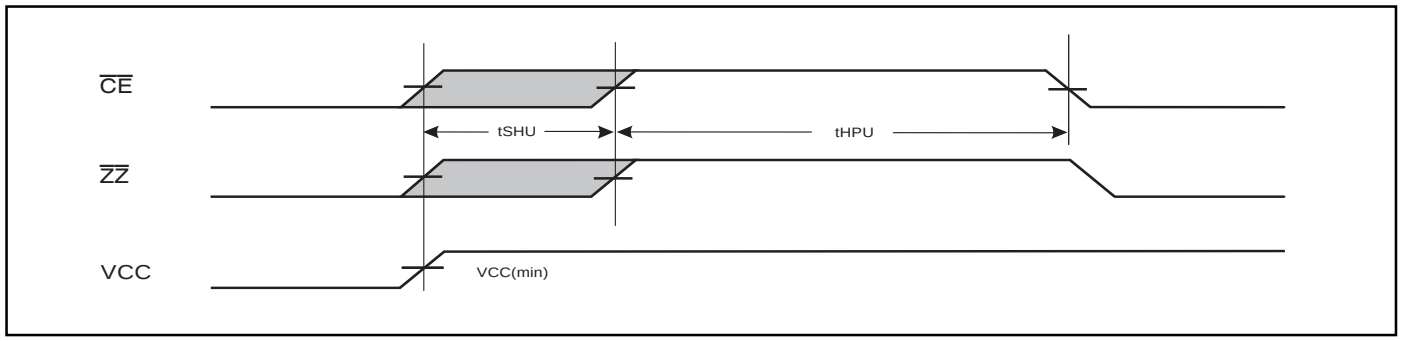
STANDBY



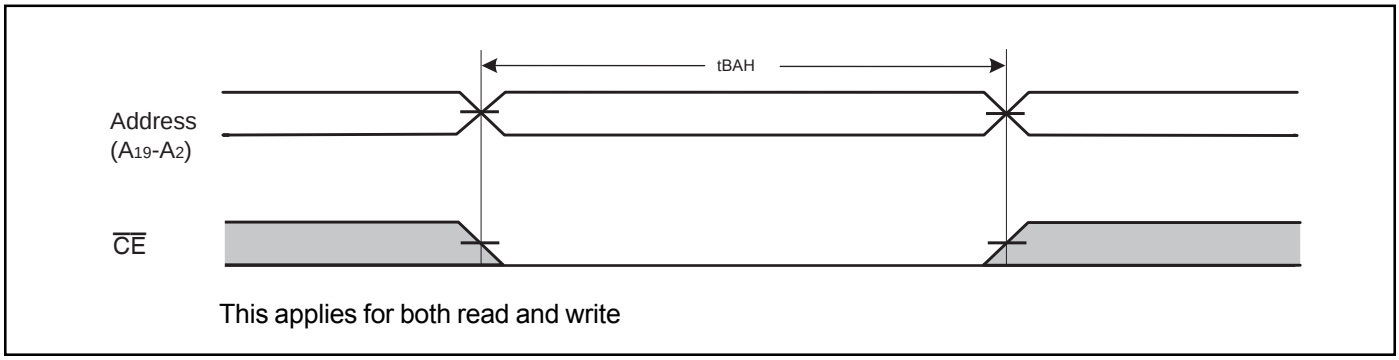
Power Down Mode Entry / Exit



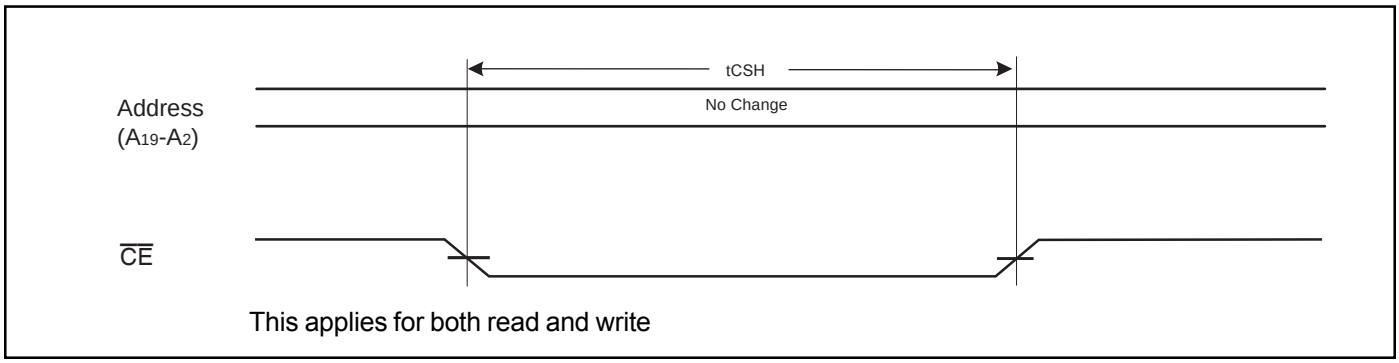
Power Up



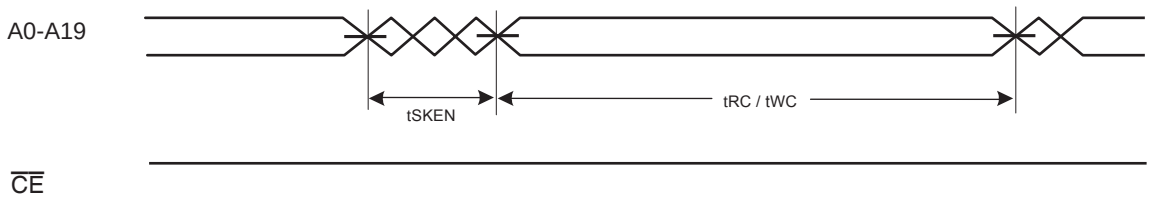
Data Retention(1)



Data Retention(2)

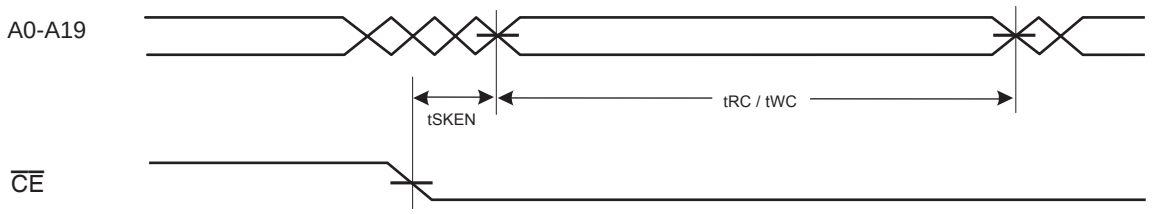


Address Skew(1)



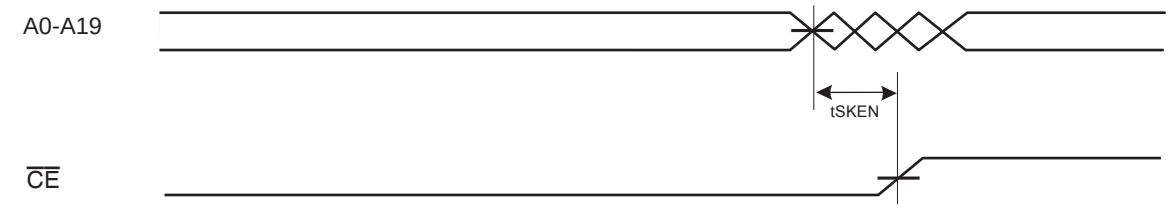
tSKEN is from first address change to last address change

Address Skew(2)



tSKEN is from first address change to last address change

Address Skew(2)



tSKEN is from first address change to last address change

ORDERING INFORMATION
Temperature Range: -25°C to +85°C

Order Part No.	Speed (ns)	Package
IC66LV10016AL-70B	70	6*8mm TFBGA

Integrated Circuit Solution Inc.
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NO.2, TECHNOLOGY RD. V, SCIENCE-BASED INDUSTRIAL PARK,
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