



GENERAL DESCRIPTION

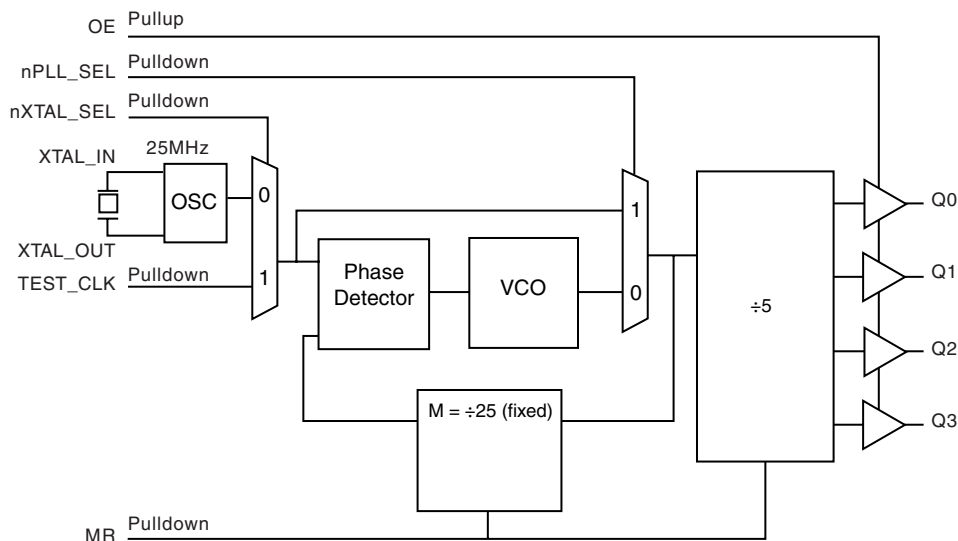


The ICS840024I is a 4 output LVCMOS/LVTTL Synthesizer optimized to generate Ethernet reference clock frequency and is a member of the HiPerClocks™ family of high performance clock solutions from ICS. The ICS840024I uses ICS' 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical random rms phase jitter, easily meeting Ethernet jitter requirements. The ICS840024I is packaged in a small 20-pin TSSOP package.

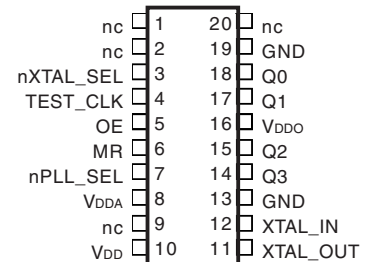
FEATURES

- Four LVCMOS/LVTTL outputs, 15Ω typical output impedance
- Selectable crystal oscillator interface or LVCMOS single-ended input
- Supports the following output frequency: 125MHz
- RMS phase jitter @ 125MHz (1.875MHz - 20MHz): 0.60ps (typical)
- Output supply modes:
Core/Output
3.3V/3.3V
3.3V/2.5V
2.5V/2.5V
- -40°C to 85°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS840024I

20-Lead TSSOP

6.5mm x 4.4mm x 0.92mm
package body
G Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.



TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|----------------|-------------------|--------|----------|---|
| 1, 2, 9, 20 | nc | Unused | | No connect. |
| 3 | nXTAL_SEL | Input | Pulldown | Selects between the crystal or TEST_CLK inputs as the PLL reference source. When HIGH, selects TEST_CLK. When LOW, selects XTAL inputs. LVCMOS/LVTTL interface levels. |
| 4 | TEST_CLK | Input | Pulldown | Single-ended LVCMOS/LVTTL clock input. |
| 5 | OE | Input | Pullup | Output enable pin. When HIGH, the outputs are active. When LOW, the outputs are in a high impedance state. LVCMOS/LVTTL interface levels. |
| 6 | MR | Input | Pulldown | Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the outputs to go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels. |
| 7 | nPLL_SEL | Input | Pulldown | PLL Bypass. When LOW, the output is driven from the VCO output. When HIGH, the PLL is bypassed and the output frequency = reference clock frequency/N output divider. LVCMOS/LVTTL interface levels. |
| 8 | V _{DDA} | Power | | Analog supply pin. |
| 10 | V _{DD} | Power | | Core supply pin. |
| 11, 12 | XTAL_OUT, XTAL_IN | Input | | Crystal oscillator interface. XTAL_OUT is the output. XTAL_IN is the input. |
| 13, 19 | GND | Power | | Power supply ground. |
| 14, 15, 17, 18 | Q3, Q2, Q1, Q0 | Output | | Single-ended clock outputs. LVCMOS/LVTTL interface levels. 15Ω typical output impedance. |
| 16 | V _{DDO} | Power | | Output supply pin. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------------|--|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 4 | | pF |
| C _{PD} | Power Dissipation Capacitance | V _{DD} , V _{DDA} , V _{DDO} = 3.465V | | TBD | | pF |
| | | V _{DD} , V _{DDA} = 3.465V, V _{DDO} = 2.625V | | TBD | | pF |
| | | V _{DD} , V _{DDA} , V _{DDO} = 2.625V | | TBD | | pF |
| R _{PULLUP} | Input Pullup Resistor | | | 51 | | KΩ |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | KΩ |
| R _{OUT} | Output Impedance | | | 15 | | Ω |



ABSOLUTE MAXIMUM RATINGS

| | |
|--|--------------------------|
| Supply Voltage, V_{DD} | 4.6V |
| Inputs, V_i | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, V_o | -0.5V to $V_{DD} + 0.5V$ |
| Package Thermal Impedance, θ_{JA} | 73.2°C/W (0 lfm) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DDD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| V_{DD} | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDA} | Analog Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDO} | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| I_{DD} | Power Supply Current | | | 75 | | mA |
| I_{DDA} | Analog Supply Current | | | 6 | | mA |
| I_{DDO} | Output Supply Current | | | 3 | | mA |

TABLE 3B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| V_{DD} | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDA} | Analog Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDO} | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| I_{DD} | Power Supply Current | | | 75 | | mA |
| I_{DDA} | Analog Supply Current | | | 6 | | mA |
| I_{DDO} | Output Supply Current | | | 3 | | mA |

TABLE 3C. POWER SUPPLY DC CHARACTERISTICS, $V_{DDD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| V_{DD} | Core Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| V_{DDA} | Analog Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| V_{DDO} | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| I_{DD} | Power Supply Current | | | 70 | | mA |
| I_{DDA} | Analog Supply Current | | | 6 | | mA |
| I_{DDO} | Output Supply Current | | | 3 | | mA |



TABLE 3D. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ OR $2.5V \pm 5\%$, OR $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-----------------------------|-----------------------------------|---|---------|---------|----------------|---------------|
| V_{IH} | Input High Voltage | OE, MR, nPLL_SEL, nXTAL_SEL, | | 2 | | $V_{DD} + 0.3$ | V |
| | | TEST_CLK | | 2 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | OE, MR, nPLL_SEL, nXTAL_SEL, | | -0.3 | | 0.8 | V |
| | | TEST_CLK | | -0.3 | | 1.3 | V |
| I_{IH} | Input High Current | OE | $V_{DD} = V_{IN} = 3.465\text{V}$ or 2.625V | | | 5 | μA |
| | | nPLL_SEL, MR, nXTAL_SEL, TEST_CLK | $V_{DD} = V_{IN} = 3.465\text{V}$ or 2.625V | | | 150 | μA |
| I_{IL} | Input Low Current | OE | $V_{DD} = 3.465\text{V}$ or 2.625V , $V_{IN} = 0\text{V}$ | -150 | | | μA |
| | | nPLL_SEL, MR, nXTAL_SEL, TEST_CLK | $V_{DD} = 3.465\text{V}$ or 2.625V , $V_{IN} = 0\text{V}$ | -5 | | | μA |
| V_{OH} | Output High Voltage; NOTE 1 | | $V_{DDO} = 3.3V \pm 5\%$ | 2.6 | | | V |
| | | | $V_{DDO} = 2.5V \pm 5\%$ | 1.8 | | | V |
| V_{OL} | Output Low Voltage; NOTE 1 | | $V_{DDO} = 3.3V$ or $2.5V \pm 5\%$ | | | 0.5 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Information, Output Load Test Circuit.

TABLE 4. CRYSTAL CHARACTERISTICS

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | | 25 | | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |

NOTE: Characterized using an 18pf parallel resonant crystal.



TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------|--------------------------------------|--|---------|---------|---------|-------|
| f_{OUT} | Output Frequency | | | 125 | | MHz |
| $t_{sk(o)}$ | Output Skew; NOTE 1, 3 | | | TBD | | ps |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter (Random); NOTE 2 | Intergration Range 1.875MHz - 20MHz | | 0.60 | | ps |
| t_L | PLL Lock Time | | | TBD | | ms |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | | 400 | | ps |
| odc | Output Duty Cycle | | | 50 | | % |

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions.
Measured at $V_{DDO}/2$.

NOTE 2: Please refer to the Phase Noise Plot.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------|--------------------------------------|--|---------|---------|---------|-------|
| f_{OUT} | Output Frequency | | | 125 | | MHz |
| $t_{sk(o)}$ | Output Skew; NOTE 1, 3 | | | TBD | | ps |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter (Random); NOTE 2 | Intergration Range 1.875MHz - 20MHz | | 0.55 | | ps |
| t_L | PLL Lock Time | | | TBD | | ms |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | | 400 | | ps |
| odc | Output Duty Cycle | | | 50 | | % |

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions.
Measured at $V_{DDO}/2$.

NOTE 2: Please refer to the Phase Noise Plot.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5C. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------|--------------------------------------|--|---------|---------|---------|-------|
| f_{OUT} | Output Frequency | | | 125 | | MHz |
| $t_{sk(o)}$ | Output Skew; NOTE 1, 3 | | | TBD | | ps |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter (Random); NOTE 2 | Intergration Range 1.875MHz - 20MHz | | 0.50 | | ps |
| t_L | PLL Lock Time | | | TBD | | ms |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | | 400 | | ps |
| odc | Output Duty Cycle | | | 50 | | % |

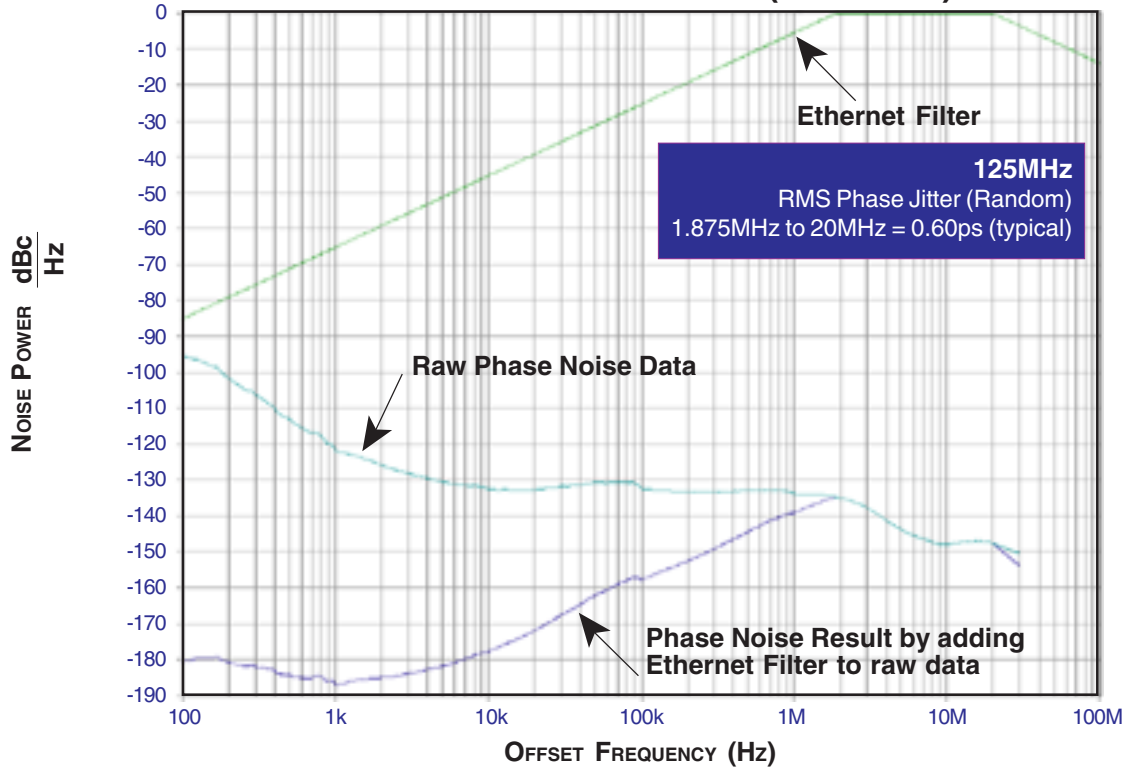
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions.
Measured at $V_{DDO}/2$.

NOTE 2: Please refer to the Phase Noise Plot.

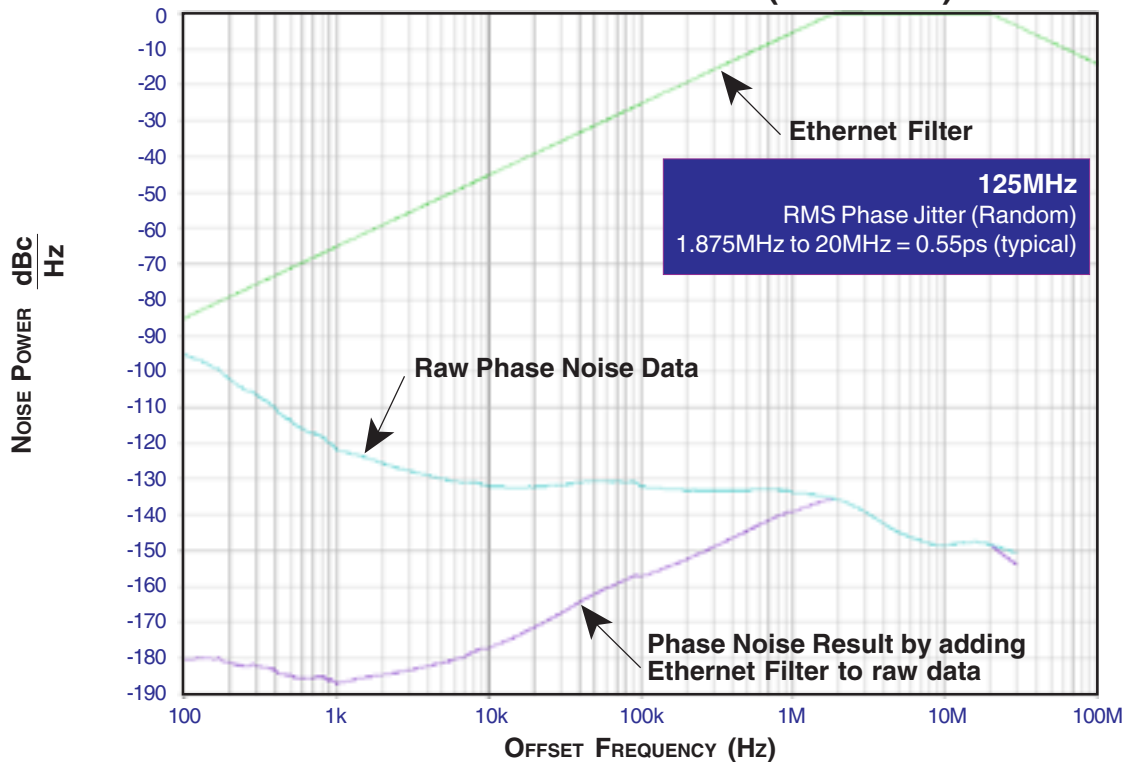
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.



TYPICAL PHASE NOISE AT 125MHz (3.3V/3.3V)

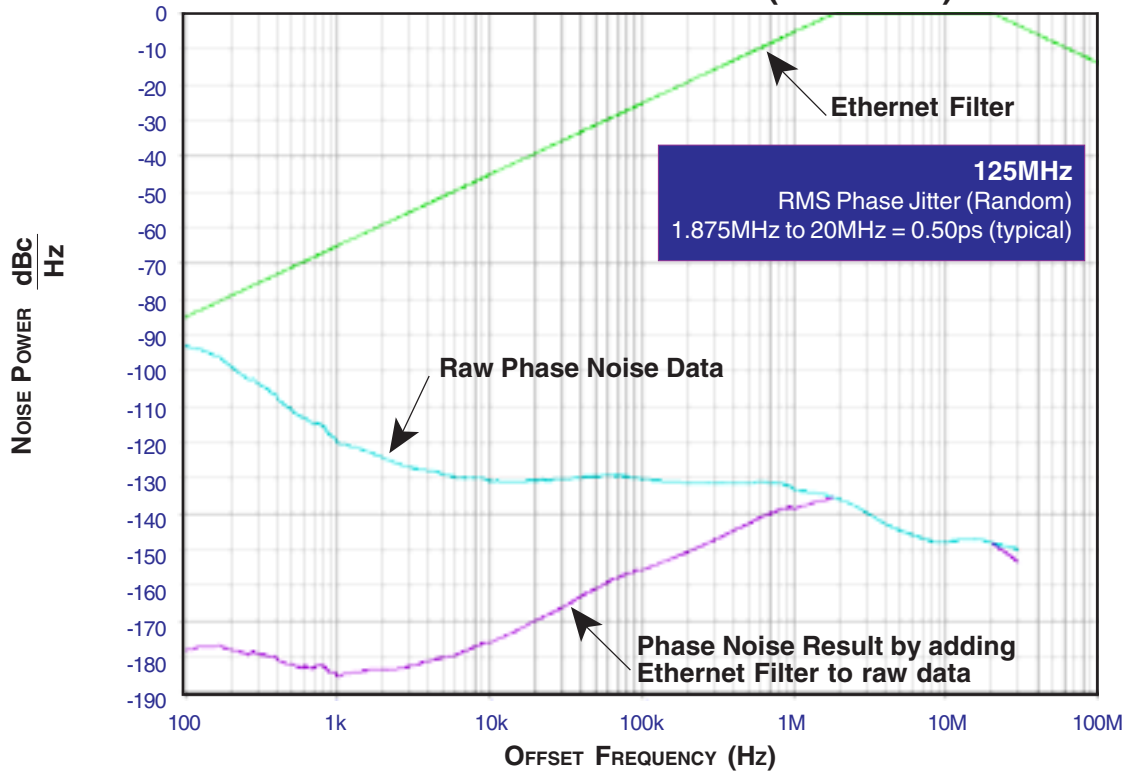


TYPICAL PHASE NOISE AT 125MHz (3.3V/2.5V)



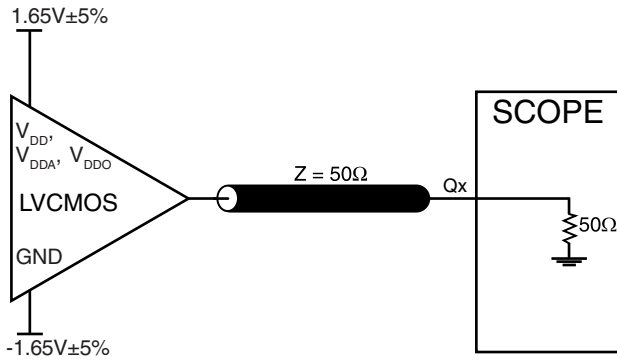


TYPICAL PHASE NOISE AT 125MHz (2.5V/2.5V)

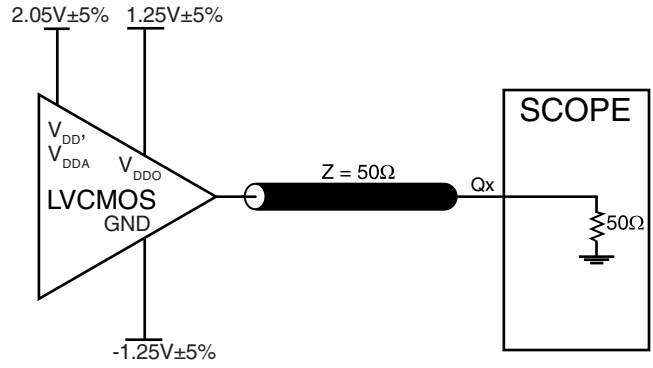




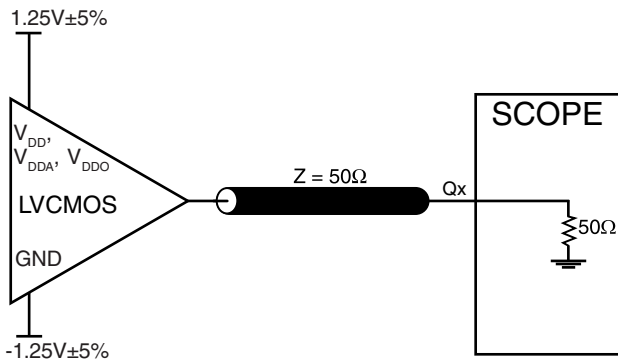
PARAMETER MEASUREMENT INFORMATION



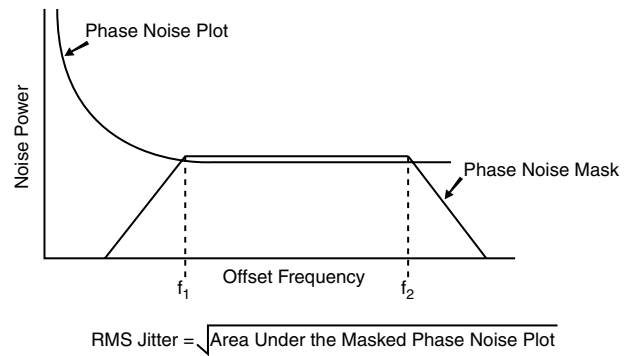
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



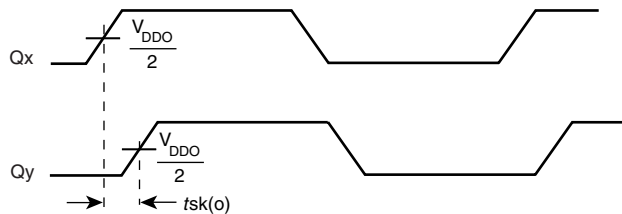
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



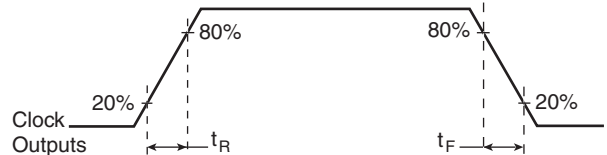
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



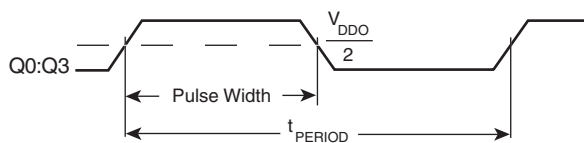
RMS PHASE JITTER



OUTPUT SKEW



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

$$odc = \frac{t_{PW}}{t_{PERIOD}}$$



APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS840024I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} , V_{DDA} , and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a $10\mu\text{F}$ and a $.01\mu\text{F}$ bypass capacitor should be connected to each V_{DDA} .

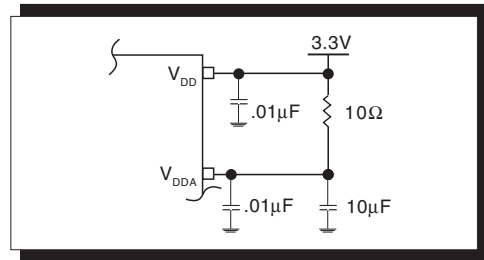


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS840024I has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2*

below were determined using a 25MHz 18pF parallel resonant crystal and were chosen to minimize the ppm error.

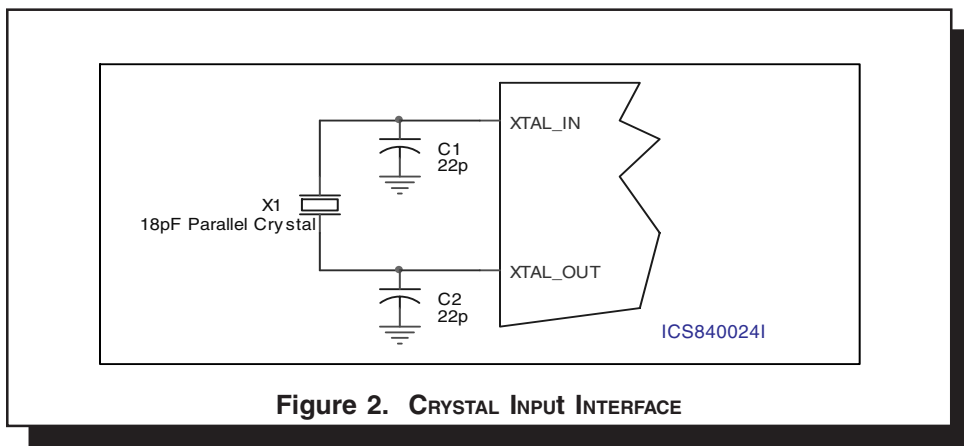


Figure 2. CRYSTAL INPUT INTERFACE



RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD TSSOP

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|--|-----------|------------|------------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 73.2°C/W | 66.6°C/W | 63.5°C/W |

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS840024I is: 3085



PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP

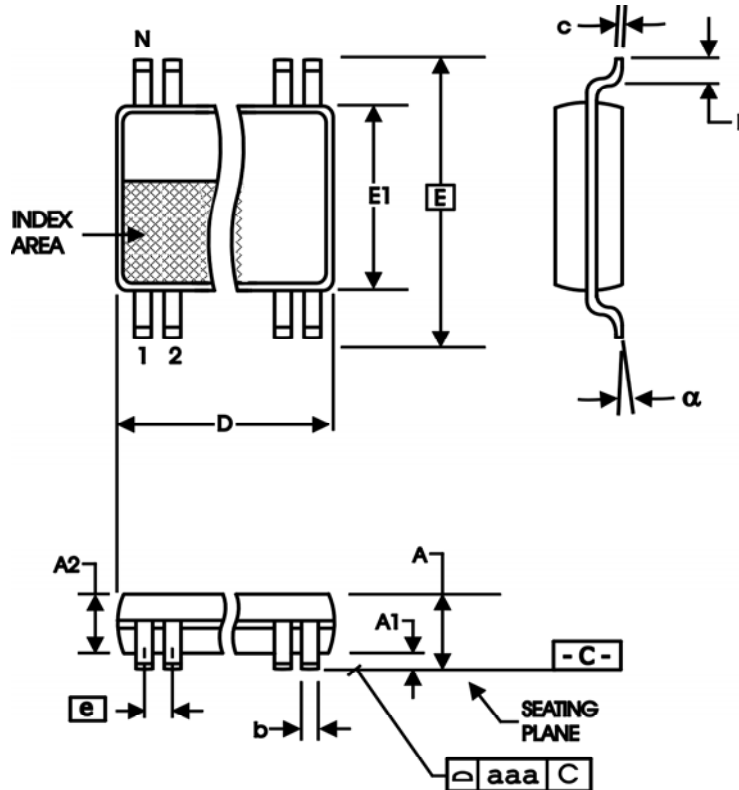


TABLE 7. PACKAGE DIMENSIONS

| SYMBOL | Millimeters | |
|--------|-------------|------|
| | MIN | MAX |
| N | 20 | |
| A | -- | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 6.40 | 6.60 |
| E | 6.40 BASIC | |
| E1 | 4.30 | 4.50 |
| e | 0.65 BASIC | |
| L | 0.45 | 0.75 |
| alpha | 0° | 8° |
| aaa | -- | 0.10 |

Reference Document: JEDEC Publication 95, MO-153



Integrated
Circuit
Systems, Inc.

PRELIMINARY

ICS840024I
FEMTOCLOCKS™ CRYSTAL-TO-
LVCMOS/LVTTL FREQUENCY SYNTHESIZER

TABLE 8. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Count | Temperature |
|-------------------|---------|--------------------------------|-------------|---------------|
| ICS840024AGI | TBD | 20 Lead TSSOP | 72 per tube | -40°C to 85°C |
| ICS840024AGIT | TBD | 20 Lead TSSOP on Tape and Reel | 2500 | -40°C to 85°C |

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