PRELIMINARY

Integrated
Circuit
Systems, Inc.

ICS84327

CRYSTAL-TO-3.3V LVPECL FREQUENCY SYNTHESIZER W/INTEGRATED FANOUT BUFFER

GENERAL DESCRIPTION

The ICS84327 is a Crystal-to-3.3V LVPECL Clock Synthesizer/Fanout Buffer designed for SONET, 10 Gigabit Fibre Channel and 10 Gigabit Ethernet applications and is a member of the HiperClockS family of High Performance Clock Solutions from ICS. The output frequency can be set using the frequency select pins and a 19.44MHz crystal for SONET frequencies, or a 25MHz crystal for 10 Gigabit Ethernet frequencies, or a 25.5MHz crystal for a 10 Gigabit Fibre Channel. The low phase noise characteristics of the ICS84327 make it an ideal clock for these demanding applications.

FUNCTION TABLE

Inputs					Output Frequency
F_XTAL	**MR**	**SEL2**	**SEL1**	**SEL0**	**F_OUT**
X	1	X	X	X	LOW
19.44MHz	0	1	0	0	77.76MHz
19.44MHz	0	1	0	1	155.52MHz
19.44MHz	0	1	1	0	311.04MHz
19.44MHz	0	1	1	1	622.08MHz
25MHz	0	0	0	0	78.125MHz
25MHz	0	0	0	1	156.25MHz
25MHz	0	0	1	0	312.5 MHz
25MHz	0	0	1	1	625MHz
25.5MHz	0	0	0	1	159.375MHz

FEATURES

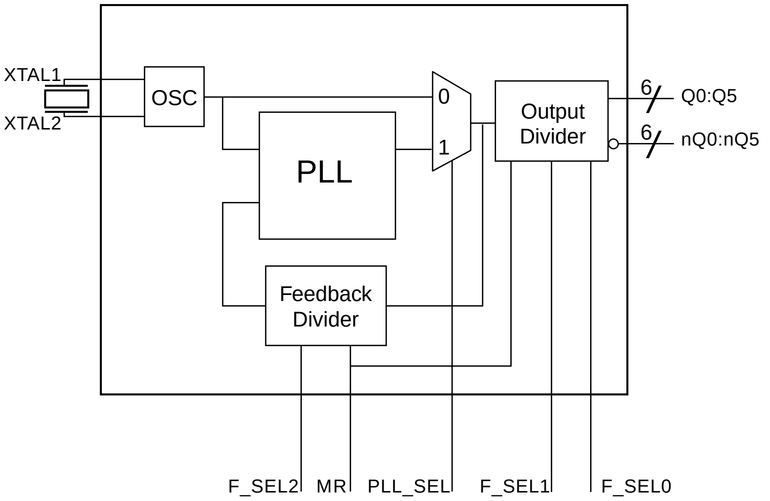
- 6 LVPECL outputs
- Crystal oscillator interface
- Output frequency range: 77.76MHz to 625MHz
- Crystal input frequency: 19.44MHz, 25MHz or 25.5MHz
- RMS phase jitter at 155.52MHz, using a 19.44MHz crystal (12KHz to 20MHz): 3.4ps (typical)

  Phase noise:

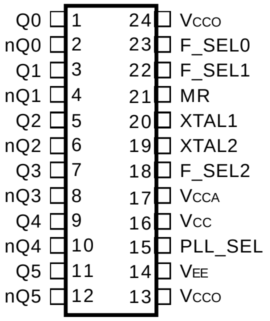
Offset	Noise Power
100Hz	-92 dBc/Hz
1KHz	-105 dBc/Hz
10KHz	-122 dBc/Hz
100KHz	-123 dBc/Hz

- Full 3.3V or 3.3V core, 2.5V output supply mode
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS84327
24-Lead, 300-MIL SOIC
7.5mm x 15.33mm x 2.3mm body package
M Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. LVPECL interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. LVPECL interface levels.
5, 6	Q2, nQ2	Output		Differential output pair. LVPECL interface levels.
7, 8	Q3, nQ3	Output		Differential output pair. LVPECL interface levels.
9, 10	Q4, nQ4	Output		Differential output pair. LVPECL interface levels.
11, 12	Q5, nQ5	Output		Differential output pair. LVPECL interface levels.
13, 24	V_{CCO}	Power		Output supply pins.
16	V_{CC}	Power		Core supply pin.
14	V_{EE}			Negative supply pin.
15	PLL_SEL	Input	Pullup	Selects between the PLL and crystal inputs as the input to the dividers. When HIGH, selects PLL. When LOW, selects XTAL1, XTAL2. LVCMOS / LVTTL interface levels.
17	V_{CCA}	Power		Analog supply pin.
18	F_SEL2	Input	Pullup	Feedback frequency select pin. LVCMOS/LVTTL interface levels.
19, 20	XTAL2, XTAL1	Input		Crystal oscillator interface. XTAL1 is the input. XTAL2 is the output.
21	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low, and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
22	F_SEL1	Input	Pulldown	Output frequency select pin. LVCMOS/LVTTL interface levels.
23	F_SEL0	Input	Pullup	Output frequency select pin. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	50°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current			140		mA
I_{CCA}	Analog Supply Current			20		mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, $V_{CC} = V_{CCA}$ = 3.3V±5%, V_{CCO} = 3.3V±5% OR 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	PLL_SEL, MR, F_SEL0, F_SEL1		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	PLL_SEL, MR, F_SEL0, F_SEL1		-0.3		0.8	V
I_{IH}	Input High Current	MR, F_SEL1	$V_{CC} = V_{IN}$ = 3.465V			150	µA
		PLL_SEL, F_SEL0	$V_{CC} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	MR, F_SEL1	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA
		PLL_SEL, F_SEL0	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA

TABLE 4C. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCA}$ = 3.3V±5%, V_{CCO} = 3.3V±5% OR 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 1.0	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.

TABLE 4D. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA}$ = 3.3V±5%, V_{CCO} = 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current			140		mA
I_{CCA}	Analog Supply Current			20		mA

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		19.44		25.5	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pf parallel resonant crystal.

TABLE 6A. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency		77.76		625	MHz
*t*sk(o)	Output Skew; NOTE 1, 2			30		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle			50		%
t_{LOCK}	PLL Lock Time				1	ms

See Parameter Measurement Information section.

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crossing points.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 6B. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V \pm 5\%$, $V_{CCO} = 2.5V \pm 5\%$, $T_A = 0°C$ TO $70°C$

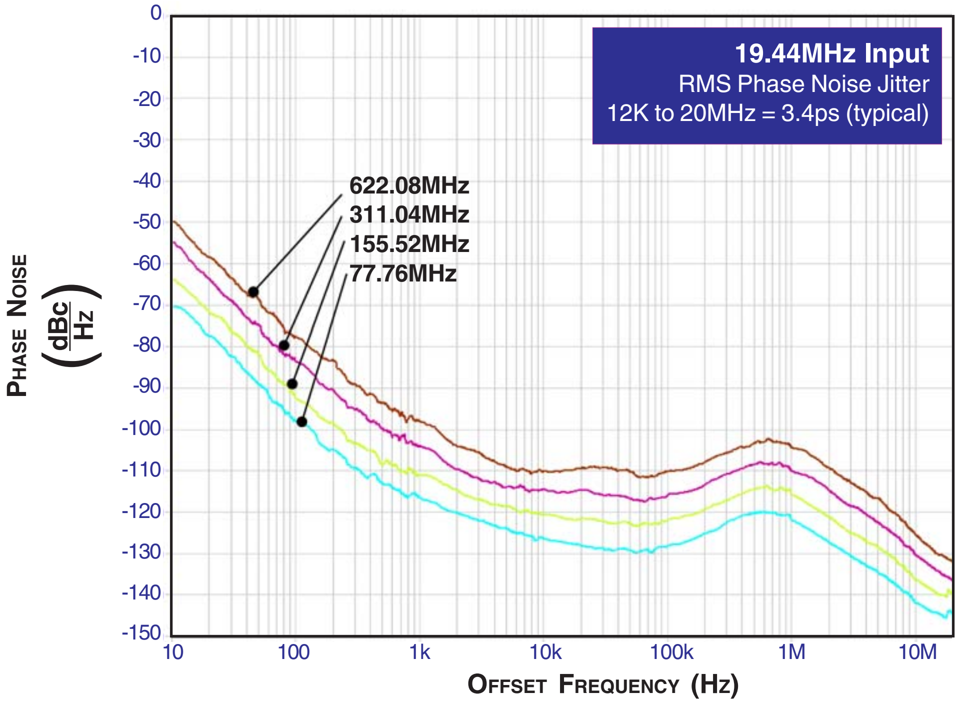
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency		77.76		625	MHz
*t*sk(o)	Output Skew; NOTE 1, 2			30		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle			50		%
t_{LOCK}	PLL Lock Time				1	ms

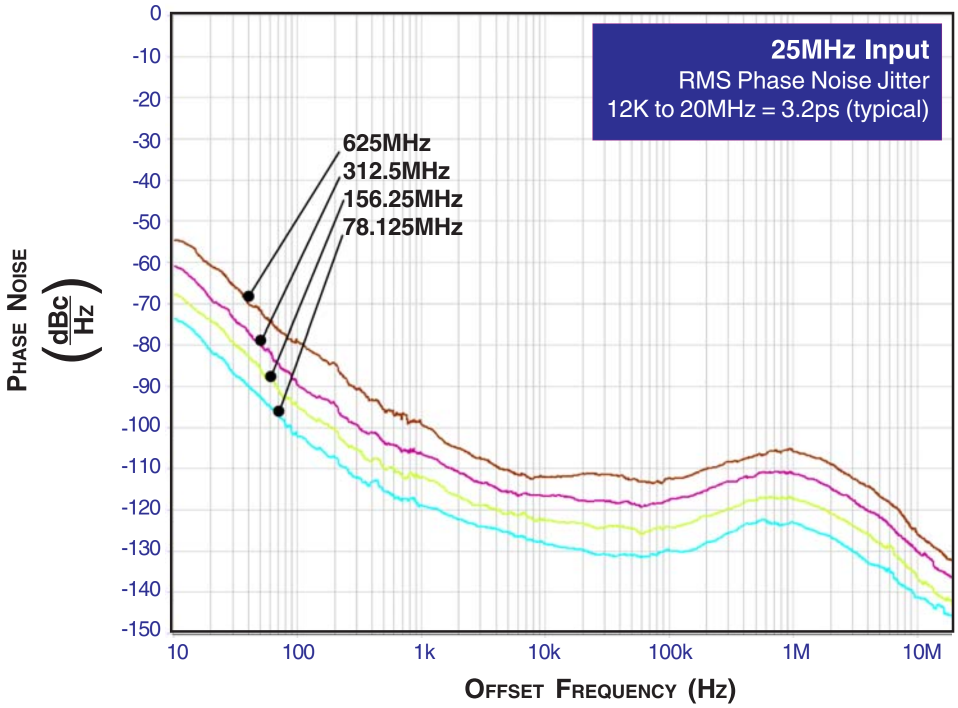
See Parameter Measurement Information section.

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crossing points.

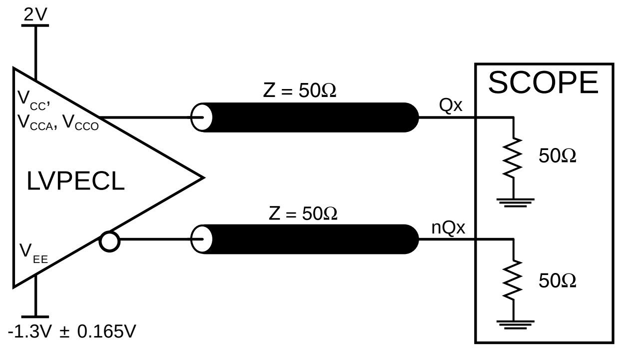
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

TYPICAL PHASE NOISE

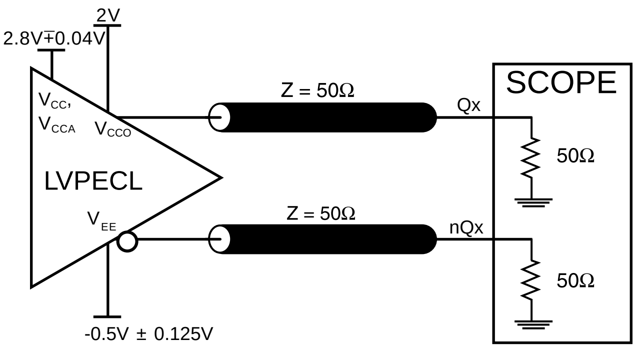




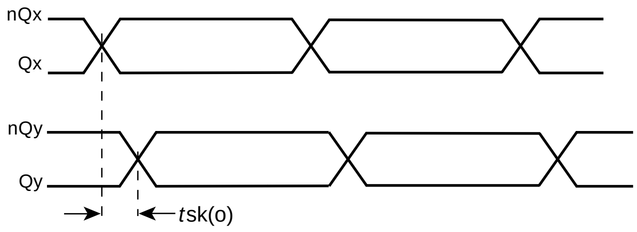
PARAMETER MEASUREMENT INFORMATION



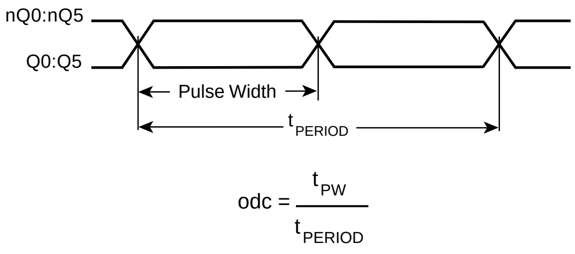
3.3V OUTPUT LOAD AC TEST CIRCUIT



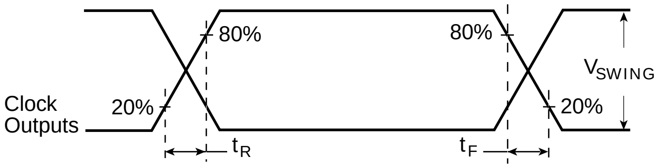
3.3V/2.5V OUTPUT LOAD AC TEST CIRCUIT



OUTPUT SKEW



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS84327 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA} and V_{CCO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA} pin.

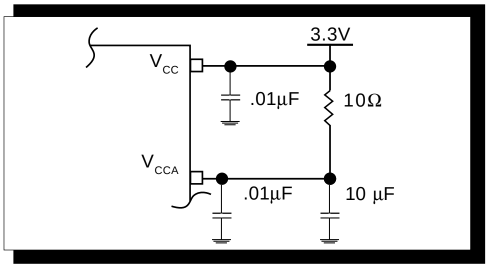


FIGURE 1. POWER SUPPLY FILTERING

TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

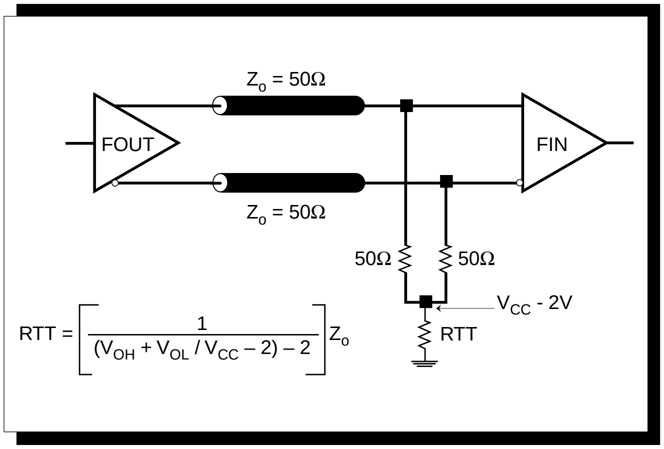


FIGURE 2A. LVPECL OUTPUT TERMINATION

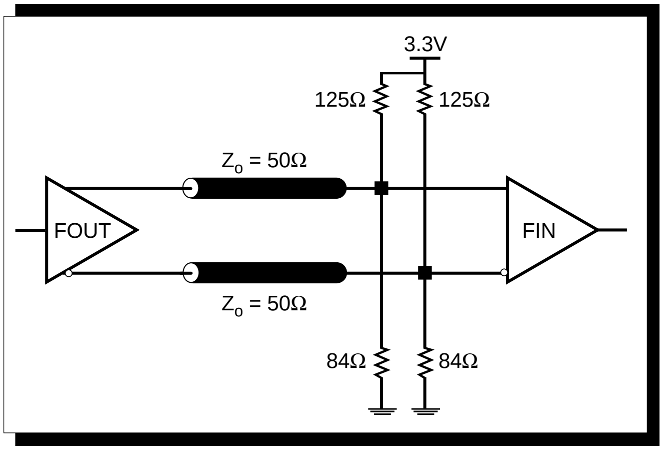


FIGURE 2B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 3A and *Figure 3B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 3B can be eliminated and the termination is shown in *Figure 3C.*

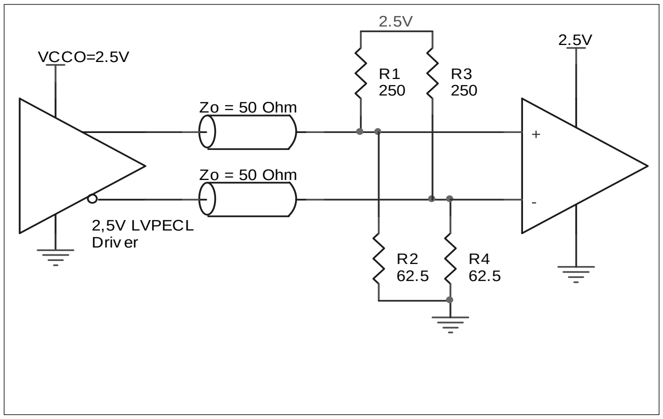


FIGURE 3A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

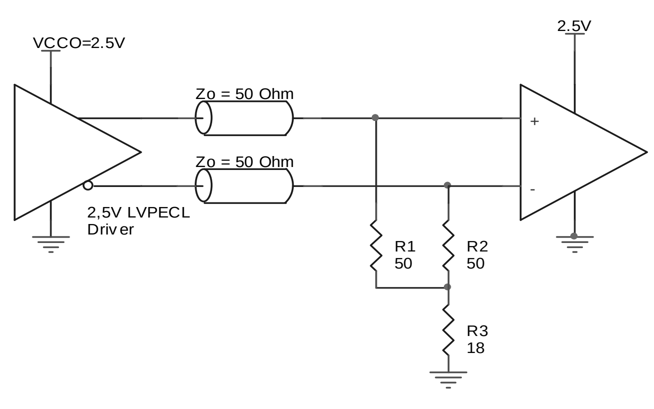


FIGURE 3B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

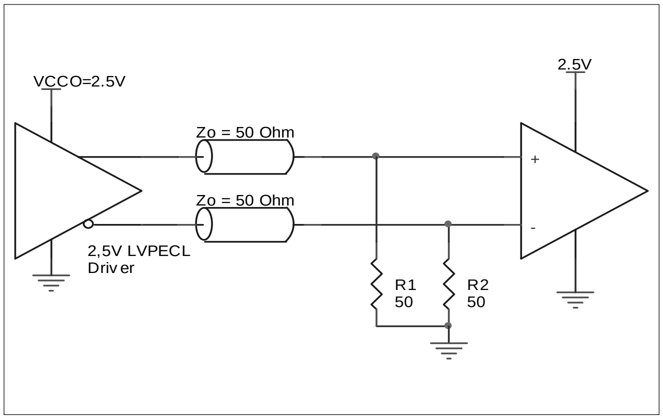


FIGURE 3C. 2.5V LVPECL TERMINATION EXAMPLE

CRYSTAL INPUT INTERFACE

The ICS84327 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 4* below were determined using a 25MHz 18pF parallel resonant crystal and were chosen to minimize the ppm error.

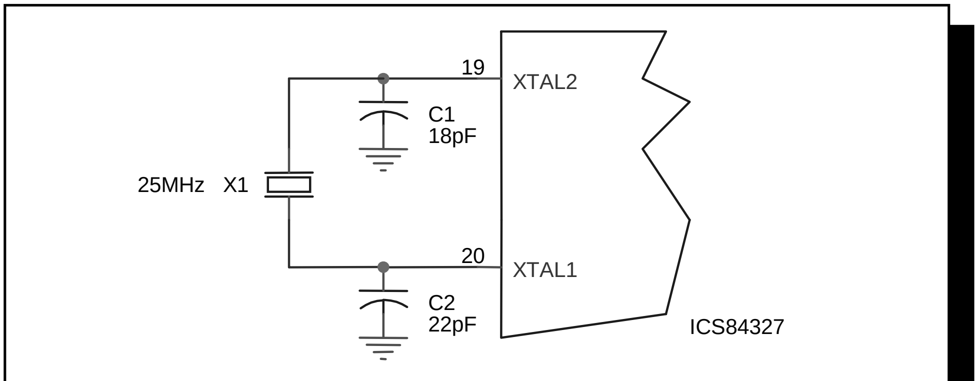


Figure 4. **CRYSTAL INPUT INTERFACE**

SCHEMATIC EXAMPLE

Figure 5A shows a schematic example of using an ICS84327. In this example, the input is a 25MHz parallel resonant crystal with load capacitor CL=18pF. The frequency fine tuning capacitors C1 and C2 is 22pF and 18pF respectively. This example also shows logic control input handling. The configuration is set at F_SEL[2:0]=011, therefore, the output frequency is 625MHz. It is recommended to have one decouple capacitor per power pin. Each decoupling capacitor should be located as close as possible to the power pin. The low pass filter R7, C11 and C16 for clean analog supply should also be located as close to the V_{CCA} pin as possible.

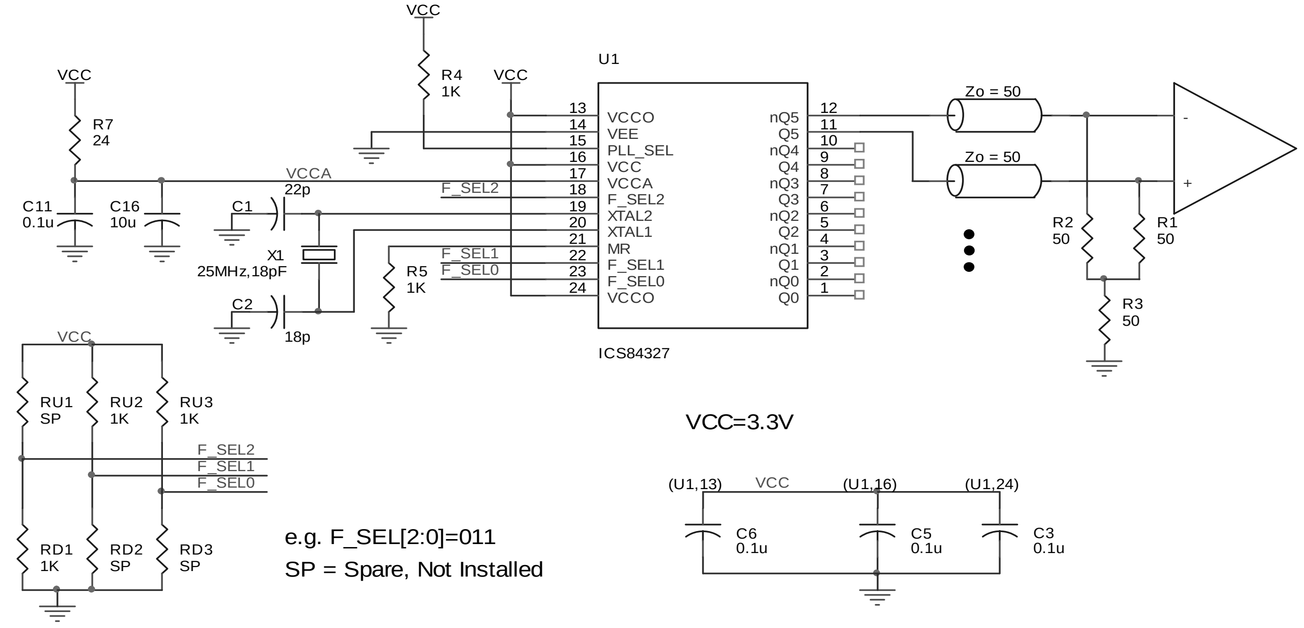


FIGURE 5A. ICS84327 SCHEMATIC EXAMPLE

The following component footprints are used in this layout example:

All the resistors and capacitors are size 0603.

POWER AND GROUNDING

Place the decoupling capacitors C3, C5 and C6, as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the V_{CCA} pin as possible.

CLOCK TRACES AND TERMINATION

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 50Ω output traces should have the same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.
- The matching termination resistors should be located as close to the receiver input pins as possible.

CRYSTAL

The crystal X1 should be located as close as possible to the pins 20 (XTAL1) and 19 (XTAL2). The trace length between the X1 and U1 should be kept to a minimum to avoid unwanted parasitic inductance and capacitance. Other signal traces should not be routed near the crystal traces.

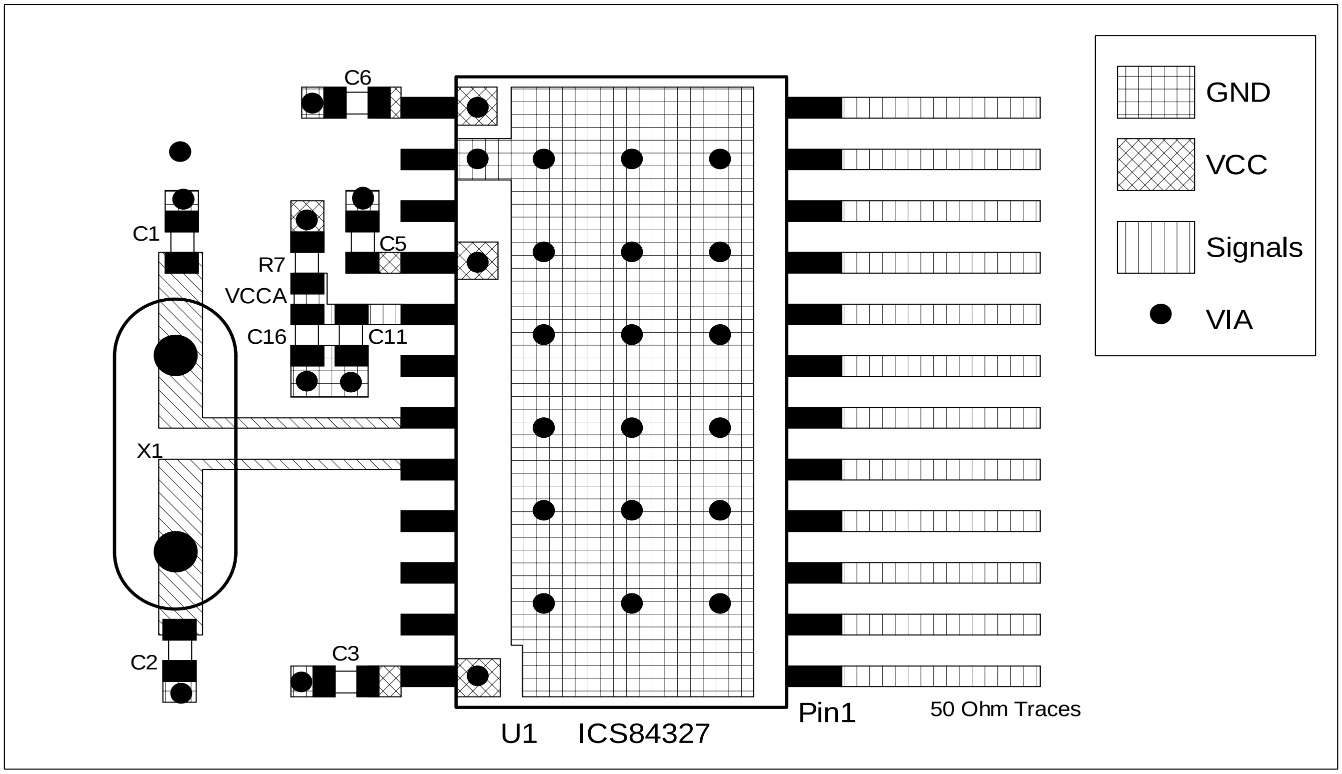


FIGURE 5B. PCB BOARD LAYOUT FOR ICS84327

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS84327.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS84327 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 140mA = 485**mW**
- Power (outputs)$_{MAX}$ = **30.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 6 * 30.2mW = **181mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 485mW + 181mW = **666mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS^{TM} devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 43°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.666W * 43°C/W = 98.6°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 24-PIN SOIC, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	50°C/W	43°C/W	38°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6.*

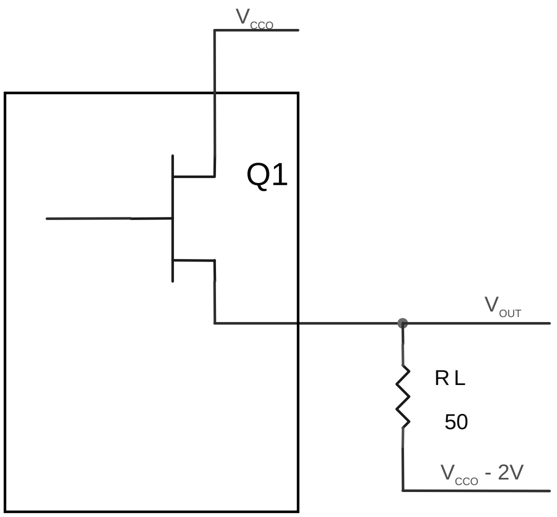


FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 1.0V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{1.0V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 1V)/50\Omega] * 1V = \mathbf{20.0mW}$

$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.2mW**

RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD SOIC

θ_{JA} by Velocity (Linear Feet per Minute)

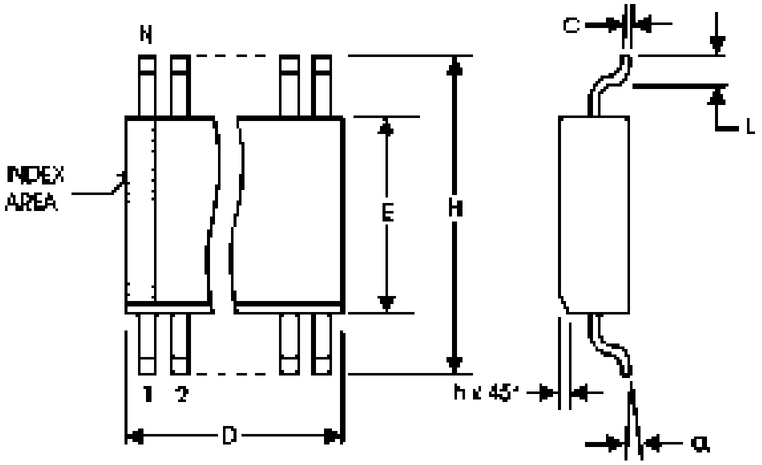
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	50°C/W	43°C/W	38°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS84327 is: 2804

PACKAGE OUTLINE - M SUFFIX FOR 24 LEAD SOIC



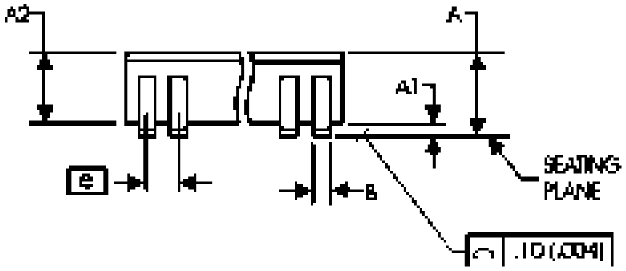


TABLE 9. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	2.65
A1	0.10	--
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	15.20	15.85
E	7.40	7.60
e	1.27 BASIC	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-013, MO-119

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS84327AM	ICS84327AM	24 Lead SOIC	30 per tube	0°C to 70°C
ICS84327AMT	ICS84327AM	24 Lead SOIC on Tape and Reel	1000	0°C to 70°C