Integrated Circuit Systems, Inc.

ICS9250-19

Frequency Generator & Integrated Buffers for Celeron & PII/III™

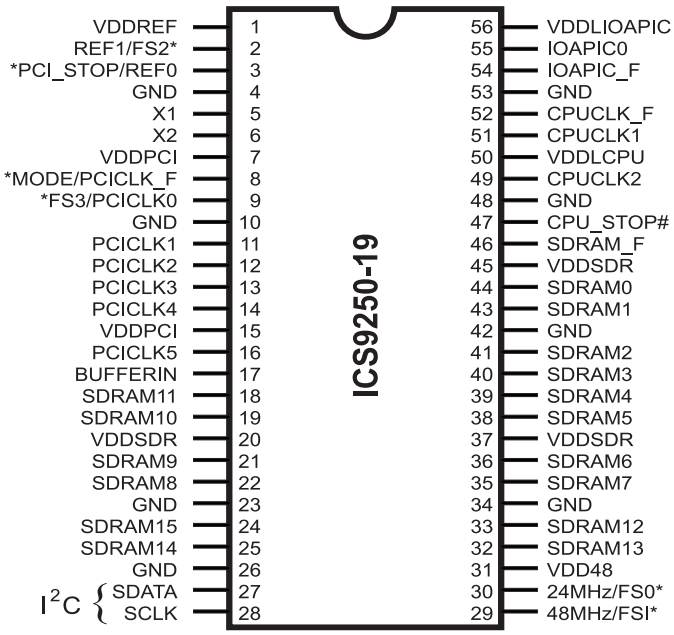
Recommended Application:
BX, Appollo Pro 133 type of chip set.

Output Features:
- 3 - CPUs @2.5V, up to 150MHz.
- 17 - SDRAM @ 3.3V, up to 150MHz.
- 7 - PCI @3.3V
- 2 - IOAPIC @ 2.5V
- 1 - 48MHz, @3.3V fixed.
- 1 - 24MHz @ 3.3V
- 2 - REF @3.3V, 14.318MHz.

Features:
- Up to 150MHz frequency support
- Support power management: CPU, PCI, stop and Power down Mode form I^2C programming.
- Spread spectrum for EMI control (0 to -0.5%, ± 0.25%).
- Uses external 14.318MHz crystal

Key Specifications:
- CPU – CPU: <175ps
- CPU – PCI: 1 - 4ns
- PCI – PCI: <500ps
- SDRAM - SDRAM: <250ps

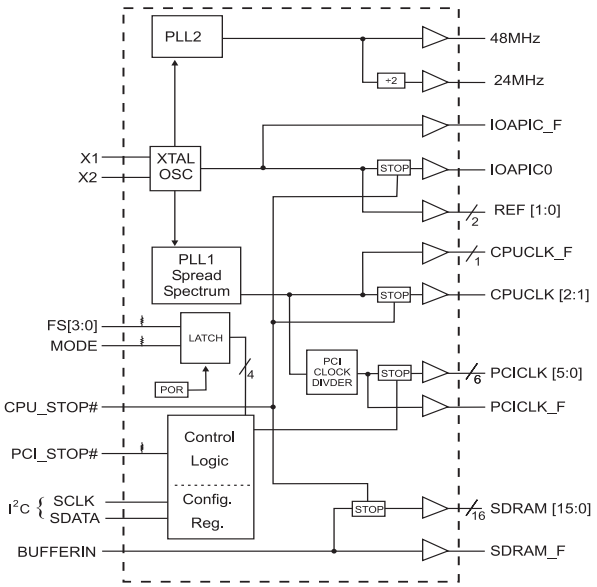
Pin Configuration



56-Pin SSOP

* Internal Pull-up Resistor of 240K to 3.3V on indicated inputs
** Internal Pull-down resistor of 240K to GND on indicated inputs.

Block Diagram



Functionality

FS3	FS2	FS1	FS0	CPU (MHz)	PCICLK (MHz)
1	1	1	1	133	33.3 (CPU/4)
1	1	1	0	124	31 (CPU/4)
1	1	0	1	150	37.5 (CPU/4)
1	1	0	0	140	35 (CPU/4)
1	0	1	1	105	35 (CPU/3)
1	0	1	0	110	36.67 (CPU/3)
1	0	0	1	115	38.33 (CPU/3)
1	0	0	0	120	40.00 (CPU/3)
0	1	1	1	100.0	33.43 (CPU/3)
0	1	1	0	133	44.33 (CPU/3)
0	1	0	1	112	37.33 (CPU/3)
0	1	0	0	103	34.33 (CPU/2)
0	0	1	1	66.6	33.40 (CPU/2)
0	0	1	0	83.3	41.65 (CPU/2)
0	0	0	1	75	37.5 (CPU/2)
0	0	0	0	124	41.33 (CPU/2)

Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
2	REF1	OUT	14.318 MHz reference clock output
	FS2[1]	IN	Latched frequency select input. Has pull-up to VDDPCI
3	REF0	OUT	14.318MHz reference clock output
	PCI_STOP#	IN	Halts PCICLK [5:1] at logic "0" level when low. (in mobile, MODE=0)
4, 10, 23, 26, 34, 42, 48, 53	GND	PWR	Ground.
5	X1	IN	14.318MHz input. Has internal load cap, (nominal 33pF).
6	X2	OUT	Crystal output. Has internal load cap (33pF) and feedback resistor to X1
8	PCICLK_F	OUT	Free running BUS clock not afected by PCI_STOP#
	MODE[1]	IN	Latched input for MODE select. Converts pin 3 to PCI_STOP# when low for power management.
9	FS3	IN	Latched frequency select input, pull-down
	PCICLK0	OUT	Free running BUS clock not afected by PCI_STOP#
16, 14, 13, 12, 11	PCICLK [5:1]	OUT	PCI Clock Outputs.
17	BUFFERIN	IN	Input for Buffers
27	SDATA	IN	Serial data in for serial config port. (I^2C)
28	SCLK	IN	Clock input for serial config port. (I^2C)
30	24MHz	OUT	24MHz clock output for Super I/O or FD.
	FS0[1]	IN	Latched frequency select input. Has pull-up to VDD4.
29	48MHz	OUT	48MHz clock output for USB.
	FS1[1]	IN	Latched frequency select input. Has pull-up to VDD2.
1, 7, 15, 20, 31, 37, 45	VDDPCI, VDDREF, VDDSDR, VDD48	PWR	Nominal 3.3V power supply, see power groups for function.
24, 25, 32, 33, 18, 19, 21, 22, 35, 36, 38, 39, 40, 41, 43, 44	SDRAM [15:0]	OUT	SDRAM clocks
46	SDRAM_F	OUT	Free running SDRAM clock Not affected by CPU_STOP#
47	CPU_STOP#	IN	Halts CPUCLK [2:1], IOAPIC0, SDRAM [15:0] clocks at logic "0" level when low.
50, 56	VDDLCPU, VDDLIOAPIC	PWR	CPU and IOAPIC clock buffer power supply, 2.5V nominal.
55	IOAPIC0	OUT	IOAPIC clock output. (14.318 MHz) Poweredby VDDL1
51, 49	CPUCLK [2:1]	OUT	CPU Output clocks. Powered by VDDL2 (60 or 66.6MHz)
52	CPUCLK_F	OUT	Free running CPU output clock. Not affected ty the CPU_STOP#.
54	IOAPIC_F	OUT	Freerunning IOAPIC clock output. Not affected by the CPU_STOP# (14.31818 MHz) Powered by VDDL1

Notes:

1: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.

General Description

The **ICS9250-19** is the single chip clock solution for Desktop/designs using BX, Appollo Pro 133 type of chip sets. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I^2C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9250-19 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial programming I^2C interface allows changing functions, stop clock programming and frequency selection.

Mode Pin - Power Management Input Control

MODE (Latched Input)	
0	PCI_STOP# (Input)
1	REF0 (Output)

General I^2C serial interface information

The information in this section assumes familiarity with I^2C programming.
For more information, contact ICS for an I^2C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 5***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I^2C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I^2C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Description			PWD
Bit 7	0 = 0 to -0.5% Down Spread Spectrum Modulation 1 = ±0.25% Center Spread Spectrum Modulation			0
	Bit2 Bit6 Bit5 Bit4	CPU clock	PCI	
Bit 2, Bit 6:4	0111	100.0	33.43 (CPU/3)	Note1
	0110	133	44.33 (CPU/3)	
	0101	112	37.33 (CPU/3)	
	0100	103	34.3 (CPU/3)	
	0011	66.6	33.4 (CPU/2)	
	0010	83.3	41.65(CPU/2)	
	0001	75	37.5 (CPU/2)	
	0000	124	41.33 (CPU/3)	
	1111	133	33.25 (CPU/4)	
	1110	124	31.00 (CPU/4)	
	1101	150	37.50 (CPU/4)	
	1100	140	35.00 (CPU/4)	
	1011	105	35.00 (CPU/3)	
	1010	110	36.67 (CPU/3)	
	1001	115	38.33 (CPU/3)	
	1000	120	40.00 (CPU/3)	
Bit 3	0 - Frequency is selected by hardware select, Latched Inputs 1 - Frequency is selected by Bit 6:4 (above)			0
Bit 1	0 - Normal 1 - Spread Spectrum Enabled (Center Spread)			1
Bit 0	0 - Running 1- Tristate all outputs			0

Note 1. Default at Power-up will be for latched logic inputs to define frequency. Bits 4, 5, 6 are default to 000, and if bit 3 is written to a 1 to use Bits 6:4, then these should be defined to desired frequency at same write cycle.

Note: PWD = Power-Up Default

Byte 1: CPU, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	46	1	SDRAM_F (Act/Inact)
Bit 2	49	1	CPUCLK2 (Act/Inact)
Bit 1	51	1	CPUCLK1 (Act/Inact)
Bit 0	52	1	CPUCLK_F (Act/Inact)

Byte 2: PCI, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	8	1	PCICLKF (Act/Inact)
Bit 5	16	1	PCICLK5 (Act/Inact)
Bit 4	14	1	PCICLK4 (Act/Inact)
Bit 3	13	1	PCICLK3 (Act/Inact)
Bit 2	12	1	PCICLK2 (Act/Inact)
Bit 1	11	1	PCICLK1 (Act/Inact)
Bit 0	9	1	PCICLK0 (Act/Inact)

Byte 3: SDRAM, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	29	1	48MHz (Act/Inact)
Bit 4	30	1	24MHz (Act/Inact)
Bit 3	33, 32, 25, 24	1	SDRAM(12:15) (Act/Inact)
Bit 2	22, 21, 19, 18	1	SDRAM (8:11) (Act/Inact)
Bit 1	39, 38, 36, 35	1	SDRAM (4:7) (Act/Inact)
Bit 0	44, 43, 41, 40	1	SDRAM (0:3) (Act/Inact)

Byte 4: Reserved , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	Latched FS0#
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	X	Latched FS1#
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	X	Latched FS3#
Bit 0	-	1	Reserved

Byte 5: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	X	Latched FS2#
Bit 5	54	1	IOAPIC_F (Act/Inact)
Bit 4	55	1	IOAPIC0 (Act/Inact)
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	2	1	REF1 (Act/Inact)
Bit 0	3	1	REF0 (Act/Inact)

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inferted logic load of the input frequency select pin conditions.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the **ICS9250-19** serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 4-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm(10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figs. 1 and 2 show the recommended means of implementing this function. In Fig. 1 either one of the resistors is loaded onto the board (selective stuffing) to configure the device's internal logic. Figs. 2a and b provide a single resistor loading option where either solder spot tabs or a physical jumper header may be used.

These figures illustrate the optimal PCB physical layout options. These configuration resistors are of such a large ohmic value that they do not effect the low impedance clock signals. The layouts have been optimized to provide as little impedance transition to the clock signal as possible, as it passes through the programming resistor pad(s).

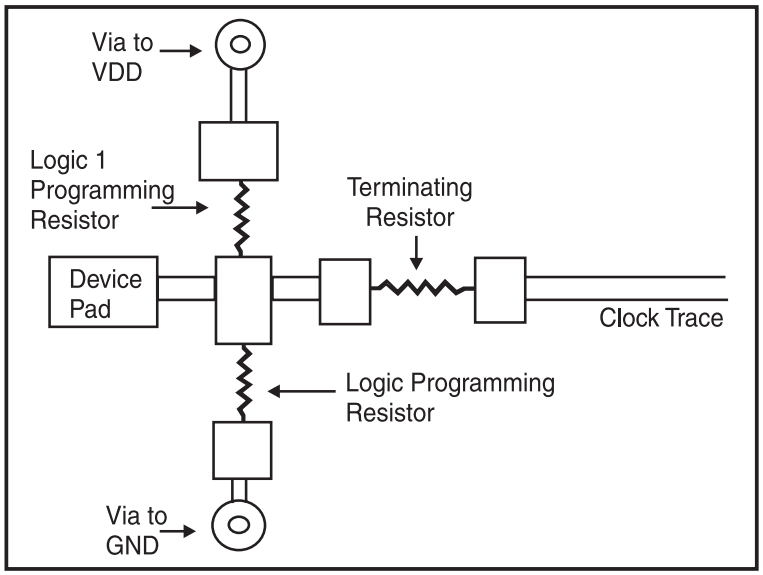


Fig. 1

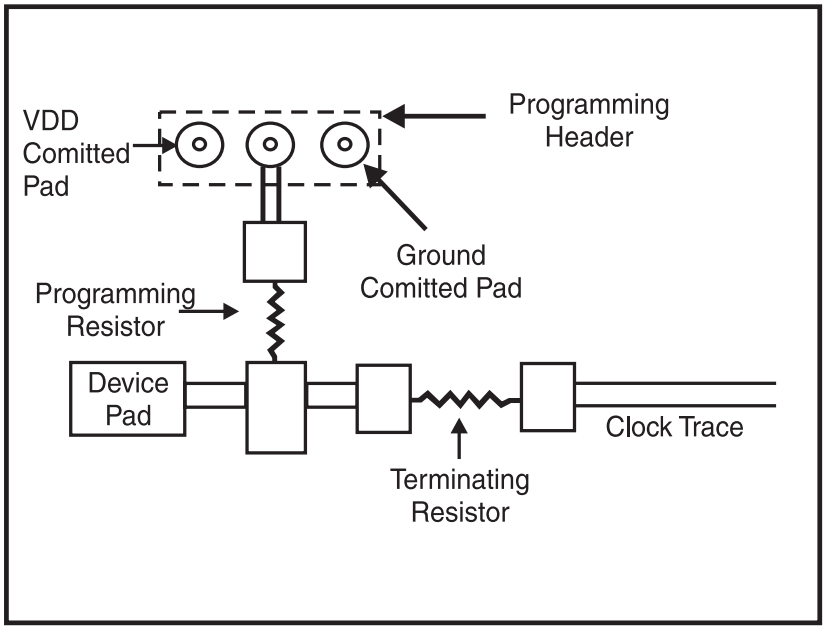


Fig. 2a

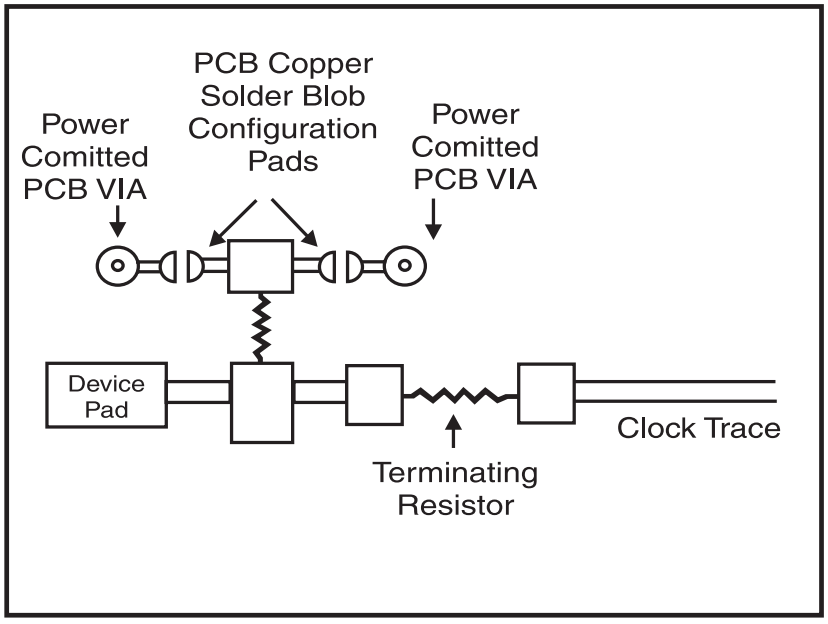
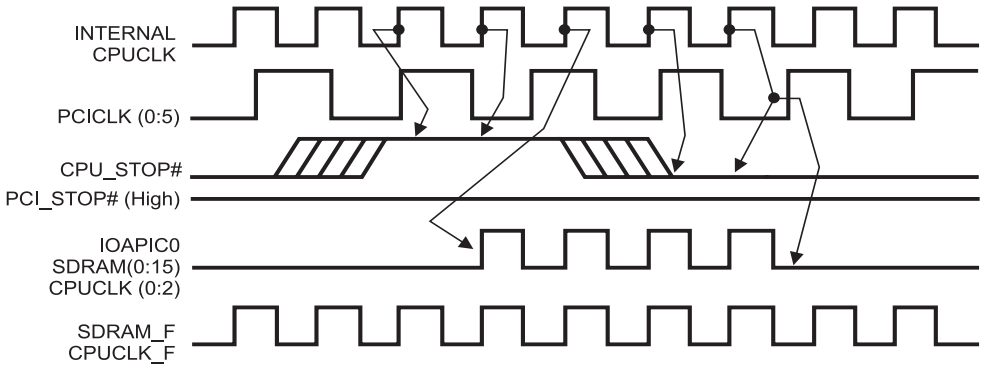


Fig. 2b

CPU_STOP# Timing Diagram

CPUSTOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPUCLKs for low power operation. CPU_STOP# is synchronized by the **ICS9250-19**. All other clocks will continue to run while the CPUCLKs are disabled. The CPUCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPUCLK on latency is less than 4 CPUCLKs and CPUCLK off latency is less than 4 CPUCLKs.

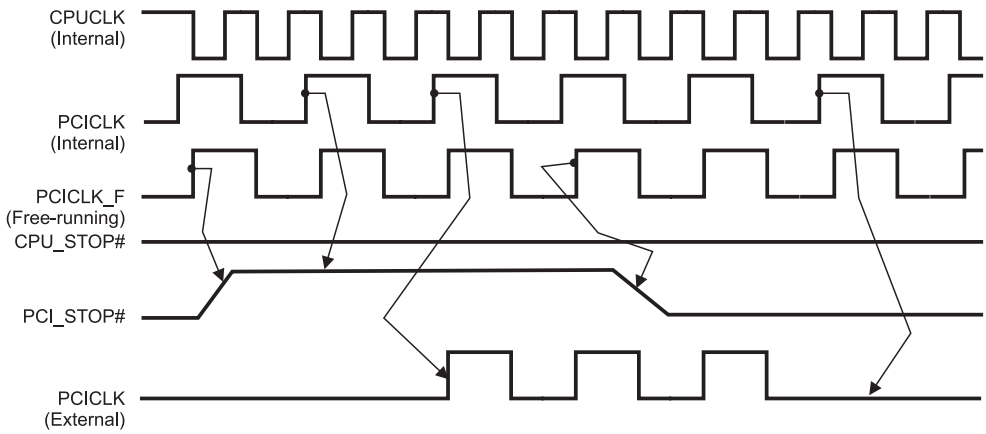


Notes:

1. All timing is referenced to the internal CPUCLK.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the **ICS9250-19.**
3. IOAPIC output is stopped Glitch Free by CPUSTOP# going low.
4. PCI_STOP# is shown in a high (true) state.
5. All other clocks continue to run undisturbed.

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9250-19**. It is used to turn off the PCICLK (0:5) clocks for low power operation. PCI_STOP# is synchronized by the **ICS9250-19** internally. PCICLK (0:5) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK (0:5) clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the device.
3. All other clocks continue to run undisturbed.
4. CPU_STOP# is shown in a high (true) state.

Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Case Temperature . . . . . 115°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70º C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$		0.1	5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5	2.0		µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200	-100		µA
Operating Supply Current	$I_{DD3.3OP100}$	Select @ 100MHz; Sdram running		150	180	mA
	$I_{DD3.3OP133}$	Select @ 133MHz; Sdram running		200	n/a	
Input frequency	F_i	V_{DD} = 3.3 V	12	14.318	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition Time[1]	T_{Trans}	To 1st crossing of target Freq.			4	ms
Settling Time[1]	T_S	From 1st crossing to 1% target Freq.		1	3	ms
Clk Stabilization[1]	T_{Stab}	From V_{DD} = 3.3 V to 1% target Freq.			4	ms

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70º C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	$I_{DD2.5OP100}$	Select @ 100MHz; Max discrete cap loads		13	25	mA
	$I_{DD2.5OP133}$	Select @ 133MHz; Max discrete cap loads		18	25	

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLK

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	I_{OH} = -12.0 mA	2	2.3		V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA		0.2	0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V		-41	-19	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19	37		mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4		1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4	1	1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45	51	55	%
Skew group1: 1,2 and 1,F	t_{sk2B}[1]	V_T = 1.25 V		120	175	ps
Skew group2: 2, F	t_{sk2B}[1]	V_T = 1.25 V			295	ps
Jitter, One Sigma	$t_{j1\sigma 2B}$[1]	V_T = 1.25 V		120	250	ps
Jitter, Absolute	t_{jabs2B}[1]	V_T = 1.25 V	-250	100	+250	ps
Jitter, Cycle-to-cycle	$t_{jcyc-cyc2B}$[1]	V_T = 1.25 V		150	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 48MHz, 24MHz,REF0

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -14 mA	2.4	2.9		V
Output Low Voltage	V_{OL5}	I_{OL} = 6.0 mA		0.25	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-42	-20	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	10	18		mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.1	2.5	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1	2.5	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	50	55	%
Jitter[1]	t_{j1s5}	V_T = 1.5 V, 24, 48MHz		100	250	ps
Jitter[1]	t_{jabs5}	V_T = 1.5 V, REF0		250	800	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

T_A = 0 - 70° C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 60 pF for PCI0 & PCI1, CL = 30 pF for other PCIs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -18 mA	2.4	2.9		V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA		0.2	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-58	-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	25	52		mA
Rise Time[1]	t_{r1}	V_{OL} = 0.8 V, V_{OH} = 2.4 V		1.5	2.5	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.4	2.5	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	50	55	%
Skew[1]	t_{sk1}	V_T = 1.5 V		270	500	ps
Jitter, One Sigma[1]	$t_{j1\sigma1}$	V_T = 1.5 V		50	150	ps
Jitter, Absolute[1]	t_{jabs1}	V_T = 1.5 V		200	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70° C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L =30 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -28 mA	2.4	2.8		V
Output Low Voltage	V_{OL1}	I_{OL} = 19 mA		0.34	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-72	-42	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	33	50		mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 04 V	0.5		2.4	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	50	55	%
Skew(Group1: F,0:4, 8:11)[1]	t_{sk1}	V_T = 1.5 V		130	250	ps
Skew(Group2: 5, 7, 12:15)[1]	t_{sk1}	V_T = 1.5 V		180	250	ps
Skew(Group3: 0, 13)[1]	t_{sk1}	V_T = 1.5 V			490	ps
Skew(Group4: 6, 13)[1]	t_{sk1}	V_T = 1.5 V			910	ps
Skew(Buferin-Output)[1]	t_{sk1}	V_T = 1.5 V		3.5	4.4	ns
Jitter, One Sigma[1]	$t_{j1\sigma1}$	V_T = 1.5 V		50	150	ps
Jitter, Absolute[1]	t_{jabs1}	V_T = 1.5 V	-250	130	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH4B}	I_{OH} = -12 mA	2	2.2		V
Output Low Voltage	V_{OL4B}	I_{OL} = 12 mA		0.3	0.4	V
Output High Current	I_{OH4B}	V_{OH} = 1.7 V		-32	-19	mA
Output Low Current	I_{OL4B}	V_{OL} = 0.7 V	19	26		mA
Rise Time[1]	T_{r4B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4	1.5	1.8	ns
Fall Time[1]	T_{f4B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4	1	1.6	ns
Duty Cycle[1]	D_{t4B}	V_T = 1.25 V	45	51	55	%
Jitter, One Sigma[1]	$T_{j1\sigma4B}$	V_T = 1.25 V		240	300	ps
Jitter, Absolute[1]	T_{jabs4B}	V_T = 1.25 V		619	650	ps

[1]Guaranteed by design, not 100% tested in production.

General Layout Precautions:

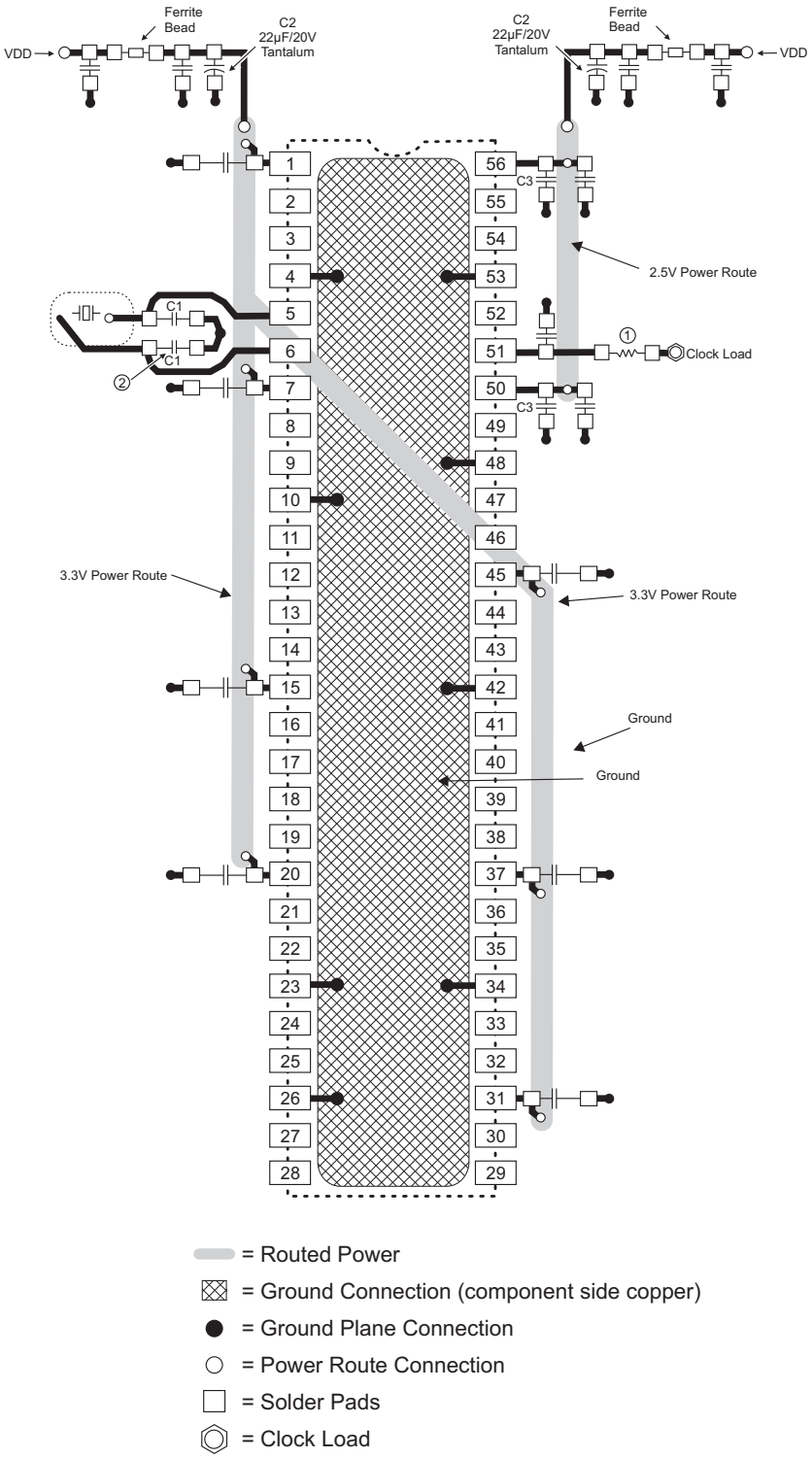
1) Use a ground plane on the top layer of the PCB in all areas not used by traces.

2) Make all power traces and ground traces as wide as the via pad for lower inductance.

Notes:

1) All clock outputs should have a series terminating resistor, and a 20pF capacitor to ground between the resistor and clock pin. Not shown in all places to improve readibility of diagram.

2) Optional crystal load capacitors are recommended. They should be included in the layout but not inserted unless needed.



Component Values:

C1 : Crystal load values determined by user

C2 : 22□F/20V/D case/Tantalum
AVX TAJD226M020R

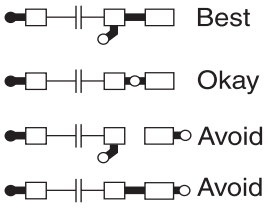
C3 : 100pF ceramic capacitor

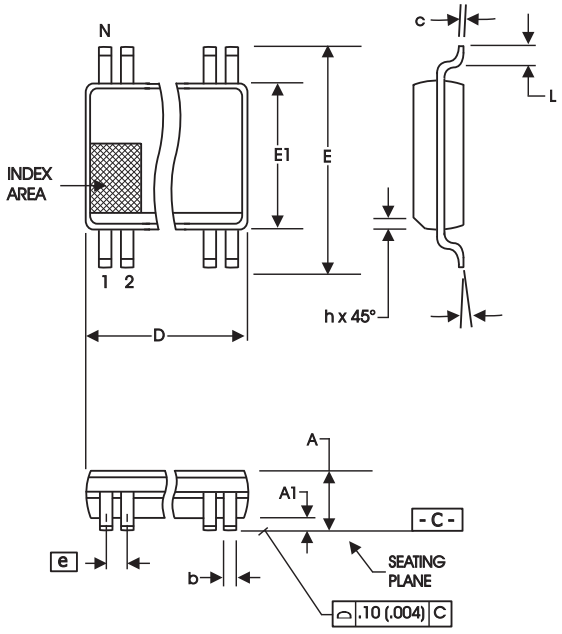
C4 : 20pF capacitor

FB = Fair-Rite products 2512066017X1

All unmarked capacitors are 0.01□F ceramic

Connections to VDD:





300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.31	18.55	.720	.730

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS9250yF-19

Example:

ICS XXXX y F - PPP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
F=SSOP

Revision Designator (will not correlate with datasheet revision)

Device Type

Prefix
ICS, AV = Standard Device