



## DDR Phase Lock Loop Zero Delay Clock Buffer

**Recommended Application:**  
DDR Zero Delay Clock Buffer

**Product Description/Features:**

- Low skew, low jitter PLL clock driver
- Max frequency supported = 266MHz (DDR 533)
- I<sup>2</sup>C for functional and output control
- Feedback pins for input to output synchronization
- Spread Spectrum tolerant inputs
- 3.3V tolerant CLK\_INT input

**Switching Characteristics:**

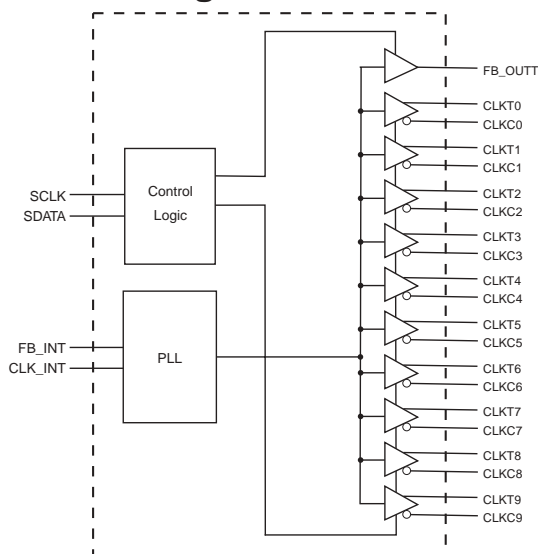
- CYCLE - CYCLE jitter (66MHz): <120ps
- CYCLE - CYCLE jitter (>100MHz): <65ps
- CYCLE - CYCLE jitter (>200MHz): <75ps
- OUTPUT - OUTPUT skew: <100ps
- Output Rise and Fall Time: 500ps - 700ps
- DUTY CYCLE: 49.5% - 50.5%

### Functionality

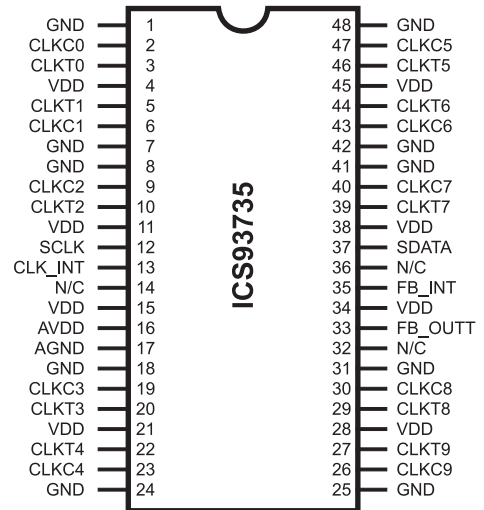
INPUTS		OUTPUTS			PLL State
AVDD	CLK_INT	CLKT	CLKC	FB_OUTT	
2.5V (nom)	L	L	H	L	on
2.5V (nom)	H	H	L	H	on
2.5V (nom)	< offset freq*	offset freq*	offset freq*	offset freq*	off
GND	L	L	H	L	Bypassed/off
GND	H	H	L	H	Bypassed/off

\* The offset frequency is ~ 20 MHz, varying somewhat from part to part.

### Block Diagram



### Pin Configuration



**48-Pin SSOP**



## Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 7, 8, 18, 24, 25, 31, 41, 42, 48	GND	PWR	Ground
26, 30, 40, 43, 47, 23, 19, 9, 6, 2	CLKC(9:0)	OUT	"Complementary" clocks of differential pair outputs.
27, 29, 39, 44, 46, 22, 20, 10, 5, 3	CLKT(9:0)	OUT	"True" Clock of differential pair outputs.
4, 11, 15, 21, 28, 34, 38, 45,	VDD	PWR	Power supply 2.5V
12	SCLK	IN	Clock input of I <sup>2</sup> C input, 5V tolerant input
13	CLK_INT	IN	"True" reference clock input, 3.3V tolerant input
14, 32, 36	N/C	-	Not connected
16	AVDD	PWR	Analog power supply, 2.5V
17	AGND	PWR	Analog ground.
33	FB_OUTT	OUT	"True" " Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INT.
35	FB_INT	IN	"True" Feedback input, provides feedback signal to the internal PLL for synchronization with CLK_INT to eliminate phase error.
37	SDATA	I/O	Data pin for I <sup>2</sup> C circuitry 5V tolerant

### Byte 0: Output Control (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

### Byte 1: Output Control (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved



**Byte 2: Reserved**  
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

**Byte 3: Reserved**  
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

**Byte 4: Reserved**  
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

**Byte 5: Reserved**  
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	3,2	1	CLK0 (T&C)
Bit6	5,6	1	CLK1 (T&C)
Bit5	10, 9	1	CLK2 (T&C)
Bit4	20, 19	1	CLK3 (T&C)
Bit3	22, 23	1	CLK4 (T&C)
Bit2	27, 26	1	CLK9 (T&C)
Bit1	-	1	Reserved
Bit0	-	1	Reserved

**Byte 6: Reserved**  
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Reserved (Note)
Bit6	-	0	Reserved (Note)
Bit5	-	0	Reserved (Note)
Bit4	29, 30	1	CLK8 (T&C)
Bit3	39, 40	1	CLK7 (T&C)
Bit2	44, 43	1	CLK6 (T&C)
Bit1	46, 47	1	CLK5 (T&C)
Bit0	-	1	Reserved

**Note:** Don't write into these registers (7:5), writing into these registers can cause malfunction.



## General I<sup>2</sup>C serial interface information

The information in this section assumes familiarity with I<sup>2</sup>C programming. For more information, contact ICS for an I<sup>2</sup>C programming application note.

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D4<sub>(H)</sub>
- ICS clock will *acknowledge*
- Controller (host) sends a dummy command code
- ICS clock will *acknowledge*
- Controller (host) sends a dummy byte count
- ICS clock will *acknowledge*
- Controller (host) starts sending first byte (Byte 0) through byte 6
- ICS clock will *acknowledge* each byte *one at a time*.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D4 <sub>(H)</sub>	
	<b>ACK</b>
Dummy Command Code	
	<b>ACK</b>
Dummy Byte Count	
	<b>ACK</b>
Byte 0	
	<b>ACK</b>
Byte 1	
	<b>ACK</b>
Byte 2	
	<b>ACK</b>
Byte 3	
	<b>ACK</b>
Byte 4	
	<b>ACK</b>
Byte 5	
	<b>ACK</b>
Byte 6	
	<b>ACK</b>
Stop Bit	

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D5<sub>(H)</sub>
- ICS clock will *acknowledge*
- ICS clock will send the *byte count*
- Controller (host) acknowledges
- ICS clock sends first byte (**Byte 0**) through **byte 6**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D5 <sub>(H)</sub>	
	<b>ACK</b>
	<b>Byte Count</b>
ACK	
	<b>Byte 0</b>
ACK	
	<b>Byte 1</b>
ACK	
	<b>Byte 2</b>
ACK	
	<b>Byte 3</b>
ACK	
	<b>Byte 4</b>
ACK	
	<b>Byte 5</b>
ACK	
	<b>Byte 6</b>
ACK	
Stop Bit	

### Notes:

1. The ICS clock generator is a slave/receiver, I<sup>2</sup>C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol.**
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I<sup>2</sup>C interface, the protocol is set to use only **"Block-Writes"** from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.



### Absolute Maximum Ratings

- Supply Voltage (VDD & AVDD) . . . . . -0.5V to 3.6V
- Logic Inputs . . . . . GND -0.5 V to VDD +0.5 V
- Ambient Operating Temperature . . . . . 0°C to +85°C
- Storage Temperature . . . . . -65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

### Electrical Characteristics - Input / Supply / Common Output parameters

T<sub>A</sub> = 0 - 70°C; Supply Voltage AV<sub>DD</sub>, V<sub>DD</sub> = 2.50V ± 0.20V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	I <sub>DD2.5</sub>	R <sub>T</sub> = 120W, C <sub>L</sub> = 12 pF at 100MHz		236	300	mA
		R <sub>T</sub> = 120W, C <sub>L</sub> = 12 pF at 133MHz		263	300	
	I <sub>DDPD</sub>	CL=0 pF			100	mA
Output High Current	I <sub>OH</sub>	V <sub>DD</sub> = 2.5V, V <sub>OUT</sub> = 1V	-48	-33	-29	mA
Output Low Current	I <sub>OL</sub>	V <sub>DD</sub> = 2.5V, V <sub>OUT</sub> = 1.2V	29	33	37	mA
High Impedance Output Current	I <sub>OZ</sub>	V <sub>DD</sub> = 2.7V, V <sub>OUT</sub> = V <sub>DD</sub> or GND			10	mA
High-level Output Voltage	V <sub>OH</sub>	V <sub>DD</sub> = min to max, I <sub>OH</sub> = -1mA	2	2.25		V
		V <sub>DD</sub> = 2.3V, I <sub>OH</sub> = -12mA		1.95		
Low-level Output Voltage	V <sub>OL</sub>	V <sub>DD</sub> = min to max, I <sub>OH</sub> = 1mA		0.05	0.1	V
		V <sub>DD</sub> = 2.3V, I <sub>OH</sub> = 12mA		0.3	0.4	
Output Capacitance <sup>1</sup>	C <sub>OUT</sub>	V <sub>I</sub> = V <sub>DD</sub> or GND		3		pF

1. Guaranteed by design, not 100% tested in production.



### Recommended Operation Conditions

T<sub>A</sub> = 0 - 70°C; Supply Voltage AV<sub>DD</sub>, V<sub>DD</sub> = 2.50V ± 0.20V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog / Core Supply Voltage	AV <sub>DD</sub>		2.3	2.5	2.7	V
Input Voltage Level	V <sub>IN</sub>		2	2.5	3	V
Output Differential Pair Crossing Voltage	V <sub>OC</sub>	66/100/133/166MHz, V <sub>DD</sub> =2.50V	1.23	1.25	1.32	V

### Timing Requirements

T<sub>A</sub> = 0 - 70°C; Supply Voltage AV<sub>DD</sub>, V<sub>DD</sub> = 2.50V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Clock Frequency	freq <sub>op</sub>	Input Voltage level: 0-2.50V	22		340	MHz
Input Clock Duty Cycle <sup>1</sup>	d <sub>tin</sub>		40	50	60	%
Clock Stabilization <sup>1</sup>	t <sub>STAB</sub>	from VDD = 2.5V to 1% target frequency			100	μs

1. Guaranteed by design, not 100% tested in production.

### Switching Characteristics

T<sub>A</sub> = 0 - 70°C; Supply Voltage AV<sub>DD</sub>, V<sub>DD</sub> = 2.50V ± 0.20V (unless otherwise stated)

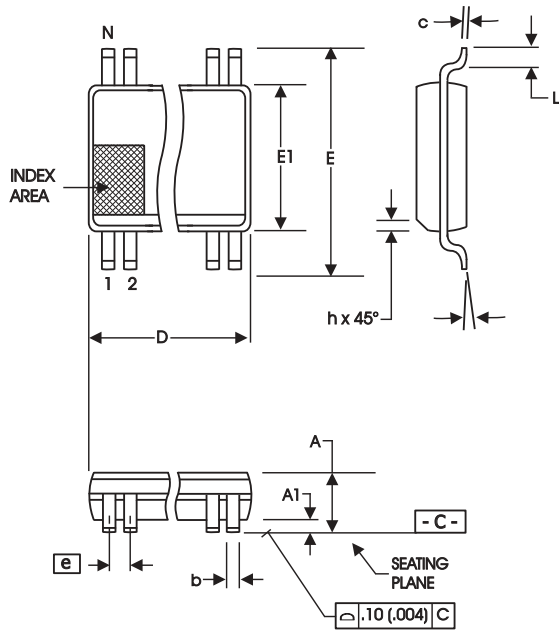
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Cycle to cycle Jitter <sup>1,2</sup>	t <sub>c-c</sub>	66 MHz	46	52	63	ps
		100 / 125 / 133 MHz	27	33	40	
Phase Error <sup>1</sup>	t <sub>pe</sub>	100MHz, input clock 0-2.5V, 0.8ns rise/fall		-113		ps
Output to output Skew <sup>1</sup>	T <sub>skew</sub>	input clock 0-2.5V, 0.8ns rise/fall	66		98	ps
Low-to-high level Propagation Delay Time, Bypass Mode <sup>1</sup>	t <sub>PLH</sub>	CLK_IN to any output, 100MHz, Load = 120 W / 12 pF	3.67		3.68	ns
Pulse Skew <sup>1</sup>	T <sub>skew</sub>					ps
Duty Cycle (Sign Ended) <sup>1,3</sup>	DC	no loads, 66 MHz to 167MHz	50.2		51.3	%
Rise Time <sup>1</sup>	t <sub>R</sub>	Single-ended 20-80 %; Load=120W/12pF	400	490	622	ps
Fall Time <sup>1</sup>	t <sub>F</sub>	Single-ended 20-80 %; Load=120W/12pF	435	579	711	ps

1. Guaranteed by design, not 100% tested in production.

2. Refers to transition on non-inverting period.

3. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies.

This is due to the formular: duty\_cycle=t<sub>wh</sub>/t<sub>c</sub>, where the cycle time (t<sub>c</sub>)decreases as the frequency increases.



300 mil SSOP Package

SYMBOL	In Millimeters		In Inches	
	COMMON DIMENSIONS	COMMON DIMENSIONS	COMMON DIMENSIONS	COMMON DIMENSIONS
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118  
10-0034

Ordering Information

ICS93735yF-T

Example:

ICS XXXX y F - PPP - T

