Integrated Circuit Systems, Inc.

ICS950104

Advance Information

Programmable System Clock Chip for PIII™ Processor

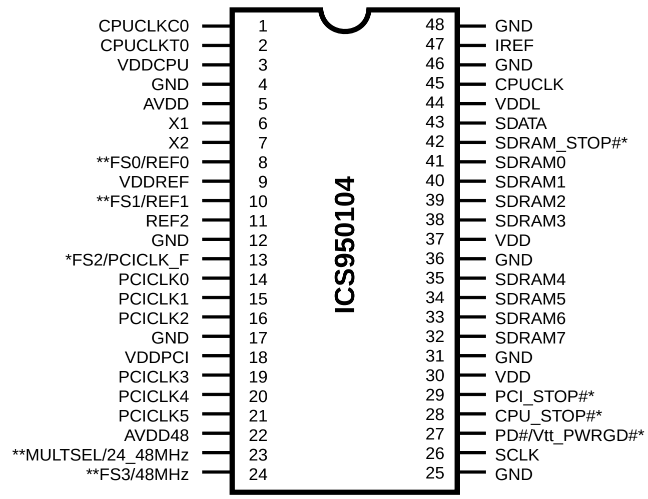
Recommended Application:
SIS630ST style chipset

Output Features:
- 1 - CPU clocks @ 2.5V
- 1 - Pair of differential CPU clocks @ 3.3V
- 9 - SDRAM @ 3.3V
- 7 - PCI @3.3V
- 1 - 48MHz, @3.3V
- 1 - 24/48MHz @ 3.3V
- 3 - REF @3.3V, (selectable strength) through I^2C

Features:
- Programmable ouput frequency
- Programmable ouput rise/fall time
- Programmable CPU, SDRAM, and PCI skew
- Real time system reset output
- Spread spectrum for EMI control typically by 7dB to 8dB, with programmable spread percentage
- Watchdog timer technology to reset system if over-clocking causes malfunction
- Uses external 14.318MHz crystal

Skew Specifications:
- CPU - CPU: <250ps
- PCI - PCI: <500ps
- SDRAM - SDRAM: <250ps
- CPU - SDRAM:<350ps
- CPU - PCI: <3ns

Pin Configuration

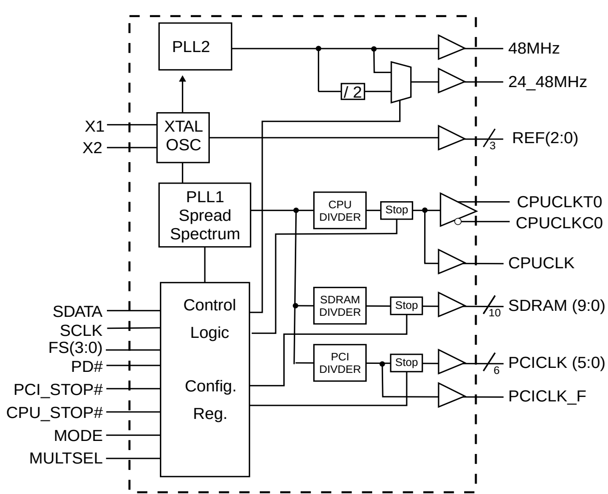


48-Pin 300mil SSOP

Notes:

REF0 can be 1X or 2X strength controlled by I^2C.
* Internal Pull-up Resistor of 120K to VDD
** Internal Pull-down of 120K to GND

Block Diagram



Functionality

FS3	FS2	FS1	FS0	CPU (MHz)	SDRAM (MHz)	PCICLK (MHz)
0	0	0	0	66.6	100.0	33.3
0	0	0	1	100.0	100.0	33.3
0	0	1	0	150.0	100.0	37.5
0	0	1	1	133.3	100.0	33.3
0	1	0	0	66.8	133.6	33.4
0	1	0	1	100.0	133.3	33.3
0	1	1	0	100.0	150.0	37.5
0	1	1	1	133.3	133.3	33.3
1	0	0	0	66.8	66.8	33.4
1	0	0	1	97.0	97.0	32.3
1	0	1	0	70.0	105.0	35.0
1	0	1	1	95.0	95.0	31.7
1	1	0	0	95.0	126.7	31.7
1	1	0	1	112.0	112.0	37.3
1	1	1	0	97.0	129.3	32.2
1	1	1	1	96.2	96.2	32.1

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	CPUCLKC0	OUT	"Complementary" clocks of differential pair CPU outputs. These clocks are 180° out of phase with SDRAM clocks. These open drain outputs need an external 1.5V pull-up.
2	CPUCLKT0	OUT	"True" clocks of differential pair CPU outputs. These clocks are in phase with SDRAM clocks. These open drain outputs need an external 1.5V pull-up.
3, 9, 18, 30, 37	VDD	PWR	Power supply pins, nominal 3.3V
4, 12, 17, 25, 31, 36, 46, 48	GND	PWR	Ground pins
5, 22	AVDD	PWR	Analog power supply for 3.3V
6	X1	IN	Crystal input,nominally 14.318MHz.
7	X2	OUT	Crystal output, nominally 14.318MHz.
8	FS0[2, 3]	IN	Frequency select pin.
	REF0	OUT	14.318 MHz reference clock.
10	FS1[2, 3]	IN	Frequency select pin.
	REF1	OUT	14.318 MHz reference clock.
11	REF2	OUT	14.318 MHz reference clock.
13	FS2[1, 3]	IN	Frequency select pin.
	PCICLK_F	OUT	Free running PCICLK not stoped by PCI_STOP#
21, 20, 19, 16, 15, 14	PCICLK(5:0)	OUT	PCI clock outputs.
23	MULTSEL[2, 3]	IN	3.3V LVTTL input for selecting the current multiplier for CPU outputs.
	24_48MHz	OUT	Selectable 48 or 24MHz output
24	FS3[2, 3]	IN	Frequency select pin.
	48MHz	OUT	48MHz output clock
26	SCLK	IN	Clock input of I^2C input, 5V tolerant input
27	PD#[1]	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms. This pin will be activiated when
	VttPWRGD#	IN	This 3.3V LVTTL input is a level sensitive strobe used to determine when FS and MULTISEL0 inputs are valid and are ready to be sampled (active low)
28	CPU_STOP#[1]	IN	This asynchronous input halts CPU, SDRAM, and AGP clocks at logic "0" level when driven low, the stop selection can be programmed through I^2C.
29	PCI_STOP#[1]	IN	Stops all PCICLKsbesides the PCICLK_F clocks at logic 0 level, when input low
32, 33, 34, 35, 38, 39, 40, 41	SDRAM (7:0)	OUT	SDRAM clock outputs.
42	SDRAM_STOP#[1]	IN	Stops all SDRAMs besides the SDRAM_F clocks at logic 0 level, when input low
43	SDATA	IN	Data input for I^2C serial input, 5V tolerant input
44	VDDL	PWR	Power supply pins, nominal 2.5V
45	CPUCLK	OUT	2.5V CPU clock
47	I REF	OUT	This pin establishes the reference current for the CPUCLK pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current.

Notes:

1: Internal Pull-up Resistor of 120K to 3.3V on indicated inputs

2: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.

3: Internal Pull-down resistor of 120K to GND on indicated inputs.

General Description

The **ICS950104** is a main clock synthesizer chip for PIII based systems with ALI 1651 style chipset. This provides all clocks required for such a system.

The **ICS950104** belongs to ICS new generation of programmable system clock generators. It employs serial programming I^2C interface as a vehicle for changing output functions, changing output frequency, configuring output strength, configuring output to output skew, changing spread spectrum amount, changing group divider ratio and dis/enabling individual clocks. This device also has ICS propriety 'Watchdog Timer' technology which will reset the frequency to a safe setting if the system become unstable from over clocking.

MULTISEL0	Board Target Trace/Term Z	Reference R, Iref = V_{DD}/(3*Rr)	Output Current	Voh @ Z
0	50 ohms	Rr = 221 1%, Iref = 5.00mA	Ioh = 4* I REF	1.0V @ 50
1	50 ohms	Rr = 475 1%, Iref = 2.32mA	Ioh = 6* I REF	0.7V @ 50

General I^2C serial interface information for the ICS950104

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte 0 through Byte 20*** (see Note)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends ***Byte 0 through byte 8 (default)***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8).***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Write:

Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
○	
○	○
○	○
	○
Byte 18	
	ACK
Byte 19	
	ACK
Byte 20	
	ACK
Stop Bit	

*See notes on the following page.

How to Read:

Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
If 7_H has been written to B8	***Byte 7***
ACK	
○	○
○	○
○	○
If 12_H has been written to B8	***Byte18***
ACK	
If 13_H has been written to B8	***Byte 19***
ACK	
If 14_H has been written to B8	***Byte 20***
ACK	
Stop Bit	

Brief I^{2}C registers description for ICS950104 Programmable System Frequency Generator

Register Name	Byte	Description	PWD Default
Functionality & Frequency Select Register	0	Output frequency, hardware / I^{2}C frequency select, spread spectrum & output enable control register.	See individual byte description
Output Control Registers	1-6	Active / inactive output control registers/latch inputs read back.	See individual byte description
Vendor ID & Revision ID Registers	7	Byte 11 bit[7:4] is ICS vendor id - 1001. Other bits in this register designate device revision ID of this part.	See individual byte description
Byte Count Read Back Register	8	Writing to this register will configure byte count and how many byte will be read back. Do not write 00_H to this byte.	08_H
Watchdog Timer Count Register	9	Writing to this register will configure the number of seconds for the watchdog timer to reset.	10_H
Watchdog Control Registers	10 Bit [6:0]	Watchdog enable, watchdog status and programmable 'safe' frequency' can be configured in this register.	000,0000
VCO Control Selection Bit	10 Bit [7]	This bit select whether the output frequency is control by hardware/byte 0 configurations or byte 11&12 programming.	0
VCO Frequency Control Registers	11-12	These registers control the dividers ratio into the phase detector and thus control the VCO output frequency.	Depended on hardware/byte 0 configuration
Spread Spectrum Control Registers	13-14	These registers control the spread percentage amount.	Depended on hardware/byte 0 configuration
Group Skews Control Registers	15-16	Increment or decrement the group skew amount as compared to the initial skew.	See individual byte description
Output Rise/Fall Time Select Registers	17-20	These registers will control the output rise and fall time.	See individual byte description

Notes:

1. The ICS clock generator is a slave/receiver, I^{2}C component. It can read back the data stored in the latches for verification. Readback will support standard SMBUS controller protocol. **The number of bytes to readback is defined by writing to byte 8.**
2. **When writing to byte 11 - 12, and byte 13 - 14, they must be written as a set.** If for example, only byte 14 is written but not 15, neither byte 14 or 15 will load into the receiver.
3. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
4. The input is operating at 3.3V logic levels.
5. The data byte format is 8 bit bytes.
6. To simplify the clock generator I^{2}C interface, the protocol is set to use only Block-Writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
7. At power-on, all registers are set to a default condition, as shown.

Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Description									PWD
	Bit7	Bit2	Bit6	Bit5	Bit4	CPU	SDRAM	PCI	SS	
Bit 7, 2, Bit 6:4	0	0	0	0	0	66.6	100.0	33.3	0 to-0.5%	00010 Note1
	0	0	0	0	1	100.0	100.0	33.3	0 to-0.5%	
	0	0	0	1	0	150.0	100.0	37.5	±0.25%	
	0	0	0	1	1	133.3	100.0	33.3	0 to-0.5%	
	0	0	1	0	0	66.8	133.6	33.4	0 to-0.5%	
	0	0	1	0	1	100.0	133.3	33.3	0 to-0.5%	
	0	0	1	1	0	100.0	150.0	37.5	±0.25%	
	0	0	1	1	1	133.3	133.3	33.3	0 to-0.5%	
	0	1	0	0	0	66.8	66.8	33.4	±0.25%	
	0	1	0	0	1	97.0	97.0	32.3	0 to-0.5%	
	0	1	0	1	0	70.0	105.0	35.0	±0.25%	
	0	1	0	1	1	95.0	95.0	31.7	±0.25%	
	0	1	1	0	0	95.0	126.7	31.7	±0.25%	
	0	1	1	0	1	112.0	112.0	37.3	±0.25%	
	0	1	1	1	0	97.0	129.3	32.3	0 to-0.5%	
	0	1	1	1	1	96.2	96.2	32.1	0 to-0.5%	
	1	0	0	0	0	66.8	100.2	33.4	±0.25%	
	1	0	0	0	1	100.2	100.2	33.4	±0.25%	
	1	0	0	1	0	166.0	110.7	27.7	±0.25%	
	1	0	0	1	1	100.2	133.6	33.4	±0.25%	
	1	0	1	0	0	75.0	100.0	37.5	±0.25%	
	1	0	1	0	1	83.3	125.0	31.3	±0.25%	
	1	0	1	1	0	105.0	140.0	35.0	±0.25%	
	1	0	1	1	1	133.6	133.6	33.4	±0.25%	
	1	1	0	0	0	110.3	147.0	36.8	±0.25%	
	1	1	0	0	1	115.0	153.3	38.3	±0.25%	
	1	1	0	1	0	120.0	120.0	30.0	±0.25%	
	1	1	0	1	1	138.0	138.0	34.5	±0.25%	
	1	1	1	0	0	140.0	140.0	35.0	±0.25%	
	1	1	1	0	1	145.0	145.0	36.3	±0.25%	
	1	1	1	1	0	147.5	147.5	36.9	±0.25%	
	1	1	1	1	1	160.0	160.0	26.7	±0.25%	
Bit 3	0 - Frequency is selected by hardware select, Latched Inputs 1 - Frequency is selected by Bit 7, 2, 6:4									0
Bit 1	0 - Normal 1 - Spread Spectrum Enabled									1
Bit 0	0 - Running 1- Tristate all outputs									0

Note: PWD = Power-Up Default

Note1:
Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.
The I^2C readback for Bits 7, 2, 6:4 indicate the revision code.

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Byte 1: CPU, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	FS3#
Bit 6	11	1	REF2
Bit 5	10	1	REF1
Bit 4	24	1	48MHz
Bit 3	8	1	REF0
Bit 2	8, 10, 11	1	REF(2:0) 1X, 2X default = 1=1X
Bit 1	-	1	(Reserved)
Bit 0	1, 2	1	CPUCLKT/C0

Byte 2: PCI, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	(Reserved)
Bit 6	21	1	PCICLK5
Bit 5	20	1	PCICLK4
Bit 4	19	1	PCICLK3
Bit 3	16	1	PCICLK2
Bit 2	15	1	PCICLK1
Bit 1	14	1	PCICLK0
Bit 0	13	1	PCICLK_F

Byte 3: SDRAM, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	FS0#
Bit 6	-	X	FS1#
Bit 5	-	X	FS2#
Bit 4	33	1	SDRAM6
Bit 3	32	1	SDRAM7
Bit 2	-	1	(Reserved)
Bit 1	45	1	CPUCLK
Bit 0	23	1	24_48MHz

Byte 4: Reserved , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	41	1	SDRAM0
Bit 4	40	1	SDRAM1
Bit 3	39	1	SDRAM2
Bit 2	38	1	SDRAM3
Bit 1	35	1	SDRAM4
Bit 0	34	1	SDRAM5

Byte 5: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(Reserved)
Bit 6	-	1	24_48MHz select: 0=48MHz, 1=24MHz
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	-	1	(Reserved)
Bit 2	-	1	(Reserved)
Bit 1	-	0	(Reserved)
Bit 0	-	0	(Reserved)

Byte 6: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Reserved (Note)
Bit6	-	0	Reserved (Note)
Bit5	-	0	Reserved (Note)
Bit4	-	0	Reserved (Note)
Bit3	-	0	Reserved (Note)
Bit2	-	1	Reserved (Note)
Bit1	-	1	Reserved (Note)
Bit0	-	1	Reserved (Note)

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.

Byte 7: Vendor ID and Revision ID Register

Bit	PWD	Description
Bit 7	0	Vendor ID
Bit 6	0	Vendor ID
Bit 5	1	Vendor ID
Bit 4	X	Revision ID
Bit 3	X	Revision ID
Bit 2	X	Revision ID
Bit 1	X	Revision ID
Bit 0	X	Revision ID

Byte 8: Byte Count and Read Back Register

Bit	PWD	Description
Bit 7	0	Reserved
Bit 6	0	Reserved
Bit 5	0	Reserved
Bit 4	0	Reserved
Bit 3	1	Reserved
Bit 2	0	Reserved
Bit 1	0	Reserved
Bit 0	0	Reserved

Byte 9: Watchdog Timer Count Register

Bit	PWD	Description
Bit 7	0	The decimal representation of these 8 bits correspond to how many 290ms the watchdog timer will wait before it goes to alarm mode and reset the frequency to the safe setting. Default at power up is 16X 290ms = 4.64 seconds.
Bit 6	0	
Bit 5	0	
Bit 4	1	
Bit 3	0	
Bit 2	0	
Bit 1	0	
Bit 0	0	

Byte 10: VCO Control Selection Bit & Watchdog Timer Control Register

Bit	PWD	Description
Bit 7	0	0=Hw/B0 freq / 1=B11 & 12 freq
Bit 6	0	WD Enable 0=disable / 1=enable
Bit 5	0	WD Status 0=normal / 1=alarm
Bit 4	0	WD Safe Frequency, Byte 0 bit 2
Bit 3	0	WD Safe Frequency, FS3
Bit 2	0	WD Safe Frequency, FS2
Bit 1	0	WD Safe Frequency, FS1
Bit 0	0	WD Safe Frequency, FS0

Note: FS values in bit (0:4) will correspond to Byte 0 FS values. Default safe frequency is same as 00000 entry in byte0.

Byte 11: VCO Frequency Control Register

Bit	PWD	Description
Bit 7	X	VCO Divider Bit0
Bit 6	X	REF Divider Bit6
Bit 5	X	REF Divider Bit5
Bit 4	X	REF Divider Bit4
Bit 3	X	REF Divider Bit3
Bit 2	X	REF Divider Bit2
Bit 1	X	REF Divider Bit1
Bit 0	X	REF Divider Bit0

Note: The decimal representation of these 7 bits (Byte 11 (6:0)) + 2 is equal to the REF divider value .

Byte 12: VCO Frequency Control Register

Bit	PWD	Description
Bit 7	X	VCO Divider Bit8
Bit 6	X	VCO Divider Bit7
Bit 5	X	VCO Divider Bit6
Bit 4	X	VCO Divider Bit5
Bit 3	X	VCO Divider Bit4
Bit 2	X	VCO Divider Bit3
Bit 1	X	VCO Divider Bit2
Bit 0	X	VCO Divider Bit1

Note: The decimal representation of these 9 bits (Byte 12 bit (7:0) & Byte 11 bit (7)) + 8 is equal to the VCO divider value. For example if VCO divider value of 36 is desired, user need to program 36 - 8 = 28, namely, 0, 00011100 into byte 12 bit & byte 11 bit 7.

Notes:

1. PWD = Power on Default

Byte 13: Spread Sectrum Control Register

Bit	PWD	Description
Bit 7	X	Spread Spectrum Bit7
Bit 6	X	Spread Spectrum Bit6
Bit 5	X	Spread Spectrum Bit5
Bit 4	X	Spread Spectrum Bit4
Bit 3	X	Spread Spectrum Bit3
Bit 2	X	Spread Spectrum Bit2
Bit 1	X	Spread Spectrum Bit1
Bit 0	X	Spread Spectrum Bit0

Note: Please utilize software utility provided by ICS Application Engineering to configure spread spectrum. Incorrect spread percentage may cause system failure.

Byte 14: Spread Sectrum Control Register

Bit	PWD	Description
Bit 7	X	Reserved
Bit 6	X	Reserved
Bit 5	X	Reserved
Bit 4	X	Spread Spectrum Bit12
Bit 3	X	Spread Spectrum Bit11
Bit 2	X	Spread Spectrum Bit10
Bit 1	X	Spread Spectrum Bi 9
Bit 0	X	Spread Spectrum Bit8

Note: Please utilize software utility provided by ICS Application Engineering to configure spread spectrum. Incorrect spread percentage may cause system failure.

Byte 15: Output Skew Control

Bit	PWD	Description
Bit 7	1	(Reserved)
Bit 6	1	
Bit 5	1	CPUCLK Skew Control
Bit 4	1	
Bit 3	1	(Reserved)
Bit 2	1	
Bit 1	1	SDRAM (7:0) Skew Control
Bit 0	1	

Byte 16: Output Skew Control

Bit	PWD	Description
Bit 7	0	PCICLK (5:0, F) Skew Control
Bit 6	0	
Bit 5	0	
Bit 4	0	
Bit 3	0	(Reserved)
Bit 2	1	
Bit 1	0	
Bit 0	0	

Byte 17: Output Rise/Fall Time Select Register

Bit	PWD	Description
Bit 7	1	(Reserved)
Bit 6	0	
Bit 5	1	CPUCLK Slew Rate Control
Bit 4	0	
Bit 3	1	PCICLK_F Slew Rate Control
Bit 2	0	
Bit 1	1	PCICLK (5:0) Slew Rate Control
Bit 0	0	

Byte 18: Output Rise/Fall Time Select Register

Bit	PWD	Description
Bit 7	1	(Reserved)
Bit 6	0	
Bit 5	1	SDRAM (7:0) Slew Control
Bit 4	0	
Bit 3	1	(Reserved)
Bit 2	0	
Bit 1	1	48MHz Slew Rate Control
Bit 0	0	

Notes:

1. PWD = Power on Default
2. The power on default for byte 13-20 depends on the harware (latch inputs FS(4:0)) or I^2C (Byte 0 bit (1:7)) setting. Be sure to read back and re-write the values of these 8 registers when VCO frequency change is desired for the first pass.
3. If Byte 8 bit 7 is driven to "1" meaning programming is intended, Byte 21-24 will lose their default power up value.

Byte 19: Reserved Register

Bit	PWD	Description
Bit 7	X	Reserved
Bit 6	X	Reserved
Bit 5	X	Reserved
Bit 4	X	Reserved
Bit 3	X	Reserved
Bit 2	X	Reserved
Bit 1	X	Reserved
Bit 0	X	Reserved

Byte 20: Reserved Register

Bit	PWD	Description
Bit 7	X	Reserved
Bit 6	X	Reserved
Bit 5	X	Reserved
Bit 4	X	Reserved
Bit 3	X	Reserved
Bit 2	X	Reserved
Bit 1	X	Reserved
Bit 0	X	Reserved

Note: Byte 19 and 20 are reserved registers, these are unused registers writing to these registers will not affect device performance or functinality.

VCO Programming Constrains

VCO Frequency .... 150MHz to 500MHz
VCO Divider Range .... 8 to 519
REF Divider Range .... 2 to 129
Phase Detector Stability .... 0.3536 to 1.4142

Useful Formula

VCO Frequency = 14.31818 x VCO/REF divider value
Phase Detector Stabiliy = 14.038 x (VCO divider value)$^{-0.5}$

To program the VCO frequency for over-clocking.

0. Before trying to program our clock manually, consider using ICS provided software utilities for easy programming.
1. Select the frequency you want to over-clock from with the desire gear ratio (i.e. CPU:SDRAM:3V66:PCI ratio) by writing to byte 0, or using initial hardware power up frequency.
2. Write 0001, 1001 (19_H) to byte 8 for readback of 21 bytes (byte 0-20).
3. Read back byte 11-20 and copy values in these registers.
4. Re-initialize the write sequence.
5. Write a '1' to byte 9 bit 7 and write to byte 11 & 12 with the desired VCO & REF divider values.
6. Write to byte 13 to 20 with the values you copy from step 3. This maintains the output spread, skew and slew rate.
7. The above procedure is only needed when changing the VCO for the 1st pass. If VCO frequency needed to be changed again, user only needs to write to byte 11 and 12 unless the system is to reboot.

Note:

1. User needs to ensure step 3 & 7 is carried out. Systems with wrong spread percentage and/or group to group skew relation programmed into bytes 13-16 could be unstable. Step 3 & 7 assure the correct spread and skew relationship.
2. If VCO, REF divider values or phase detector stability are out of range, the device may fail to function correctly.
3. Follow min and max VCO frequency range provided. Internal PLL could be unstable if VCO frequency is too fast or too slow. Use 14.31818MHz x VCO/REF divider values to calculate the VCO frequency (MHz).
4. ICS recommends users, to utilize the software utility provided by ICS Application Engineering to program the VCO frequency.
5. Spread percent needs to be calculated based on VCO frequency, spread modulation frequency and spreadamount desired. See Application note for software support.

Absolute Maximum Ratings

Supply Voltage . . . . 5.5 V
Logic Inputs . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . 0°C to +70°C
Case Temperature . . . . 115°C
Storage Temperature . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70º C; Supply Voltage $V_{DD = 3.3V}$, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$			5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			µA
Operating Supply Current	$I_{DD3.3OP66}$	C_L = 0 pF; Select @ 66MHz			77	mA
	$I_{DD3.3OP100}$	C_L = 0 pF; Select @ 100MHz			100	
Input frequency	F_i	V_{DD} = 3.3 V;	12		16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLKT/C

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Source Output Impedance	Z_O	$V_O = V_X$	3000			Ω
Output High Voltage	V_{OH}	V_R = 475W ±1%; IREF = 2.32mA; I_{OH} = 6*IREF		0.71	1.2	V
Output High Current	I_{OH}			-13.92		mA
Rise Time[1]	t_r	V_{OL} = 20%, V_{OH} = 80%	175		700	ps
Differential Crossover Voltage[1]	V_X	Note 3	45	50	55	%
Duty Cycle[1]	d_t	V_T = 50%	45	51	55	%
Skew[1], CPU to CPU	t_{sk}	V_T = 50%			100	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc}$	$V_T = V_X$			150	ps

Notes:

1 - Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLK

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	I_{OH} = -12.0 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA			0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V			-19	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19			mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V			1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V			1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45		55	%
Skew	t_{sk2B}[1]	V_T = 1.25 V			250	ps
Jitter, Cycle-to-cycle	$t_{jcyc-cyc2B}$[1]	V_T = 1.25 V			250	ps
Jitter, One Sigma	t_{j1s2B}[1]	V_T = 1.25 V			150	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-33		-33	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			175	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V			500	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70° C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH3}	I_{OH} = -28 mA	2.4			V
Output Low Voltage	V_{OL3}	I_{OL} = 23 mA			0.4	V
Output High Current	I_{OH3}	V_{OH} = 2.0 V			-54	mA
Output Low Current	I_{OL3}	V_{OL} = 0.8 V	41			mA
Rise Time	T_{r3}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V			2	ns
Fall Time	T_{f3}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V			2	ns
Duty Cycle	D_{t3}[1]	V_T = 1.5 V	45		55	%
Skew[1]	T_{sk1}	V_T = 1.5 V			250	ps
Propagation Delay	Tprop	VT = 1.5 V			5	ns

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - 24MHz, 48MHz, REF

T_A = 0 - 70° C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -16 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V			2	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V			2	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45		55	%
Jitter, One Sigma[1]	t_{j1s5}	V_T = 1.5 V			0.5	ns
Jitter, Absolute[1]	t_{jabs5}	V_T = 1.5 V	-1		1	ns

[1]Guaranteed by design, not 100% tested in production.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

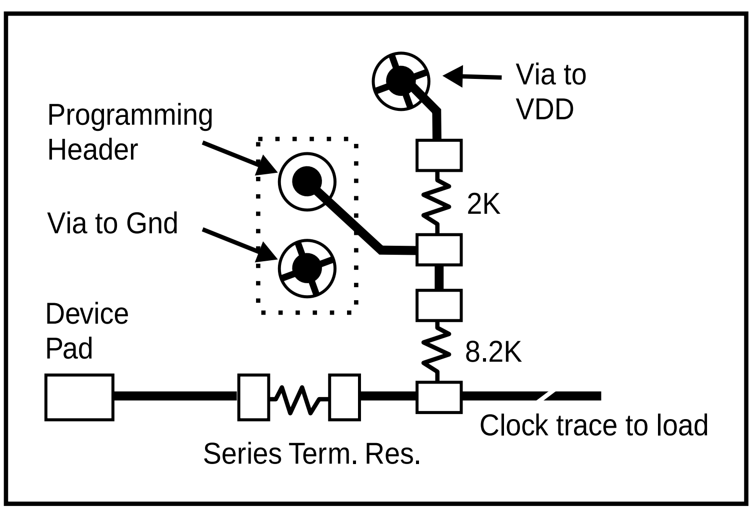
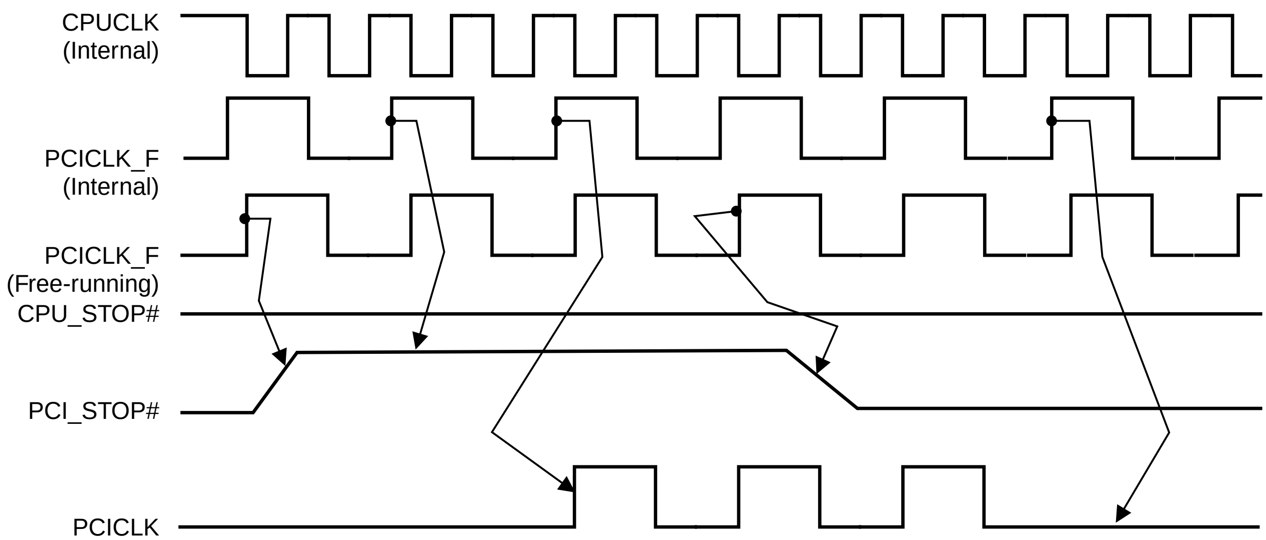


Fig. 1

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS94252**. It is used to turn off the PCICLK clocks for low power operation. PCI_STOP# is synchronized by the **ICS94252** internally. The minimum that the PCICLK clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK clocks. PCICLK clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



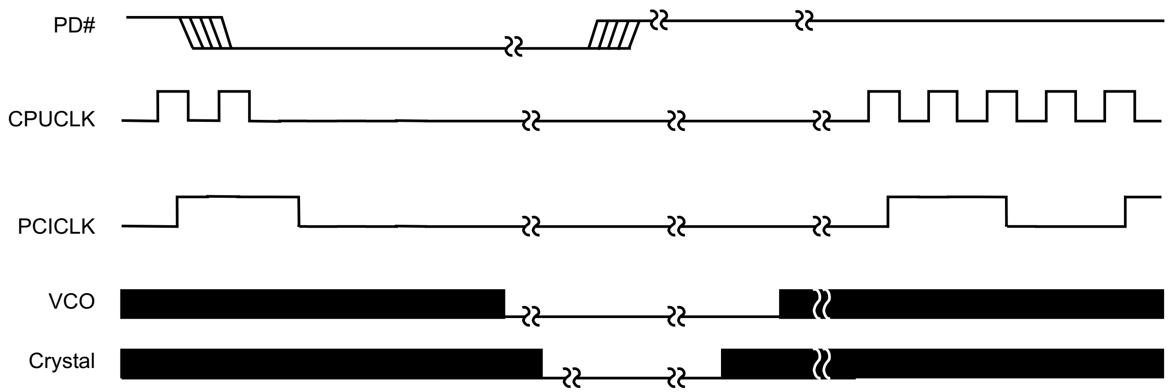
Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS94252 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS94252.
3. All other clocks continue to run undisturbed.
4. CPU_STOP# is shown in a high (true) state.

PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

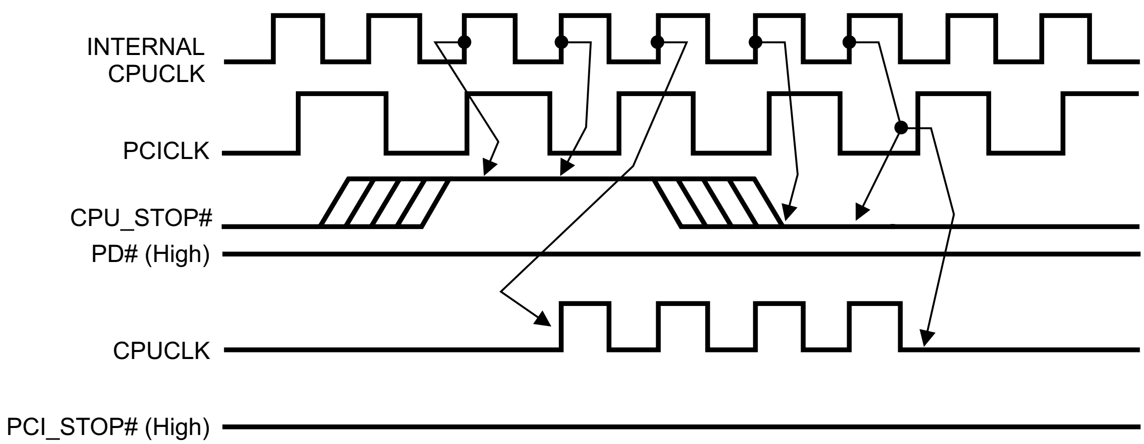
Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. PCI_STOP# and CPU_STOP# are considered to be don't cares during the power down operations. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.



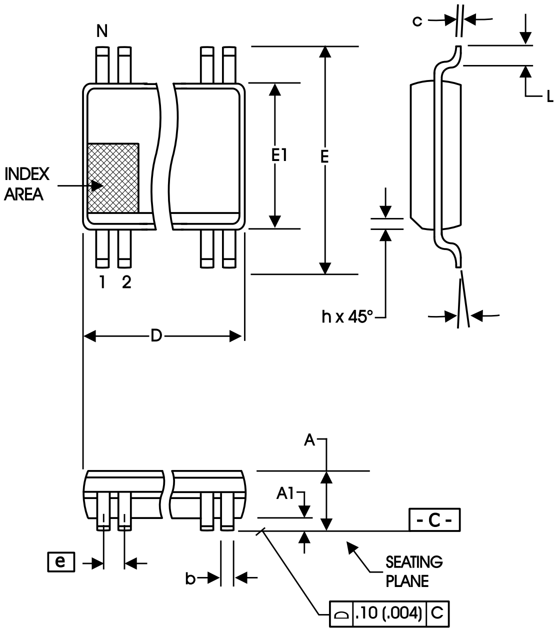
Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS94252 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.

CPU_STOP# Timing Diagram

CPU_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CPU_STOP# is synchronized by the **ICS94252**. The minimum that the CPU clock is enabled (CPU_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.



Notes:
1. All timing is referenced to the internal CPU clock.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS94252.
3. All other clocks continue to run undisturbed.



300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS950104yFT

Example:

ICS XXXX y F - T

- T — **Designation for tape and reel packaging**
- F — **Package Type**
  F=SSOP
- y — **Revision Designator** (will not correlate with datasheet revision)
- XXXX — **Device Type**
- ICS — **Prefix**
  ICS = Standard Device