HIGH SPEED 64K (4K X 16 BIT) SEQUENTIAL ACCESS RANDOM ACCESS MEMORY (SARAM™)

IDT70824S/L

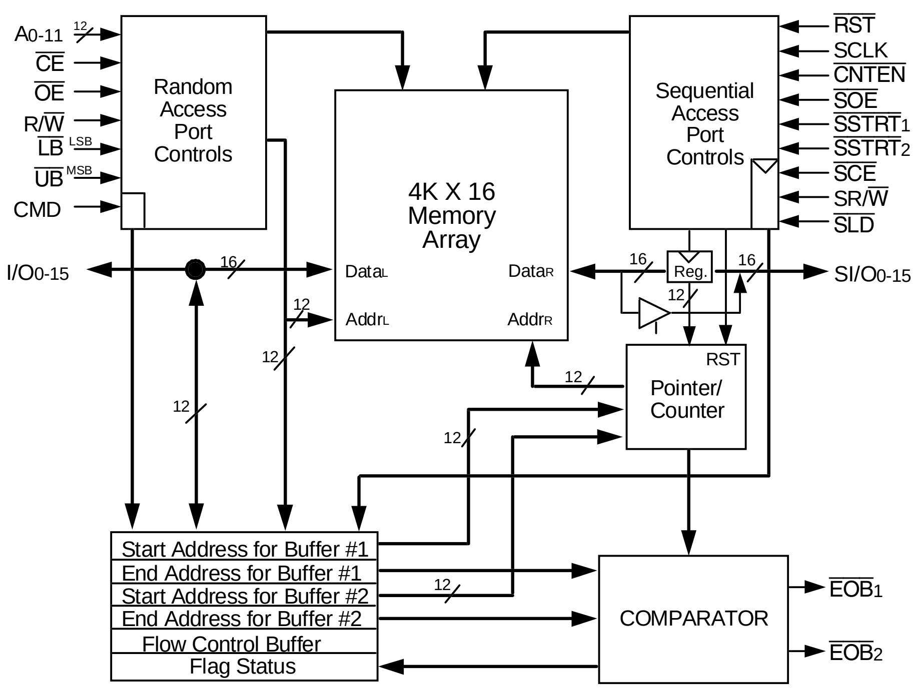
Features

- **High-speed access**
  - *Military: 35/45ns (max.)*
  - *Commercial: 20/25/35/45ns (max.)*
- **Low-power operation**
  - *IDT70824S*
    Active: 775mW (typ.)
    Standby: 5mW (typ.)
  - *IDT70824L*
    Active: 775mW (typ.)
    Standby: 1mW (typ.)
- **4K x 16 Sequential Access Random Access Memory (SARAM™)**
  - *Sequential Access from one port and standard Random Access from the other port*
  - *Separate upper-byte and lower-byte control of the Random Access Port*
- **High speed operation**
  - *20ns t_{AA} for random access port*
  - *20ns t_{CD} for sequential port*
  - *25ns clock cycle time*
- **Architecture based on Dual-Port RAM cells**
- **Compatible with Intel BMIC and 82430 PCI Set**
- **Width and Depth Expandable**
- **Sequential side**
  - *Address based flags for buffer control*
  - *Pointer logic supports up to two internal buffers*
- **Battery backup operation - 2V data retention**
- **TTL-compatible, single 5V (±10%) power supply**
- **Available in 80-pin TQFP and 84-pin PGA**
- **Military product compliant to MIL-PRF-38535 QML**
- **Industrial temperature range (–40°C to +85°C) is available for selected speeds**

Description

The IDT70824 is a high-speed 4K x 16-Bit Sequential Access Random Access Memory (SARAM). The SARAM offers a single-chip solution to buffer data sequentially on one port, and be accessed randomly (asynchronously) through the other port. The device has a Dual-Port RAM based architecture with a standard SRAM interface for the random (asynchronous) access port, and a clocked interface with counter se-

Functional Block Diagram



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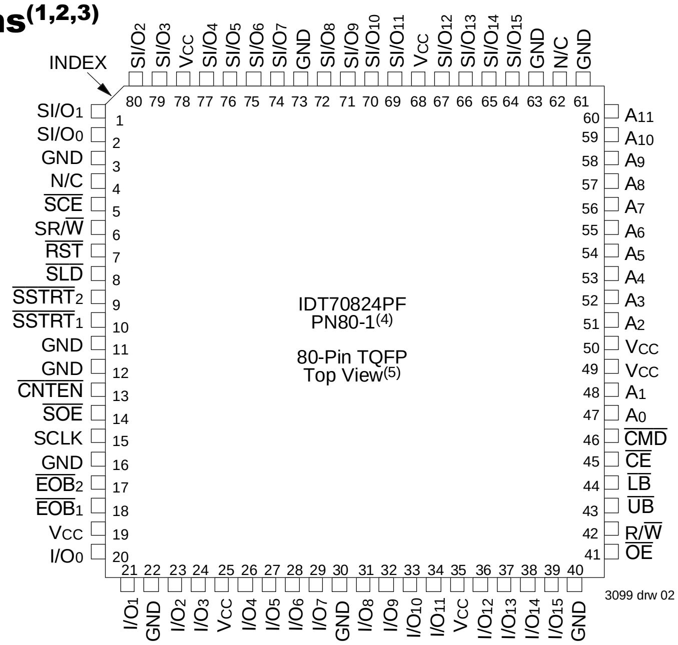
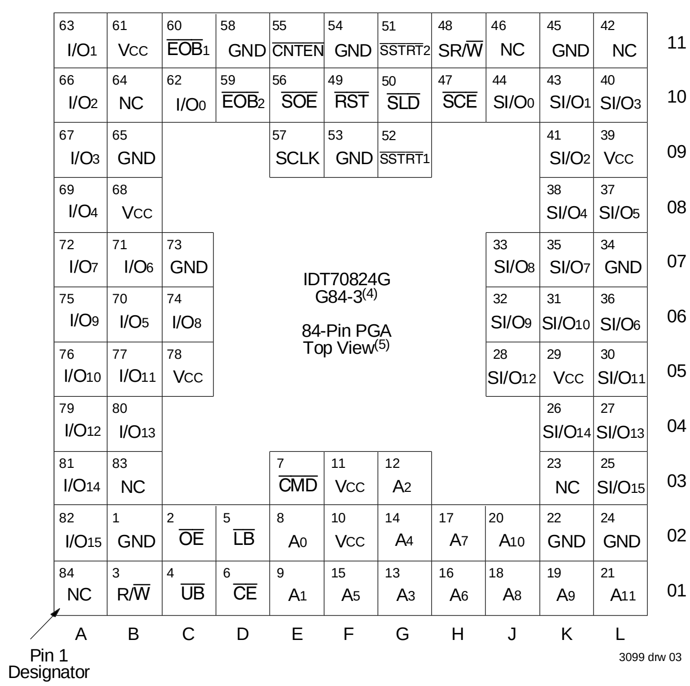
quencing for the sequential (synchronous) access port.

Fabricated using CMOS high-performance technology, this memory device typically operates on less than 775mW of power at maximum high-speed clock-to-data and Random Access. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT70824 is packaged in a 80-pin Thin Quad Flatpack (TQFP) or 84-pin Pin Grid Array (PGA). Military grade product is manufactured in compliance with the latest revision of MIL-PRF-38535 QML, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

Pin Configurations(1,2,3)





NOTES:
1. All VCC pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. PN80-1 package body is approximately 14mm x 14mm x 1.4mm.
   G84-3 package body is approximately 1.12 in x 1.12 in x .16 in.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Descriptions: Random Access Port(1)

SYMBOL	NAME	I/O	DESCRIPTION
A_0-A_{11}	Address Lines	I	Address inputs to access the 4096-word (16-Bit) memory array.
I/O_0-I/O_{15}	Inputs/Outputs	I	Random access data inputs/outputs for 16-Bit wide data.
$\overline{CE}$	Chip Enable	I	When $\overline{CE}$ is LOW, the random access port is enabled. When $\overline{CE}$ is HIGH, the random access port is disabled into power-down mode and the I/O outputs are in the High-impedance state. All data is retained during $\overline{CE}$ = V_{IH}, unless it is altered by the sequential port $\overline{CE}$ and $\overline{CMD}$ may not be LOW at the same time.
$\overline{CMD}$	Control Register Enable	I	When $\overline{CMD}$ is LOW, address lines A_0-A_2, R/$\overline{W}$, and inputs and outputs I/O_0-I/O_{12}, are used to access the control register, the flag register and the start and end of buffer registers. $\overline{CMD}$ and $\overline{CE}$ may not be LOW at the same time.
R/$\overline{W}$	Read/Write Enable	I	If $\overline{CE}$ is LOW and $\overline{CMD}$ is HIGH, data is written into the array when R/$\overline{W}$ is LOW and read out of the array when R/$\overline{W}$ is HIGH. If $\overline{CE}$ is HIGH and $\overline{CMD}$ is LOW, R/$\overline{W}$ is used to access the buffer command registers. $\overline{CE}$ and $\overline{CMD}$ may not be LOW at the same time.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW and R/$\overline{W}$ is HIGH, I/O_0-I/O_{15} outputs are enabled. When $\overline{OE}$ is HIGH, the I/O outputs are in the High-impedance state.
$\overline{LB}$, $\overline{UB}$	Lower Byte, Upper Byte Enables	I	When $\overline{LB}$ is LOW, I/O_0-I/O_7 are accessible for read and write operations. When $\overline{LB}$ is HIGH, I/O_0-I/O_7 are tri-stated and blocked during read and write operations. $\overline{UB}$ controls access for I/O_8-I/O_{15} in the same manner and is asynchronous from $\overline{LB}$.
V_{CC}	Power Supply	I	Seven +5 power supply pins. All V_{CC} pins must be connected to the same +5V V_{CC} supply.
GND	Ground	I	Ten ground pins. All ground pins must be connected to the same ground supply.

3099 tbl 01

Pin Descriptions: Sequential Access Port(1)

SYMBOL	NAME	I/O	DESCRIPTION
SI/O0-15	Inputs/Outputs	I/O	Sequential data inputs/outputs for 16-bit wide data.
SCLK	Clock	I	SI/O_0-SI/O_{15}, $\overline{SCE}$, SR/$\overline{W}$, and SLD are registered on the LOW-to-HIGH transition of SCLK. Also, the sequential access port address pointer increments by 1 on each LOW-TO-HIGH transition of SCLK when $\overline{CNTEN}$ is LOW.
$\overline{SCE}$	Chip Enable	I	When $\overline{SCE}$ is LOW, the sequential access port is enabled on the LOW-to-HIGH transition of SCLK. When $\overline{SCE}$ is HIGH, the sequential access port is disabled into powered-down mode on the LOW-to-HIGH transition of SCLK, and the SI/O outputs are in the High-impedance state. All data is retained, unless altered by the random access port.
$\overline{CNTEN}$	Counter Enable	I	When $\overline{CNTEN}$ is LOW, the address pointer increments on the LOW-to-HIGH transition of SCLK. This function is independent of $\overline{CE}$.
SR/$\overline{W}$	Read/Write Enable	I	When SR/$\overline{W}$ and $\overline{SCE}$ are LOW, a write cycle is initiated on the LOW-to-HIGH transition of SCLK. When SR/$\overline{W}$ is HIGH, and $\overline{SCE}$ and $\overline{SOE}$ are LOW, a read cycle is initiated on the LOW-to-HIGH transition of SCLK. Termination of a write cycle is done on the LOW-to-HIGH transition of SCLK if SR/W or $\overline{SCE}$ is HIGH.
$\overline{SLD}$	Address Pointer Load Control	I	When $\overline{SLD}$ is sampled LOW, there is an internal delay of one cycle before the address pointer changes. When $\overline{SLD}$ is LOW, data on the inputs SI/O_0-SI/O_{11} is loaded into a data-in register on the LOW-to-HIGH transition of SCLK. On the Cycle following $\overline{SLD}$, the address pointer charges to the address location contained in the data-in register. $\overline{SSTRT_1}$ and $\overline{SSTRT_2}$ may not be LOW while $\overline{SLD}$ is LOW or during the cycle following $\overline{SLD}$.
$\overline{SSTRT_1}$, $\overline{SSTRT_2}$	Load Start of Address Register	I	When $\overline{SSTRT_1}$ or $\overline{SSTRT_2}$ is LOW, the start of address register #1 or #2 is loaded into the address pointer on the LOW-to-HIGH transition of SCLK. The start addresses are stored in internal registers. $\overline{SSTRT_1}$ and $\overline{SSTRT_2}$ may not be LOW while $\overline{SLD}$ is LOW or during the cycle following $\overline{SLD}$.
$\overline{EOB_1}$, $\overline{EOB_2}$	End of Buffer Flag	O	$\overline{EOB_1}$ or $\overline{EOB_2}$ is output low when the address pointer is incremented to match the address stored in the end of buffer registers. The flags can be cleared by either asserting $\overline{RST}$ LOW or by writing zero into Bit 0 and/or Bit 1 of the control register at address 101. $\overline{EOB_1}$ and $\overline{EOB_2}$ are dependent on separate internal registers, and therefore separate match addresses.
$\overline{SOE}$	Output Enable	I	$\overline{SOE}$ controls the data outputs and is independent of SCLK. When $\overline{SOE}$ is LOW, output buffers and the sequentially addressed data is output. When $\overline{SOE}$ is HIGH, the SI/O output bus is in the High-impedance state. $\overline{SOE}$ is asynchronous to SCLK.
$\overline{RST}$	Reset	I	When $\overline{RST}$ is LOW, all internal registers are set to their default state, the address pointer is set to zero and the $\overline{EOB_1}$ and $\overline{EOB_2}$ flags are set HIGH. $\overline{RST}$ is asynchronous to SCLK.

3099 tbl 02

NOTE:
1. "I/O" is bidirectional Input and Output. "I" is Input and "O" is Output.

Absolute Maximum Ratings[1]

Symbol	Rating	Commercial & Industrial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

3099 tbl 03

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of $V_{TERM} \geq$ Vcc + 10%.

Capacitance
(T_A = +25°C, f = 1.0mhz, TQFP only)

Symbol	Parameter	Conditions[2]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	10	pF

3099 tbl 06

NOTES:

1. This parameter is determined by device characterization, but is not production tested.
2. 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

3099 tbl 04

NOTES:

1. This is the parameter T_A.
2. Industrial temperature: for specific speeds, packages and powers contact your sales office.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0[2]	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

3099 tbl 05

NOTES:

1. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 10%.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	70824S		70824L		Unit
			Min.	Max.	Min.	Max.	
$\lvert I_{LI}\rvert$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	5	—	1	µA
$\lvert I_{LO}\rvert$	Output Leakage Current	V_{OUT} = 0V to V_{CC}	—	5	—	1	µA
V_{OL}	Output Low Voltage	I_{OL} = +4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

3099 tbl 07

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[1,2,8] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		70824X20 Com'l Only Typ.[2]	70824X20 Com'l Only Max.	70824X25 Com'l Only Typ.[2]	70824X25 Com'l Only Max.	70824X35 Com'l & Military Typ.[2]	70824X35 Com'l & Military Max.	70824X45 Com'l & Military Typ.[2]	70824X45 Com'l & Military Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IL}, Outputs Open $\overline{SCE}$ = V_{IL}[5] f = f_{MAX}[3]	COM'L	S	180	380	170	360	160	340	155	340	mA
				L	180	330	170	310	160	290	155	290	
			MIL & IND	S	—	—	—	—	160	400	155	400	
				L	—	—	—	—	160	340	155	340	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{SCE}$ and $\overline{CE}$ = V_{IH}[7] $\overline{CMD}$ = V_{IH} f = f_{MAX}[3]	COM'L	S	25	70	25	70	20	70	16	70	mA
				L	25	50	25	50	20	50	16	50	
			MIL & IND	S	—	—	—	—	20	85	16	85	
				L	—	—	—	—	20	65	16	65	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}$ or $\overline{SCE}$ = V_{IH} Active Port Outputs Open, f=f_{MAX}[3]	COM'L	S	115	260	105	250	95	240	90	240	mA
				L	115	230	105	220	95	210	90	210	
			MIL & IND	S	—	—	—	—	95	290	90	290	
				L	—	—	—	—	95	250	90	250	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}$ and $\overline{SCE}$ $\geq$ V_{CC} - 0.2V[6] V_{IN} $\geq$ V_{CC} - 0.2V or V_{IN} $\leq$ 0.2V, f = 0[4]	COM'L	S	1.0	15	1.0	15	1.0	15	1.0	15	mA
				L	0.2	5	0.2	5	0.2	5	0.2	5	
			MIL & IND	S	—	—	—	—	1.0	30	1.0	30	
				L	—	—	—	—	0.2	10	0.2	10	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	One Port $\overline{CE}$ or $\overline{SCE}$ $\geq$ V_{CC} - 0.2V[6,7] Outputs Open (Active Port) f = f_{MAX}[3] V_{IN} $\geq$ V_{CC} - 0.2V or V_{IN} $\leq$ 0.2V	COM'L	S	110	240	100	230	90	220	85	220	mA
				L	110	200	100	190	90	180	85	180	
			MIL & IND	S	—	—	—	—	90	260	85	260	
				L	—	—	—	—	90	215	85	215	

3099 tbl 08

NOTES
1. 'X' in part number indicates power rating (S or L).
2. V_{CC} = 5V, T_A = +25°C; guaranteed by device characterization but not production tested.
3. At f = f_{MAX}, address, control lines (except Output Enable), and SCLK are cycling at the maximum frequency read cycle of 1/t_{RC}.
4. f = 0 means no address or control lines change.
5. $\overline{SCE}$ may transition, but is Low (SCE=V_{IL}) when clocked in by SCLK.
6. $\overline{SCE}$ may be - 0.2V, after it is clocked in, since SCLK=V_{IH} must be clocked in prior to powerdown.
7. If one port is enabled (either $\overline{CE}$ or $\overline{SCE}$ = LOW) then the other port is disabled ($\overline{SCE}$ or $\overline{CE}$ = HIGH, respectively). CMOS HIGH $\geq$ Vcc - 0.2V and LOW $\leq$ 0.2V, and TTL HIGH = V_{IH} and LOW = V_{IL}.
8. Industrial temperature: for specific speeds, packages and powers contact your sales office.

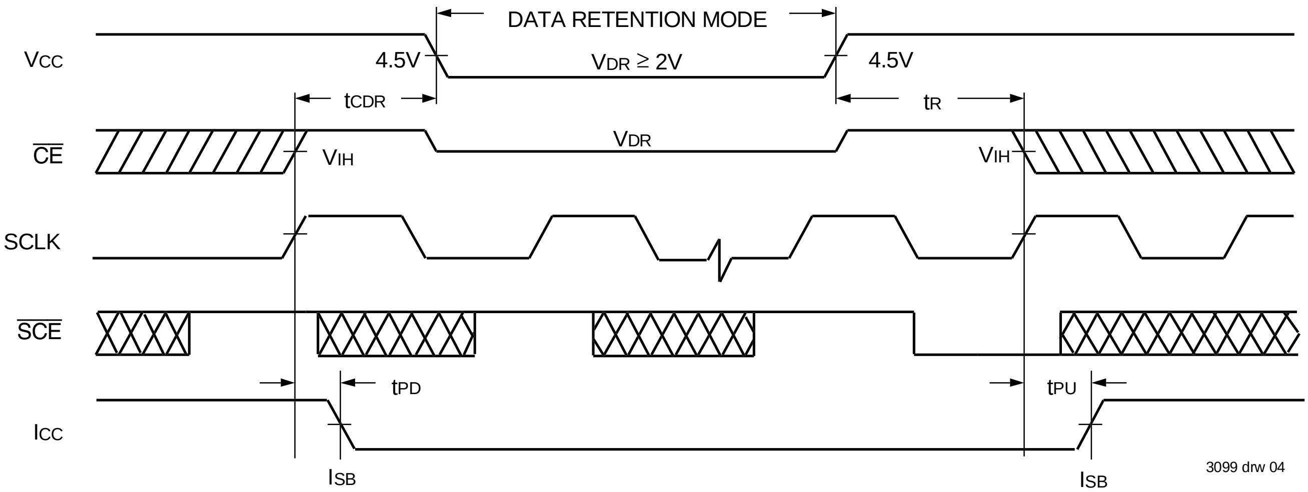
Data Retention Characteristics Over All Temperature Ranges (L Version Only) (V_{LC} $\leq$ 0.2V, V_{HC} $\geq$ V_{CC} - 0.2V)

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE}$ = V_{HC}	MIL. & IND.	—	100	4000	µA
		V_{IN} = V_{HC} or = V_{LC}	COM'L.	—	100	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time	$\overline{SCE}$ = V_{HC}[4] when SCLK = u		—	—	—	V
t_R[3]	Operation Recovery Time	$\overline{CMD}$ $\geq$ V_{HC}		t_{RC}[2]	—	—	V

3099 tbl 09

NOTES :
1. T_A = +25°C, V_{CC} = 2V; guaranteed by device characterization but not production tested.
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed by device characterization, but is not production tested.
4. To initiate data retention, $\overline{SCE}$ = V_{IH} must be clocked in.

Data Retention Power Down/Up Waveform (Random and Sequential Port)[1,2]



NOTES :
1. $\overline{SCE}$ is synchronized to the sequential clock input.
2. $\overline{CMD} \geq V_{CC}$ - 0.2V.

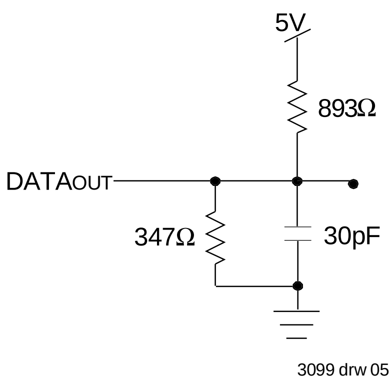


Figure 1. AC Output Test Load

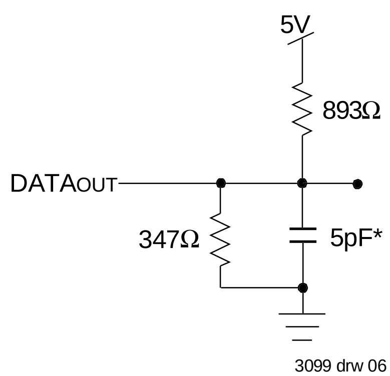


Figure 2. Output Test Load (for tCLZ, tBLZ, tOLZ, tCHZ, tBHZ, tOHZ,tWHZ, tCKHZ, and tCKLZ)
(*Including scope and jig.)

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1,2 and 3

3099 tbl 10

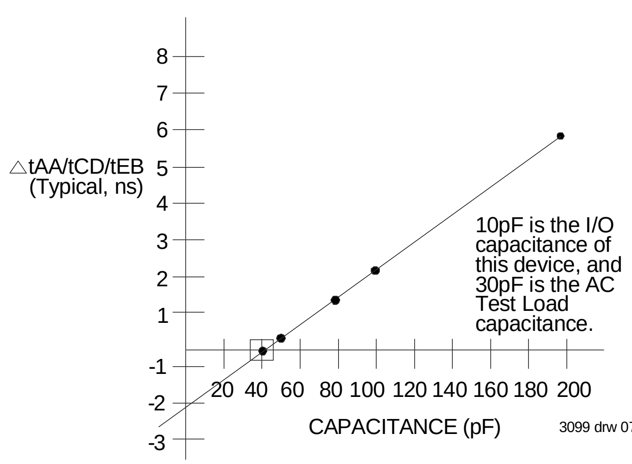


Figure 3. Lumped Capacitance Load Typical Derating Curve

Truth Table I: Random Access Read and Write[1,2]

Inputs/Outputs								
$\overline{CE}$	$\overline{CMD}$	R/$\overline{W}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O_0-I/O_7	I/O_8-I/O_{15}	MODE
L	H	H	L	L	L	$DATA_{OUT}$	$DATA_{OUT}$	Read both Bytes.
L	H	H	L	L	H	$DATA_{OUT}$	High-Z	Read lower Byte only.
L	H	H	L	H	L	High-Z	$DATA_{OUT}$	Read upper Byte only.
L	H	L	H[3]	L	L	$DATA_{IN}$	$DATA_{IN}$	Write to both Bytes.
L	H	L	H[3]	L	H	$DATA_{IN}$	High-Z	Write to lower Byte only.
L	H	L	H[3]	H	L	High-Z	$DATA_{IN}$	Write to upper Byte only.
H	H	X	X	X	X	High-Z	High-Z	Both Bytes deselected and powered down.
L	H	H	H	X	X	High-Z	High-Z	Outputs disabled but not powered down.
L	H	X	X	H	H	High-Z	High-Z	Both Bytes deselected but not powered down.
H	L	L	H[3]	L[4]	L[4]	$DATA_{IN}$	$DATA_{IN}$	Write I/O_0-I/O_{11} to the Buffer Command Register.
H	L	H	L	L[4]	L[4]	$DATA_{OUT}$	$DATA_{OUT}$	Read contents of the Buffer Command Register via I/O_0-I/O_{12}.

3099 tbl 11

NOTES:
1. H = V_{IH}, L = V_{IL}, X = Don't Care, and HIGH-Z = High-impedance.
2. $\overline{RST}$, $\overline{SCE}$, $\overline{CNTEN}$, SR/$\overline{W}$, $\overline{SLD}$, $\overline{SSTRT_1}$, $\overline{SSTRT_2}$, SCLK, SI/O_0-SI/O_{15}, $\overline{EOB_1}$, $\overline{EOB_2}$, and $\overline{SOE}$ are unrelated to the random access port control and operation.
3. If $\overline{OE}$ = V_{IL} during write, t_{WHZ} must be added to the t_{WP} or t_{CW} write pulse width to allow the bus to float prior to being driven.
4. Byte operations to control register using $\overline{UB}$ and $\overline{LB}$ separately are also allowed.

Truth Table II: Sequential Read[1,2,3,6,8]

Inputs/Outputs								
SCLK	$\overline{SCE}$	$\overline{CNTEN}$	SR/$\overline{W}$	$\overline{EOB_1}$	$\overline{EOB_2}$	$\overline{SOE}$	SI/O	MODE
↑	L	L	H	LOW	LAST	L	[$\overline{EOB_1}$]	Counter Advanced Sequential Read with $\overline{EOB_1}$ reached.
↑	L	H	H	LAST	LAST	L	[$\overline{EOB_1}$ - 1]	Non-Counter Advanced Sequential Read, without $\overline{EOB_1}$ reached
↑	L	L	H	LAST	LOW	L	[$\overline{EOB_2}$]	Counter Advanced Sequential Read with $\overline{EOB_2}$ reched.
↑	L	H	H	LAST	LAST	L	[$\overline{EOB_2}$ - 1]	Non-Counter Advanced Sequential Read without $\overline{EOB_2}$ reached
↑	L	L	H	LOW	LOW	H	High-Z	Counter Advanced Sequential Non-Read with $\overline{EOB_1}$ and $\overline{EOB_2}$ reached

3099 tbl 12

Truth Table III: Sequential Write[1,2,3,4,5,6,7,8]

Inputs/Outputs								
SCLK	$\overline{SCE}$	$\overline{CNTEN}$	SR/$\overline{W}$	$\overline{EOB_1}$	$\overline{EOB_2}$	$\overline{SOE}$	SI/O	MODE
↑	L	H	L	LAST	LAST	H	SI/O_{IN}	Non-Counter Advanced Sequential Write, without $\overline{EOB_1}$ or $\overline{EOB_2}$ reached.
↑	L	L	L	LOW	LOW	H	SI/O_{IN}	Counter Advanced Sequential Write with $\overline{EOB_1}$ and $\overline{EOB_2}$ reached.
↑	H	H	X	LAST	LAST	X	High-Z	No Write or Read due to Sequential port Deselect. No counter advance.
↑	H	L	X	NEXT	NEXT	X	High-Z	No Write or Read due to Sequential port Deselect. Counter does advance.

3099 tbl 13

NOTES:
1. H = V_{IH}, L = V_{IL}, X = Don't Care, and HIGH-Z = High-impedance. LOW = V_{OL}.
2. $\overline{RST}$, $\overline{SLD}$, $\overline{SSTRT_1}$, $\overline{SSTRT_2}$ are continuously HIGH during a sequential write access, other than pointer access operations.
3. $\overline{CE}$, $\overline{OE}$, R/$\overline{W}$, $\overline{CMD}$, $\overline{LB}$, $\overline{UB}$, and I/O_0-I/O_{15} are unrelated to the sequential port control and operation except for $\overline{CMD}$ which must not be used concurrently with the sequential port operation (due to the counter and register control). $\overline{CMD}$ should be HIGH ($\overline{CMD}$ = V_{IH}) during sequential port access.
4. $\overline{SOE}$ must be HIGH ($\overline{SOE}$=V_{IH}) prior to write conditions only if the previous cycle is a read cycle, since the data being written must be an input at the rising edge of the clock during the cycle in which SR/$\overline{W}$ = V_{IL}.
5. SI/O_{IN} refers to SI/O_0-SI/O_{15} inputs.
6. "LAST" refers to the previous value still being output, no change.
7. Termination of a write is done on the LOW-to-HIGH transition of SCLK if SR/$\overline{W}$ or $\overline{SCE}$ is HIGH.
8. When $\overline{CLKEN}$=LOW, the address is incremented on the next rising edge before any operation takes place. See the diagrams called "Sequential Counter Enable Cycle after Reset, Read (and write) Cycle".

Truth Table: Sequential Address Pointer Operations(1,2,3,4,5)

Inputs/Outputs					MODE
SCLK	SLD	SSTRT1	SSTRT1	SOE	
↑	H	L	H	X	Non-Counter Advanced Sequential Write, without EOB1 or EOB2 reached.
↑	H	H	L	X	Counter Advanced Sequential Write with EOB1 and EOB2 reached.
↑	L	H	H	H(6)	No Write or Read due to Sequential port Deselect. No counter advance.

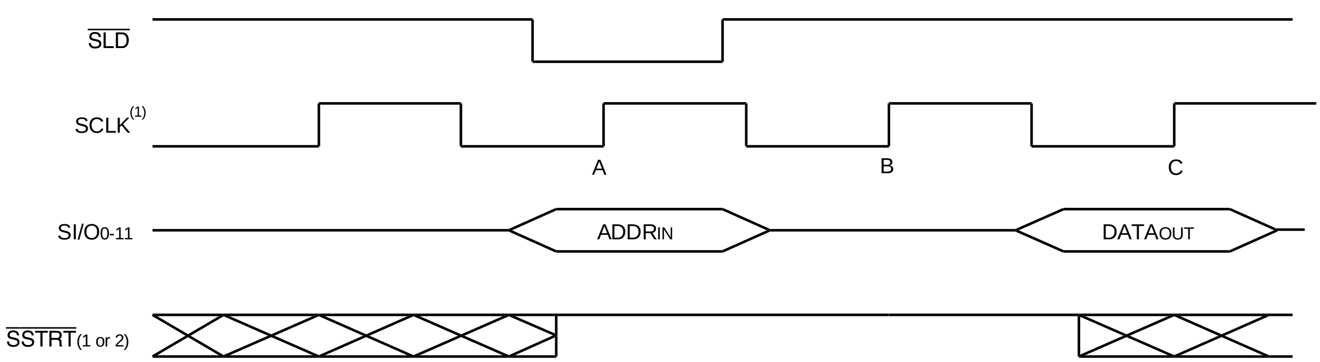
3099 tbl 14

NOTES:
1. H = VIH, L = VIL, X = Don't Care, and High-Z = High-impedance.
2. RST is continuously HIGH. The conditions of SCE CNTEN, and SR/W are unrelated to the sequential address pointer operations.
3. CE, OE, R/W, LB, UB, and I/O0-I/O15 are unrelated to the sequential port control and operation, except for CMD which must not be used concurrently with the sequential port operation (due to the counter and register control). CMD should be HIGH (CMD = VIH) during sequential port access.
4. Address pointer can also change when it reaches an end of buffer address. See Flow Control Bits table.
5. When SLD is sampled LOW, there is an internal delay of one cycle before the address pointer changes. The state of CNTEN is ignored and the address is not incremented during the two cycles.
6. SOE may be LOW with SCE deselect or in the write mode using SR/W.

Address Pointer Load Control (SLD)

In SLD mode, there is an internal delay of one cycle before the address pointer changes in the cycle following SLD. When SLD is LOW, data on the inputs SI/O0-SI/O11 is loaded into a data-in register on the LOW-to-HIGH transition of SCLK. On the cycle following SLD, the address pointer changes to the address location contained in the data-in register. SSTRT1, SSTRT2 may not be low while SLD is LOW, or during the cycle following SLD. The SSTRT1 and SSTRT2 require only one clock cycle, since these addresses are pre-loaded in the registers already.

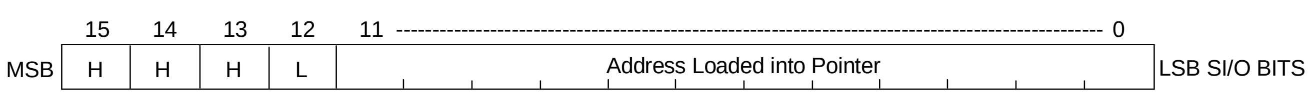
SLD Mode(1)



3099 drw 08

NOTE:
1. At SCLK edge (A), SI/O0-SI/O11 data is loaded into a data-in register. At edge (B), contents of the data-in register are loaded into the address pointer (i.e. address pointer changes). At SCLK edge (A), SSTRT1 and SSTRT2 must be HIGH to ensure for proper sequential address pointer loading. At SCLK edge (B), SLD and SSTRT1,2 must be HIGH to ensure for proper sequential address pointer loading. For SSTRT1 or SSTRT2, the data to be read will be ready for edge (B), while data will not be ready at edge (B) when SLD is used, but will be ready at edge (C).

Sequential Load of Address into Pointer/Counter(1)



3099 drw 09

NOTE:
1. "H" = VIH and "L" = VIL for the SI/O intput state.

Reset ($\overline{RST}$)

Setting $\overline{RST}$ LOW resets the control state of the SARAM. $\overline{RST}$ functions asynchronously of SCLK (i.e. not registered). The default states after a reset operation are displayed in the adjacent chart.

Register	Contents
Address	0
$\overline{EOB}$ Flags	Cleared to HIGH state
Buffer Flow Mode	BUFFER CHAINING
Start Address Buffer #1	0 (1)
End Address Buffer #1	4095 (4K)
Start Address Buffer #2[1]	Cleared (set at invalid points)
End Address Buffer #2[1]	Cleared (set at invalid points)
Registered State	$\overline{SCE}$ = V_{IH}, SR/$\overline{W}$ = V_{IL}

3099 tbl 15

NOTE:
1. Start address and End of address for Buffer #2 and the Flow Control for both Buffer #1 and #2, must be programmed as described in the "Buffer Command Mode" section.

Buffer Command Mode ($\overline{CMD}$)

Buffer Command Mode ($\overline{CMD}$) allows the random access port to control the state of the two buffers. Address pins A_0-A_2 and I/O pins I/O_0-I/O_{11} are used to access the start of buffer and the end of buffer addresses and to set the flow control mode of each buffer. The Buffer Command Mode also allows reading and clearing the status of the $\overline{EOB}$ flags. Seven different $\overline{CMD}$ cases are available depending on the conditions of A_0-A_2 and R/W. Address bits A_3-A_{11} and data I/O bits I/O_{12}-I/O_{15} are not used during this operation.

Random Access Port $\overline{CMD}$ Mode[1]

Case #	A_2-A_0	R/$\overline{W}$	DESCRIPTIONS
1	000	0 (1)	Write (read) the start address of Buffer #1 through I/O_0-I/O_{11}.
2	001	0 (1)	Write (read) the end address of Buffer #1 through I/O_0-I/O_{11}.
3	010	0 (1)	Write (read) the start address of Buffer #2 through I/O_0-I/O_{11}.
4	011	0 (1)	Write (read) the end address of Buffer #2 through I/O_0-I/O_{11}.
5	100	0 (1)	Write (read) flow control register.
6	101	0	Write only - clear $\overline{EOB_1}$ and/or $\overline{EOB_2}$ flag.
7	101	1	Read only - flag status register.
8	110/111	(X)	(Reserved)

3099 tbl 16

NOTE:
1. R/$\overline{W}$ input "0(1)" indicates a write(0) or read(1) occurring with the same address input.

Cases 1 through 4: Start and End of Buffer Register Description[1,2]

	15	14	13	12	11 ------------------------------------ 0	
MSB	H	H	H	L	Address Loaded into Buffer	LSB I/O BITS

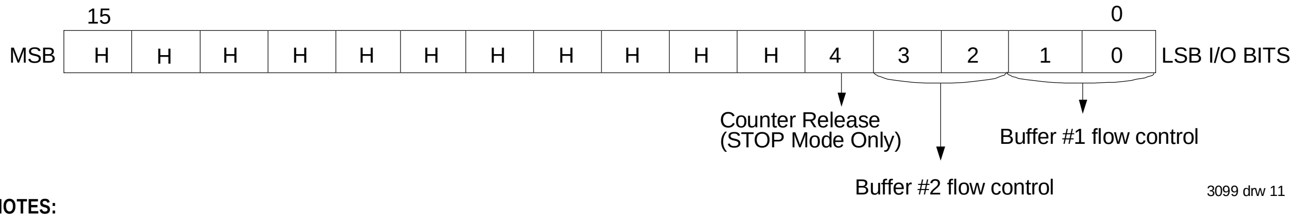
3099 drw 10

NOTES:
1. "H" = V_{OH} for I/O in the output state and "Don't Cares" for I/O in the input state. "L" = V_{IL} for I/O in the input state.
2. A write into the buffer occurs when R/$\overline{W}$ = V_{IL} and a read when R/$\overline{W}$ = V_{IH}. $\overline{EOB_1}$/$\overline{SOB_1}$ and $\overline{EOB_2}$/$\overline{SOB_2}$ are chosen through address A_0-A_2 while $\overline{CMD}$ = V_{IL} and $\overline{CE}$ = V_{IH}.

Case 5: Buffer Flow Modes

Within the SARAM, the user can designate one of two buffer flow modes for each buffer. Each buffer flow mode defines a unique set of actions for the sequential port address pointer and $\overline{EOB}$ flags. In BUFFER CHAINING mode, after the address pointer reaches the end of the buffer, it sets the corresponding $\overline{EOB}$ flag and continues from the start address of the other buffer. In STOP mode, the address pointer stops incrementing after it reaches the end of the buffer. There is no linear or mask mode available.

Flow Control Register Description[1,2]



NOTES:
1. "H" = V_{OH} for I/O in the output state and "Don't Cares"' for I/O in the input state.
2. Writing a 0 into bit 4 releases the address pointer after it is stopped due to the STOP mode and allows sequential write operations to resume. This occurs asynchronously of SCLK, and therefore caution should be taken. The pointer will be at address EOB+2 on the next rising edge of SCLK that is enabled by CNTEN. The pointer is also released by RST, SLD, SSTRT1 and SSTRT2 operations.

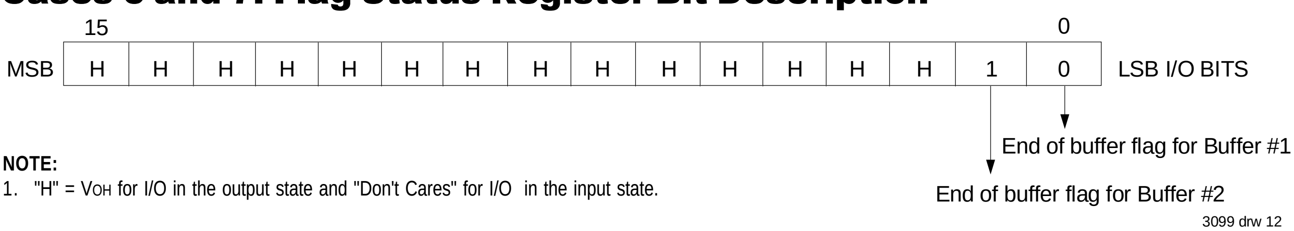
Flow Control Bits[5]

Flow Control		Functional Description
Bit 1 & Bit 0 (Bit 3 & Bit 2)	Mode	
00	BUFFER CHAINING	EOB1 (EOB2) is asserted (Active LOW output) when the pointer matches the end address of Buffer #1 (Buffer #2). The pointer value is changed to the start address of Buffer #2 (Buffer #1)[1,3]
01	STOP	EOB1 (EOB2) is asserted when the pointer matches the end address of Butler #1 (Butler #2). The address pointer will stop incrementing when it reaches the next address (EOB address + 1), if CNTEN is LOW on the next clock's rising edge. Otherwise, the address pointer will stop incrementing on EOB. Sequential write operations are inhibited after the address pointer is stopped. The pointer can be released by bit 4 of the flow control register.[1,2,4]

3099 tbl 17

NOTES:
1. EOB1 and EOB2 may be asserted (set) at the same time, if both end addresses have been loaded with the same value.
2. CMD flow control bits are unchanged, the count does not continue advancement.
3. If EOB1 and EOB2 are equal, then the pointer will jump to the start of Buffer #1.
4. If the counter has stopped at EOBx and was released by bit 4 of the flow control register, CNTEN must be LOW on the next rising edge of SCLK; otherwise the flow control will remain in the stop mode.
5. Flow Control Bit settings of '10' and '11' are reserved.
6. Start address and End of address for Buffer #2 and the Flow Control for both Buffer #1 and #2, must be programmed as described in the "Buffer Command Mode" section. RST conditions are not set to valid addresses.

Cases 6 and 7: Flag Status Register Bit Description[1]



NOTE:
1. "H" = V_{OH} for I/O in the output state and "Don't Cares" for I/O in the input state.

Cases 6: Flag Status Register Write Conditions[1]

Flag Status Bit 0, (Bit 1)	Functional Description
0	Clears Buffer Flag EOB1, (EOB2).
1	No change to the Buffer Flag.[2]

3099 tbl 18

NOTES:
1. Either bit 0 or bit 1, or both bits, may be changed simultaneously. One may be cleared while the second is left alone, or both may be cleared.
2. Remains as it was prior to the CMD operation, either HIGH (1) or LOW (0).

Case 7: Flag Status Register Read Conditions

Flag Status Bit 0, (Bit 1)	Functional Description
0	EOB1 (EOB2) flag has not been set, the Pointer has not reached the End of the Buffer.
1	EOB1 (EOB2) flag has been set, the Pointer has reached the end of the Buffer.

3099 tbl 19

Cases 8 and 9: (Reserved)

Illegal operations. All outputs will be HIGH on the I/O bus during a READ.

Random Access Port: AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(2,4,5)

Symbol	Parameter	70824X20 Com'l Only		70824X25 Com'l Only		70824X35 Com'l & Military		70824X45 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	20	—	25	—	35	—	45	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	—	45	ns
t_{ACE}	Chip Enable Access Time	—	20	—	25	—	35	—	45	ns
t_{BE}	Byte Enable Access Time	—	20	—	25	—	35	—	45	ns
t_{OE}	Output Enable Access Time	—	10	—	10	—	15	—	20	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{CLZ}	Chip Select Low-Z Time(1)	3	—	3	—	3	—	3	—	ns
t_{BLZ}	Byte Select Low-Z Time(1)	3	—	3	—	3	—	3	—	ns
t_{OLZ}	Output Enable Low-Z Time(1)	2	—	2	—	2	—	2	—	ns
t_{CHZ}	Chip Select High-Z Time(1)	—	10	—	12	—	15	—	15	ns
t_{BHZ}	Byte Select High-Z Time(1)	—	10	—	12	—	15	—	15	ns
t_{OHZ}	Output Select High-Z Time(1)	—	9	—	11	—	15	—	15	ns
t_{PU}	Chip Select Power-Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Select Power-Down Time	—	20	—	25	—	35	—	45	ns

3099 tbl 20

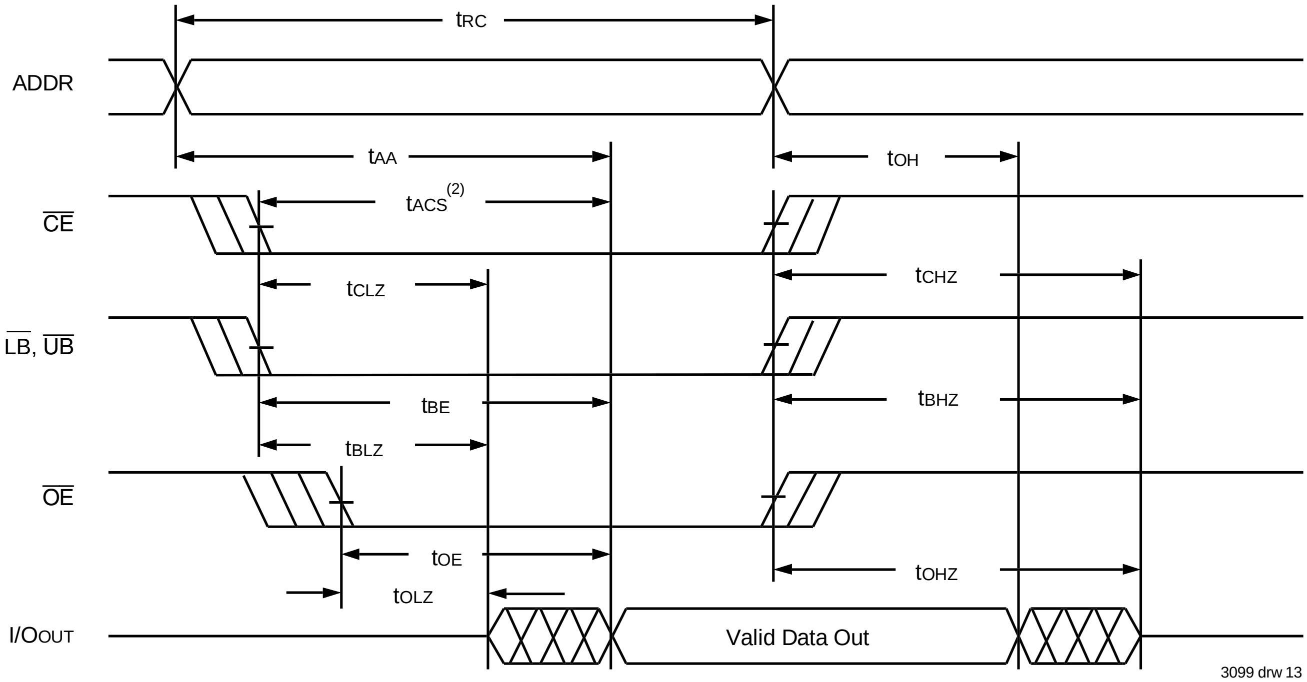
Random Access Port: AC Electrical Characteristics Over the Operating Temperature and Supply Voltage(2,4,5)

Symbol	Parameter	70824X20 Com'l Only		70824X25 Com'l Only		70824X35 Com'l & Military		70824X45 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
t_{WC}	Write Cycle Time	20	—	25	—	35	—	45	—	ns
t_{CW}	Chip Enable to End-of-Write	15	—	20	—	25	—	30	—	ns
t_{AW}	Address Valid to End-of-Write(3)	15	—	20	—	25	—	30	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width(3)	13	—	20	—	25	—	30	—	ns
t_{BP}	Byte Enable Pulse Width(3)	15	—	20	—	25	—	30	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}	Write Enable Output High-Z Time(1)	—	10	—	12	—	15	—	15	ns
t_{DW}	Data Set-up Time	13	—	15	—	20	—	25	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{OW}	Output Active from End-of-Write	3	—	3	—	3	—	3	—	ns

3099 tbl 21

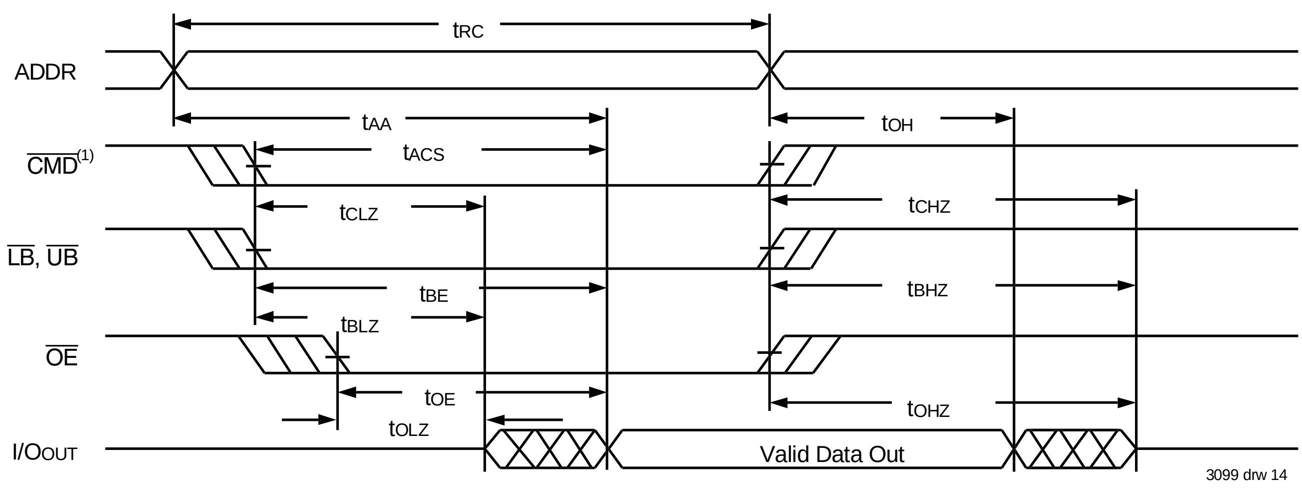
NOTES:
1. Transition measured at 0mV from steady state. This parameter is guaranteed with the AC Output Test Load (Figure 1) by device characterization, but is not production tested.
2. 'X' in part number indicates power rating (S or L).
3. $\overline{OE}$ is continuously HIGH, $\overline{OE}$ = V_{IH}. If during the R/$\overline{W}$ controlled write cycle the $\overline{OE}$ is LOW, t_{WP} must be greater or equal to t_{WHZ} + t_{DW} to allow the I/O drivers to turn off and on the data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during the R/$\overline{W}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP}. For the $\overline{CE}$ controlled write cycle, $\overline{OE}$ may be LOW with no degradation to t_{CW} timing.
4. $\overline{CMD}$ access follows standard timing listed for both read and write accesses, ($\overline{CE}$ = V_{IH} when $\overline{CMD}$ = V_{IL}) or ($\overline{CMD}$ = V_{IH} when $\overline{CE}$ = V_{IL}).
5. Industrial temperature: for specific speeds, packages and powers contact your sales office.

Waveform of Read Cycles: Random Access Port[1,2]



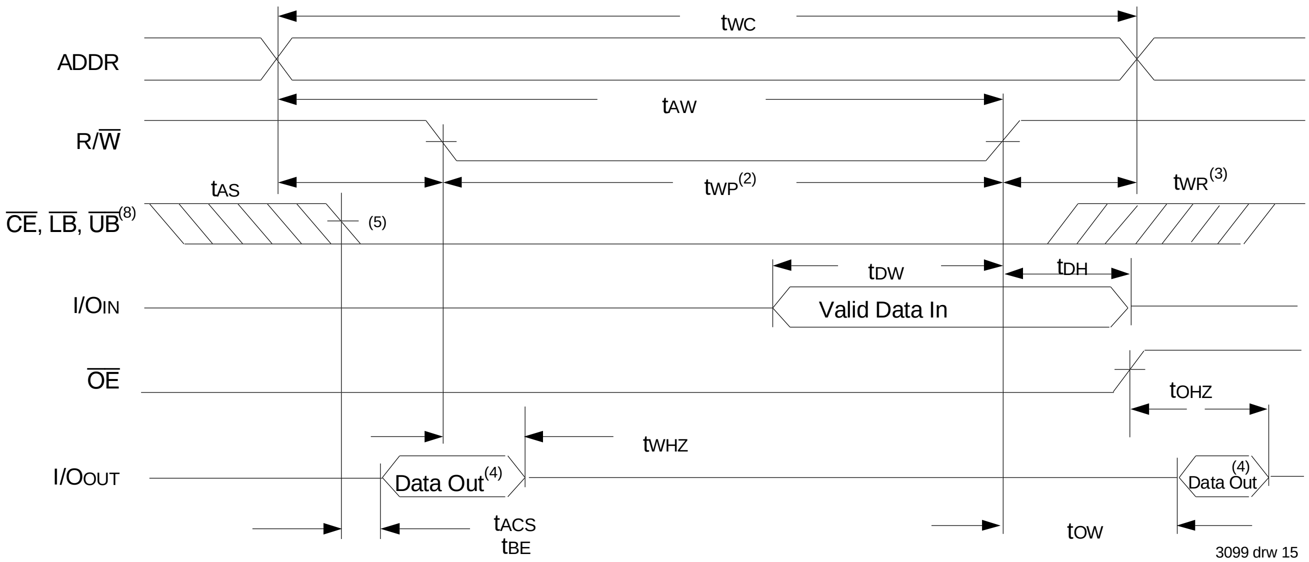
NOTES:
1. R/W̄ is HIGH for read cycle.
2. Address valid prior to or coincident with CE̅ transition LOW; otherwise t_{AA} is the limiting parameter.

Waveform of Read Cycles: Buffer Command Mode

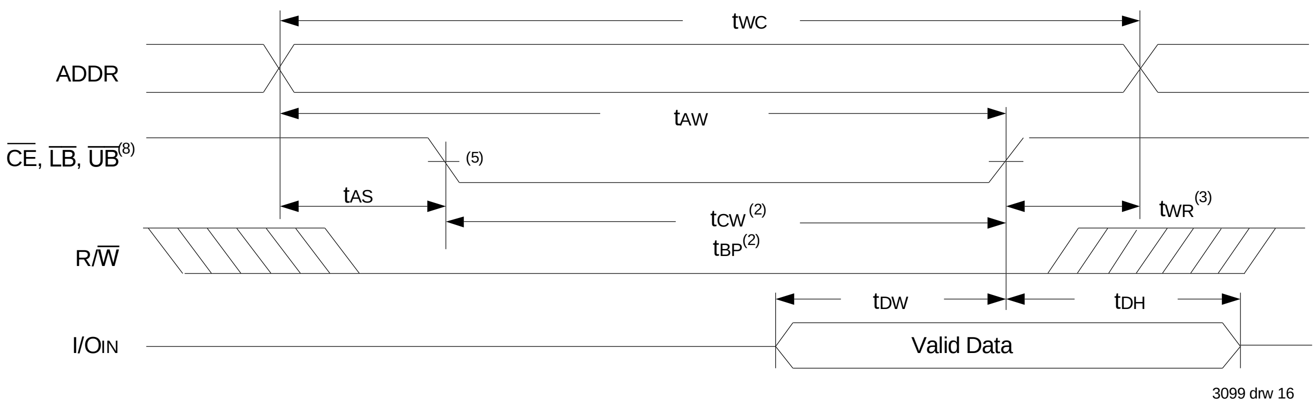


NOTE:
1. CE̅ = V_{IH} when CMD̅ = V_{IL}.

Waveform of Write Cycle No.1 (R/$\overline{W}$ Controlled Timing) Random Access Port[1,6]



Waveform of Write Cycle No.2 ($\overline{CE}$, $\overline{LB}$, and/or $\overline{UB}$ Controlled Timing) Random Access Port[1,6,7]



NOTES:

1. R/$\overline{W}$, $\overline{CE}$, or $\overline{LB}$ and $\overline{UB}$ must be inactive during all address transitions.
2. A write occurs during the overlap of R/$\overline{W}$ = V_{IL}, $\overline{CE}$ = V_{IL} and $\overline{LB}$ = V_{IL} and/or $\overline{UB}$ = V_{IL}.
3. t_{WR} is measured from the earlier of $\overline{CE}$ (and $\overline{LB}$ and/or $\overline{UB}$) or R/$\overline{W}$ going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state and the input signals must not be applied.
5. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the High-impedance state.
6. $\overline{OE}$ is continuously HIGH, $\overline{OE}$ = V_{IH}. If during the R/$\overline{W}$ controlled write cycle the $\overline{OE}$ is LOW, t_{WP} must be greater or equal to t_{WHZ} + t_{DW} to allow the I/O drivers to turn off and on the data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during the R/$\overline{W}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP}. For the $\overline{CE}$ controlled write cycle, $\overline{OE}$ may be LOW with no degregation to t_{CW} timing.
7. I/O_{OUT} is never enabled, therefore the output is in High-Z state during the entire write cycle.
8. $\overline{CMD}$ access follows the standard $\overline{CE}$ access described above. If $\overline{CMD}$ = V_{IL}, then $\overline{CE}$ must = V_{IH} or, when $\overline{CE}$ = V_{IL}, $\overline{CMD}$ must = V_{IH}.

Sequential Port: AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1,3)

Symbol	Parameter	70824X20 Com'l Only		70824X25 Com'l Only		70824X35 Com'l & Military		70824X45 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{CYC}	Sequential Clock Cycle Time	25	—	30	—	40	—	50	—	ns
t_{CH}	Clock Pulse HIGH	10	—	12	—	15	—	18	—	ns
t_{CL}	Clock Pulse LOW	10	—	12	—	15	—	18	—	ns
t_{ES}	Count Enable and Address Pointer Set-up Time	5	—	5	—	6	—	6	—	ns
t_{EH}	Count Enable and Address Pointer Hold Time	2	—	2	—	2	—	2	—	ns
t_{SOE}	Output Enable to Data Valid	—	8	—	10	—	15	—	20	ns
t_{OLZ}	Output Enable Low-Z Time(2)	2	—	2	—	2	—	2	—	ns
t_{OHZ}	Output Enable High-Z Time(2)	—	9	—	11	—	15	—	15	ns
t_{CD}	Clock to Valid Data	—	20	—	25	—	35	—	45	ns
t_{CKHZ}	Clock High-Z Time(2)	—	12	—	14	—	17	—	20	ns
t_{CKLZ}	Clock Low-Z Time(2)	3	—	3	—	3	—	3	—	ns
t_{EB}	Clock to $\overline{EOB}$	—	13	—	15	—	18	—	23	ns

3099 tbl 22

Sequential Port: AC Electrical Characteristics Over the Operating Temperature and Supply Voltage(1,3)

Symbol	Parameter	70824X20 Com'l Only		70824X25 Com'l Only		70824X35 Com'l & Military		70824X45 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
t_{CYC}	Sequential Clock Cycle Time	25	—	30	—	40	—	50	—	ns
t_{FS}	Flow Restart Time	13	—	15	—	20	—	20	—	ns
t_{WS}	Chip Select and Read/Write Set-up Time	5	—	5	—	6	—	6	—	ns
t_{WH}	Chip Select and Read/Write Hold Time	2	—	2	—	2	—	2	—	ns
t_{DS}	Input Data Set-up Time	5	—	5	—	6	—	6	—	ns
t_{DH}	Input Data Hold Time	2	—	2	—	2	—	2	—	ns

3099 tbl 23

NOTES:
1. 'X' in part number indicates power rating (S or L).
2. Transition measured at 0mV from steady state. This parameter is guaranteed with the AC Output Test Load (Figure 1) by device characterization, but is not production tested.
3. Industrial temperature: for specific speeds, packages and powers contact your sales office.

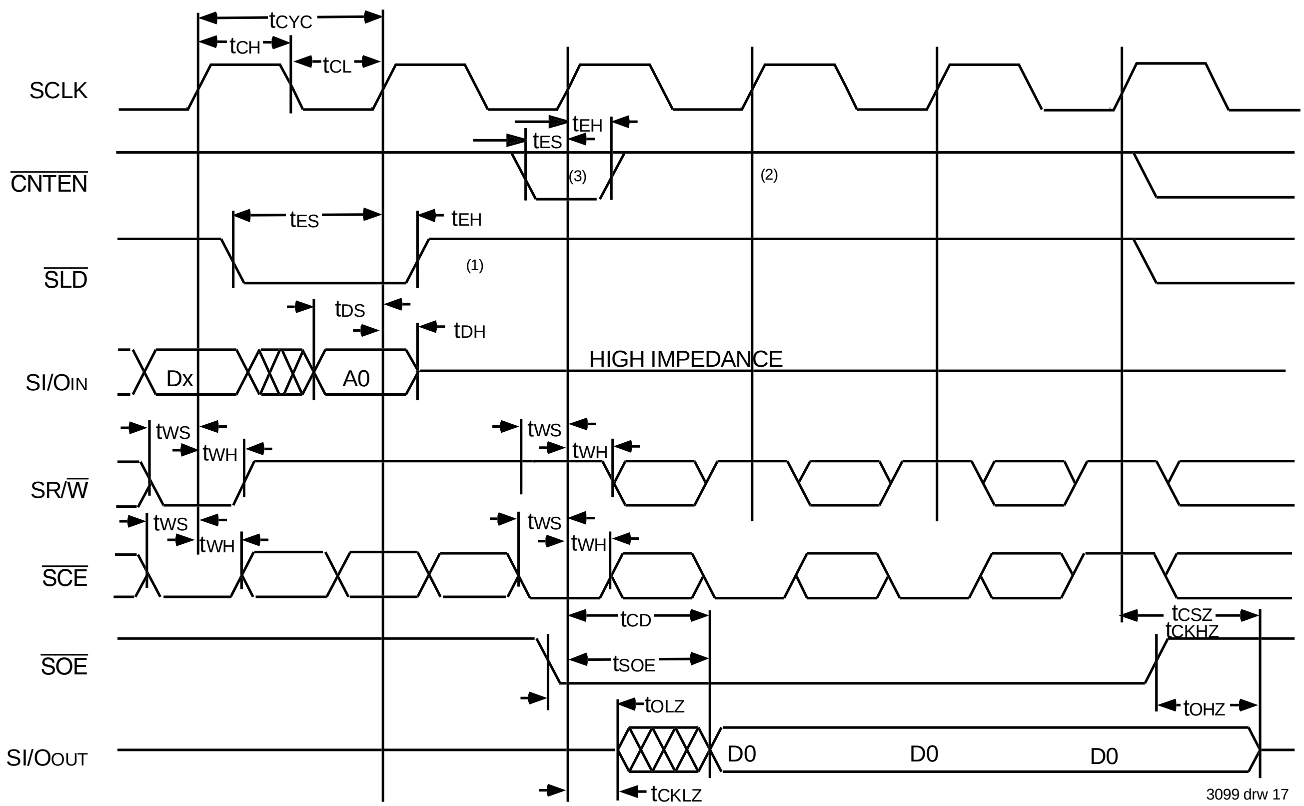
Sequential Port: AC Electrical Characteristics Over the Operating Temperature and Supply Voltage(1,2)

Symbol	Parameter	70824X20 Com'l Only		70824X25 Com'l Only		70824X35 Com'l & Military		70824X45 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
t_{RSPW}	Reset Pulse Width	13	—	15	—	20	—	20	—	ns
t_{WERS}	Write Enable HIGH to Reset HIGH	10	—	10	—	10	—	10	—	ns
t_{RSRC}	Reset HIGH to Write Enable LOW	10	—	10	—	10	—	10	—	ns
t_{RSFV}	Reset HIGH to Flag Valid	15	—	20	—	25	—	25	—	ns

3099 tbl 24

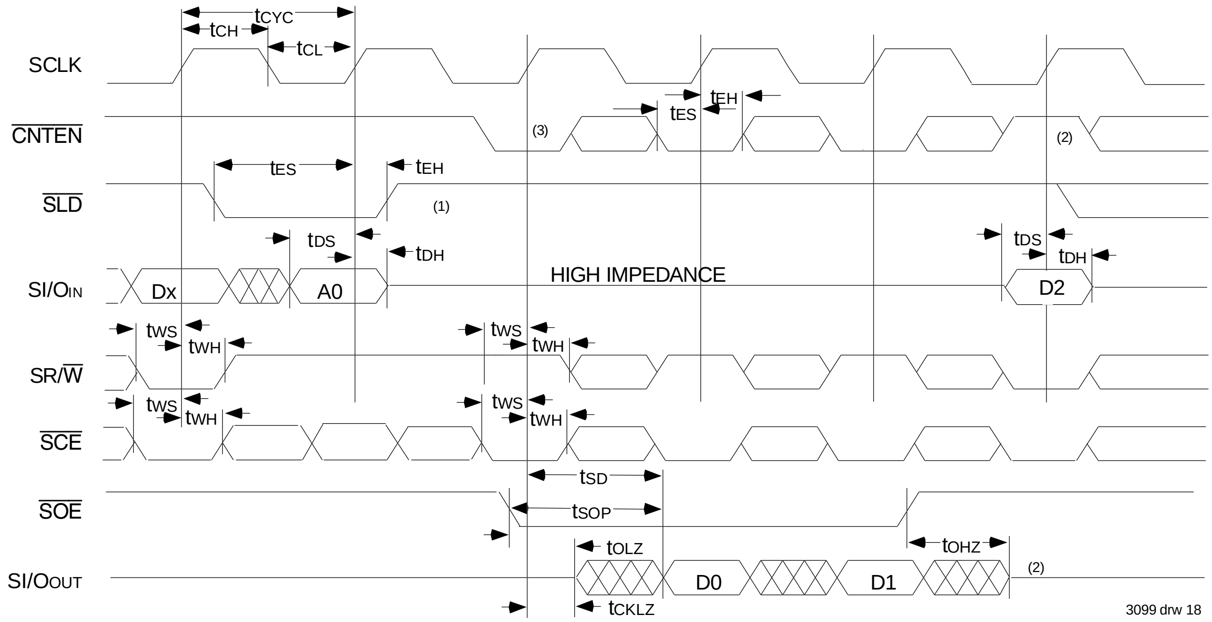
NOTES:
1. 'X' in part numbers indicates power rating (S or L).
2. Industrial temperature: for specific speeds, packages and powers contact your sales office.

Sequential Port: Write, Pointer Load Non-Incrementing Read



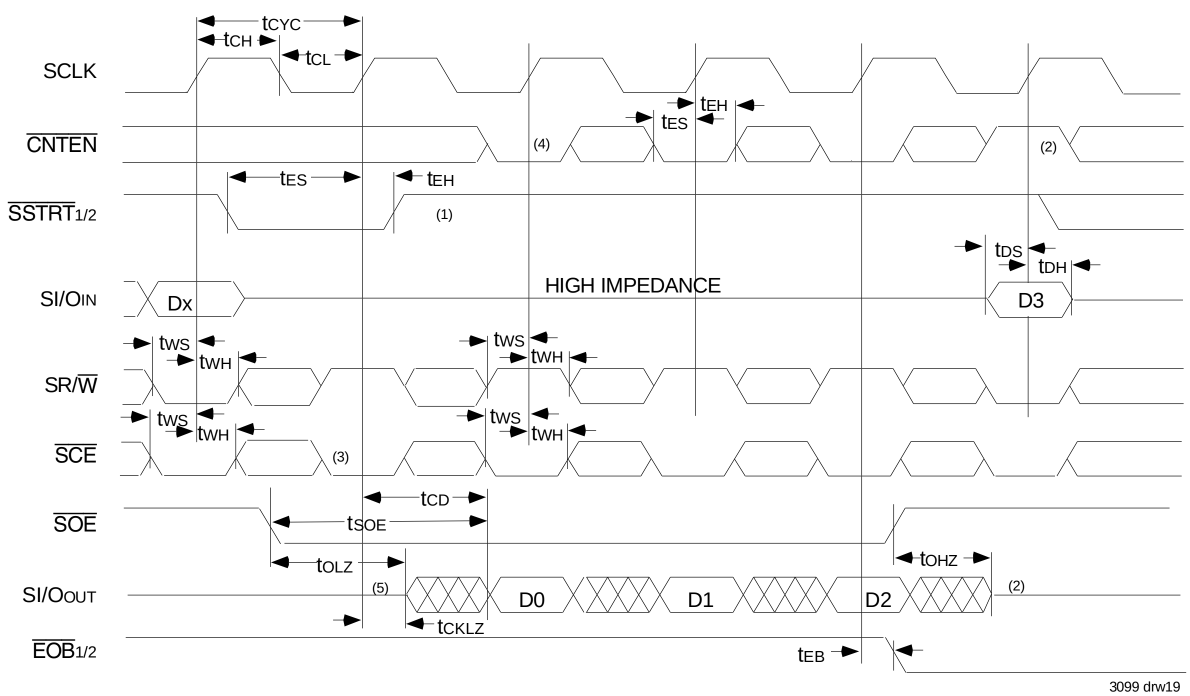
NOTES:
1. If SLD = V_{IL}, then address will be clocked in on the SCLK's rising edge.
2. If CNTEN = V_{IH} for the SCLK's rising edge, the internal address counter will not advance.
3. Pointer is not incremented on cycle immediately following SLD even if CNTEN is LOW.

Sequential Port: Write, Pointer Load, Burst Read



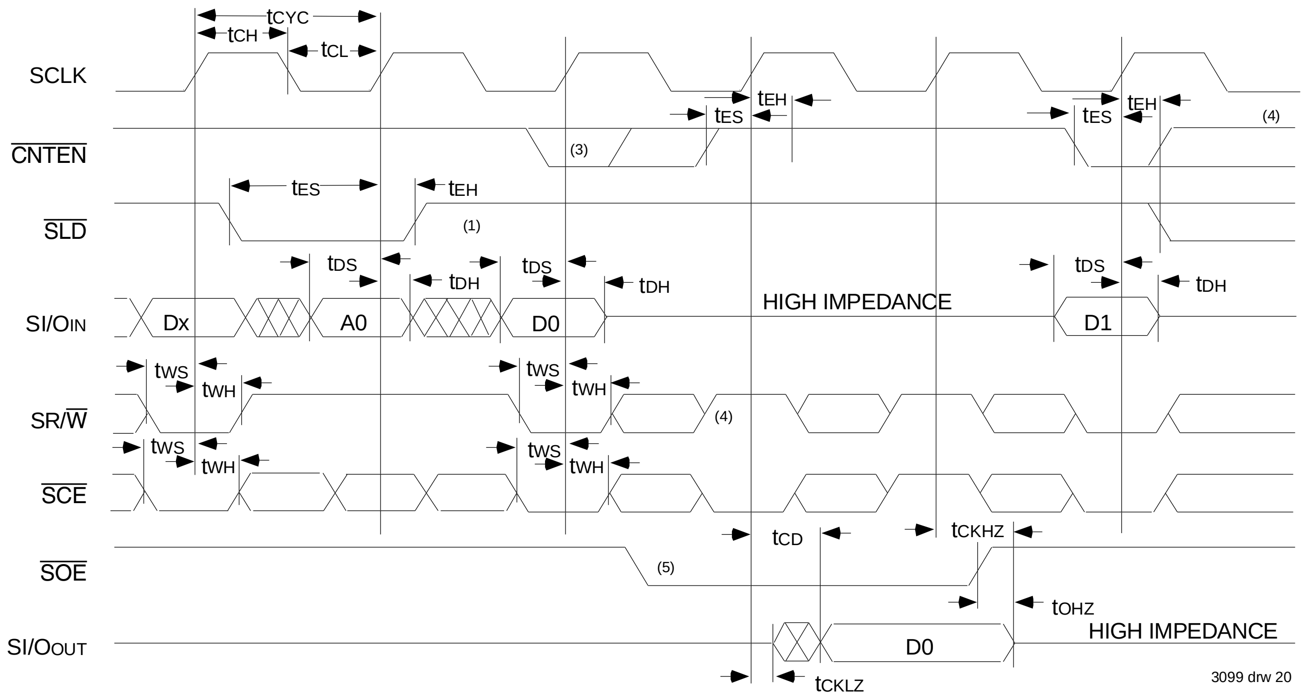
NOTES:
1. If $\overline{SLD}$ = V_{IL}, then address will be clocked in on the SCLK's rising edge.
2. If $\overline{CNTEN}$ = V_{IH} for the SCLK's rising edge, the internal address counter will not advance.
3. Pointer is not incremented on cycle immediately following $\overline{SLD}$ even if $\overline{CNTEN}$ is LOW.

Read $\overline{STRT}$/$\overline{EOB}$ Flag Timing - Sequential Port

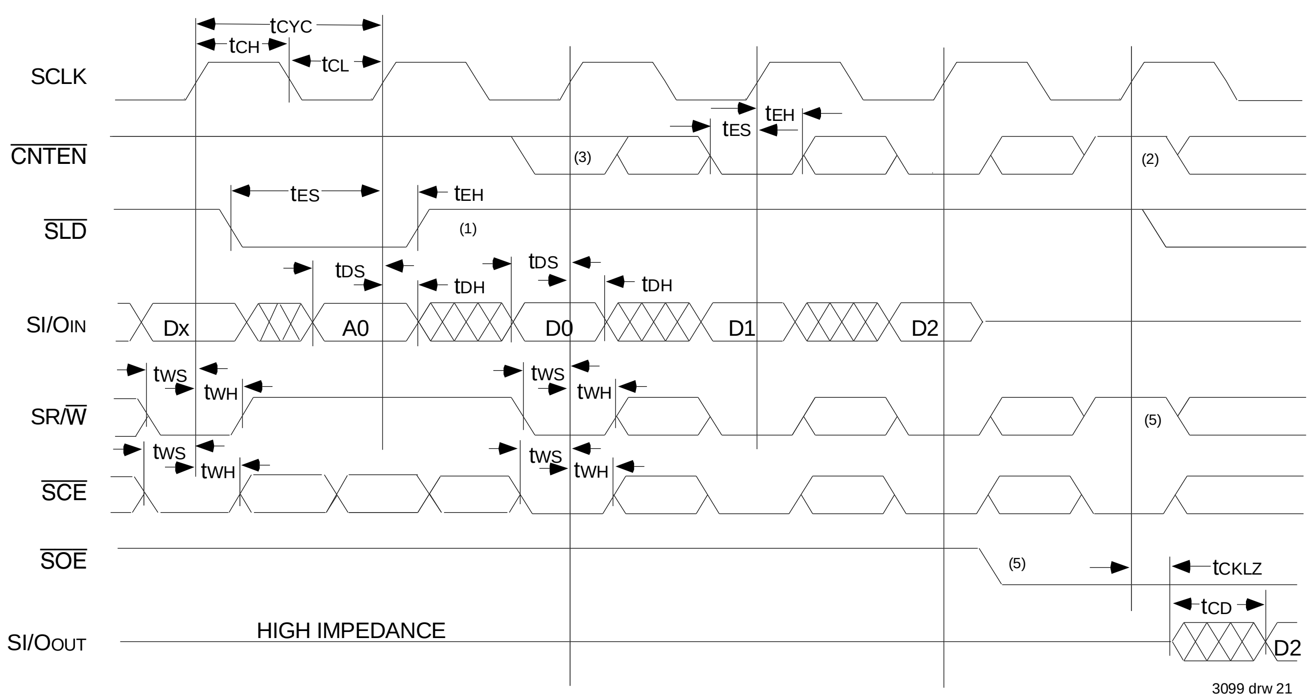


NOTES: (Also used in Figure "Read $\overline{STRT}$/$\overline{EOB}$ Flag Timing")
1. If $\overline{SSTRT_1}$ or $\overline{SSTRT_2}$ = V_{IL}, then address will be clocked in on the SCLK's rising edge.
2. If $\overline{CNTEN}$ = V_{IH} for the SCLK's rising edge, the internal address counter will not advance.
3. $\overline{SOE}$ will control the output and should be HIGH on power-up. If $\overline{SCE}$ = V_{IL} and is clocked in while SR/$\overline{W}$ = V_{IH}, the data addressed will be read out within that cycle. If $\overline{SCE}$ = V_{IL} and is clocked in while SR/$\overline{W}$ = V_{IL}, the data addressed will be written to if the last cycle was a read. $\overline{SOE}$ may be used to control the bus contention and permit a write on this cycle.
4. Unlike $\overline{SLD}$ case, $\overline{CNTEN}$ is not disabled on cycle immediately following $\overline{SSTRT}$.
5. If SR/$\overline{W}$ = V_{IL}, data would be written to D_0 again since $\overline{CNTEN}$ = V_{IH}.
6. $\overline{SOE}$ = V_{IL} makes no difference at this point since the SR/$\overline{W}$ = V_{IL} disables the output until SR/$\overline{W}$ = V_{IH} is clocked in on the next rising clock edge.

Waveform of Write Cycles: Sequential Port



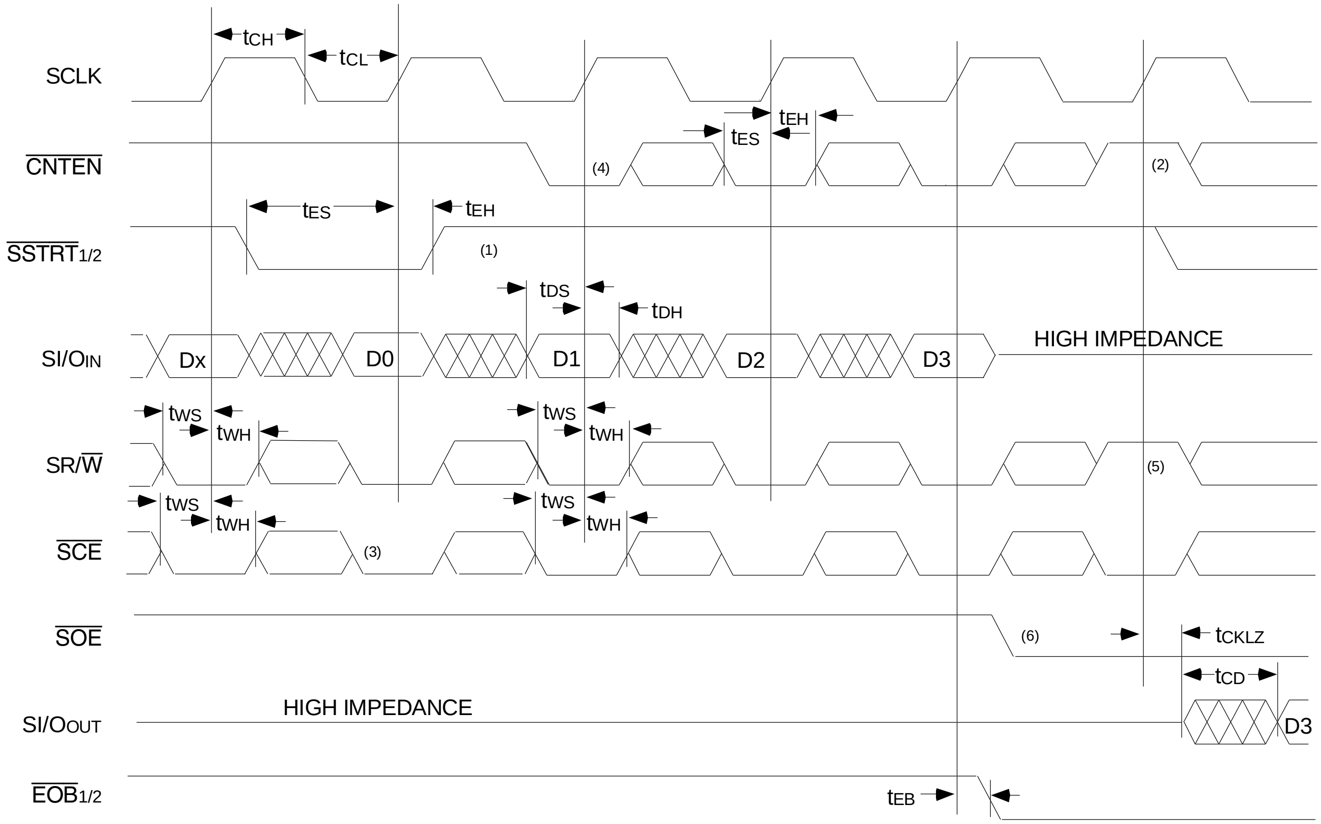
Waveform of Burst Write Cycles: Sequential Port



NOTES:

1. If $\overline{\text{SLD}}$ = V_{IL}, then address will be clocked in on the SCLK's rising edge.
2. If $\overline{\text{CNTEN}}$ = V_{IH} for the SCLK's rising edge, the internal address counter will not advance.
3. Pointer is not incrementing on cycle immediately following $\overline{\text{SLD}}$ even if $\overline{\text{CNTEN}}$ is LOW.
4. If SR/$\overline{\text{W}}$ = V_{IL}, data would be written to D_0 again since $\overline{\text{CNTEN}}$ = V_{IH}.
5. $\overline{\text{SOE}}$ = V_{IL} makes no difference at this point since the SR/$\overline{\text{W}}$ = V_{IL} disables the output until SR/$\overline{\text{W}}$ = V_{IH} is clocked in on the next rising clock edge.

Waveform of Write Cycles: Sequential Port (STRT/EOB Flag Timing)



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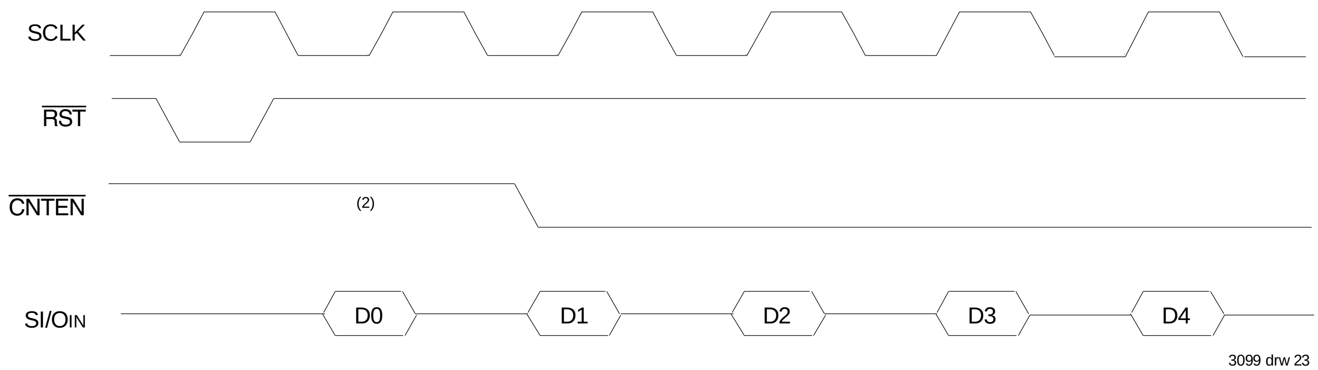
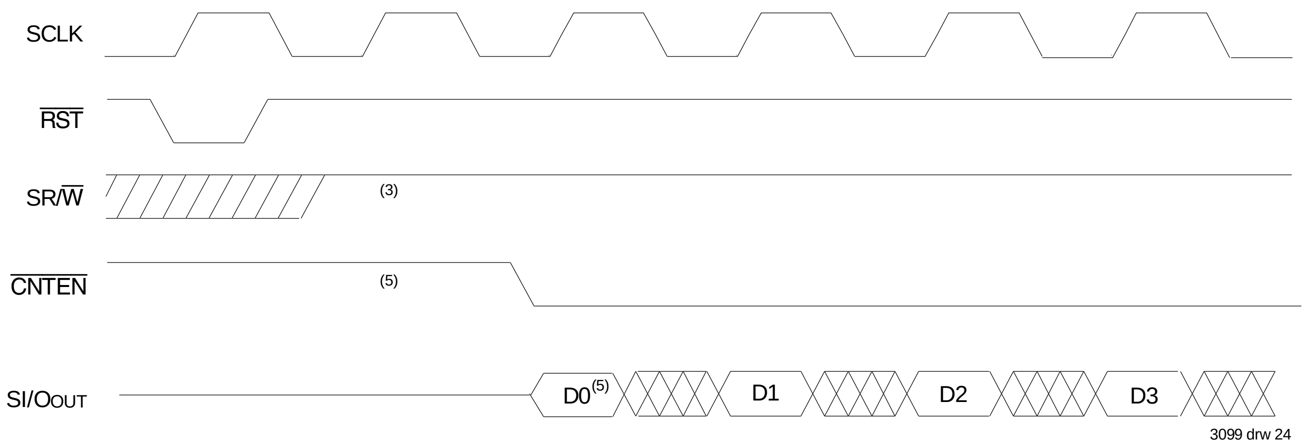
NOTES: (Also used in Figure "Read STRT/EOB Flag Timing")

1. If SSTRT1 or SSTRT2 = VIL, then address will be clocked in on the SCLK's rising edge.
2. If CNTEN = VIH for the SCLK's rising edge, the internal address counter will not advance.
3. SOE will control the output and should be HIGH on power-up. If SCE = VIL and is clocked in while SR/W = VIH, the data addressed will be read out within that cycle. If SCE = VIL and is clocked in while SR/W = VIL, the data addressed will be written to if the last cycle was a read. SOE may be used to control the bus contention and permit a write on this cycle.
4. Unlike SLD case, CNTEN is not disabled on cycle immediately following SSTRT.
5. If SR/W = VIL, data would be written to D0 again since CNTEN = VIH.
6. SOE = VIL makes no difference at this point since the SR/W = VIL disables the output until SR/W = VIH is clocked in on the next rising clock edge.

Sequential Counter Enable Cycle After Reset, Write Cycle(1,4,6)

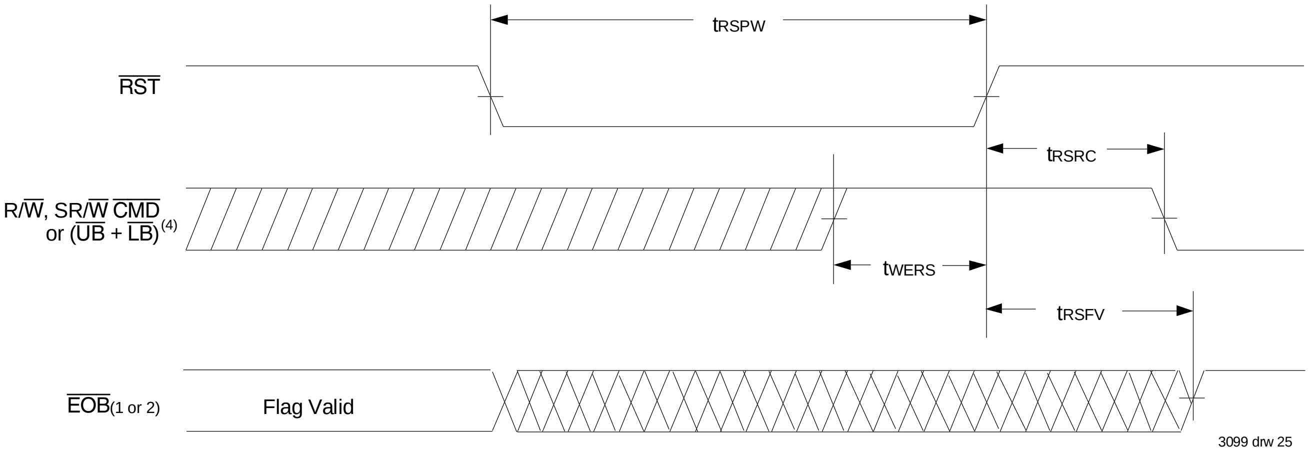


Sequential Counter Enable Cycle After Reset, Read Cycle(1,4)

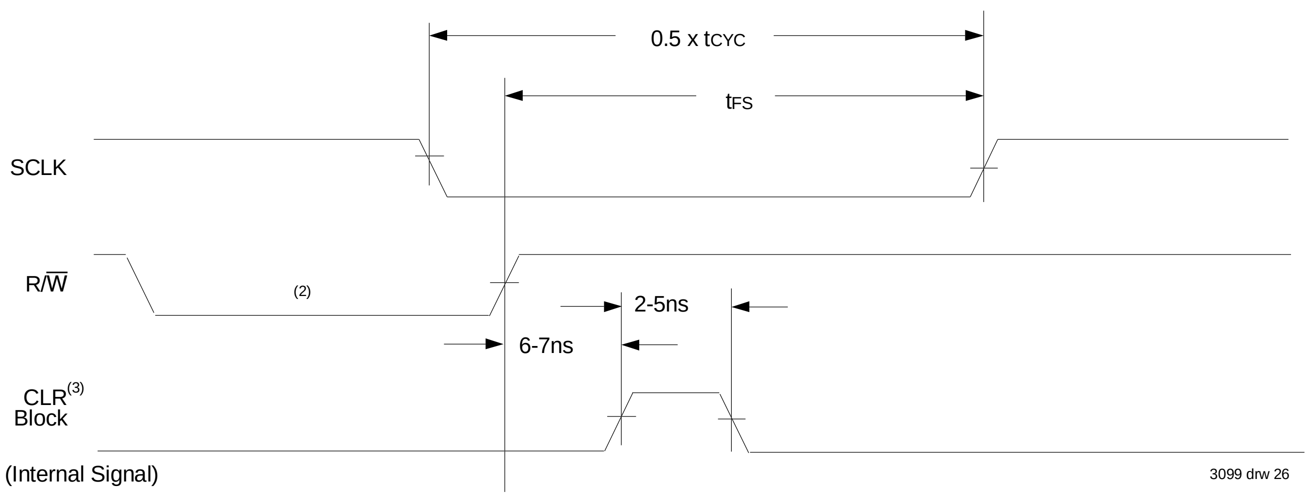


NOTES:
1. 'D0' represents data input for Address = 0, 'D1' represents data input for Address = 1, etc.
2. If $\overline{CNTEN}$ = V_{IL} then 'D1' would be written into 'A1' at this point.
3. Data output is available at a t_{CD} after the SR/$\overline{W}$ = V_{IH} is clocked. The $\overline{RST}$ sets SR/$\overline{W}$ = LOW internally and therefore disables the output until the next clock.
4. $\overline{SCE}$ = V_{IL} throughout all cycles.
5. If $\overline{CNTEN}$=V_{IL} then 'D1' would be clocked out (read) at this point.
6. SR/$\overline{W}$ = V_{IL}.

Random Access Port - Reset Timing



Random Access Port Restart Timing of Sequential Port[1]



NOTES:

1. The sequential port is in the STOP mode and is being restarted from the random port by the Bit 4 Counter Release (see Case 5).
2. "0" is written to Bit 4 from the random port at address [A_2 - A_0] = 100, when $\overline{CMD}$ = V_{IL} and $\overline{CE}$ = V_{IH}. The device is in the Buffer Command Mode (see Case 5).
3. CLR is an internal signal only and is shown for reference only.
4. Sequential port must also prohibit SR/$\overline{W}$ or $\overline{SCE}$ from being LOW for t_{WERS} and t_{RSRC} periods or SCLK must not toggle from LOW-to-HIGH until after t_{RSRC}.

Ordering Information

IDT 70824 X XX X X

Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	I[(1)]	Industrial (-40°C to +85°C)
	B	Military (–55°C to +125°C) Compliant to MIL-PRF-38535 QML
Package	G	84-pin PGA (G84-3)
	PF	80-pin TQFP (PN80-1)
Speed (Speed in nanoseconds)	20	Commercial Only
	25	Commercial Only
	35	Commercial & Military
	45	Commercial & Military
Power	S	Standard Power
	L	Low Power
Device Type	70824	64K (4K x 16) Sequential Access Random Access Memory

3099 drw 27

NOTE:
1. Industrial temperature range is available on selected TQFP packages in standard power. For specific speeds, packages and powers contact your sales office.

Datasheet Document History

3/8/99: Initiated datasheet document history
Converted to new format
Cosmetic and typographical corrections
Page 2 Added additional notes to pin configurations
6/4/99: Changed drawing format
11/10/99: Replaced IDT logo
4/18/00: Page 3 Added "Outputs" in Sequential pin description table
Changed ±200mV to 0mV in notes

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