



Integrated Device Technology, Inc.

HIGH-SPEED 8K x 16 SEQUENTIAL ACCESS RANDOM ACCESS MEMORY (SARAM™)

IDT70825S/L

FEATURES:

- 8K x 16 Sequential Access Random Access Memory (SARAM™)
 - Sequential Access from one port and standard Random Access from the other port
 - Separate upper-byte and lower-byte control of the Random Access Port
- High-speed operation
 - 20ns tAA for random access port
 - 20ns tCD for sequential port
 - 25ns clock cycle time
- Architecture based on Dual-Port RAM cells
- Electrostatic discharge ≥ 2001V, Class II
- Compatible with Intel BMIC and 82430 PCI Set
- Width and Depth Expandable
- Sequential side
 - Address based flags for buffer control
 - Pointer logic supports two internal buffers
- Battery backup operation—2V data retention
- TTL-compatible, single 5V (±10%) power supply
- Available in 80-pin TQFP and 84-pin PGA
- Military product compliant to MIL-STD-883.
- Industrial temperature range (−40°C to +85°C) is available, tested to military electrical specifications.

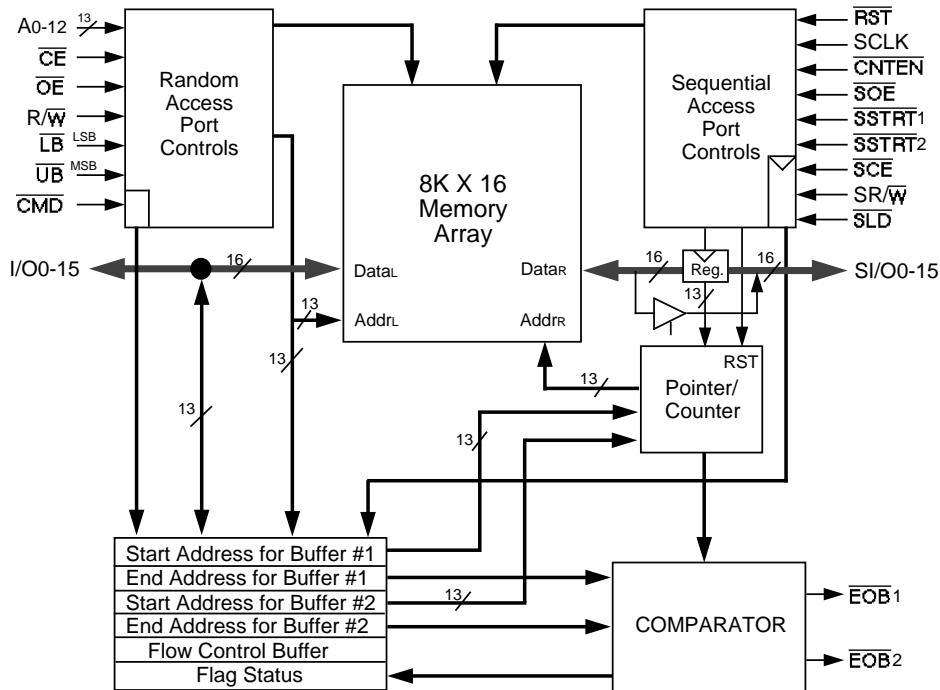
DESCRIPTION:

The IDT70825 is a high-speed 8K x 16-bit Sequential Access Random Access Memory (SARAM). The SARAM offers a single-chip solution to buffer data sequentially on one port, and be accessed randomly (asynchronously) through the other port. The device has a Dual-Port RAM based architecture with a standard SRAM interface for the random (asynchronous) access port, and a clocked interface with counter sequencing for the sequential (synchronous) access port.

Fabricated using CMOS high-performance technology, this memory device typically operates on less than 900mW of power at maximum high-speed clock-to-data and Random Access. An automatic power down feature, controlled by \overline{CE} , permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT70825 is packaged in a 80-pin Thin Plastic Quad Flatpack (TQFP) or 84-pin Ceramic Pin Grid Array (PGA). Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



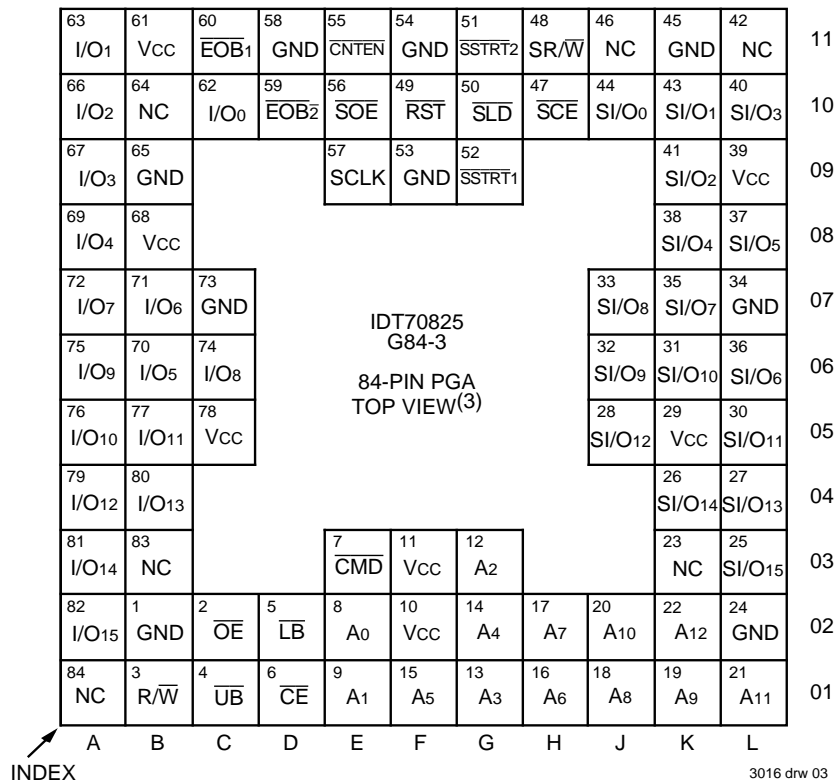
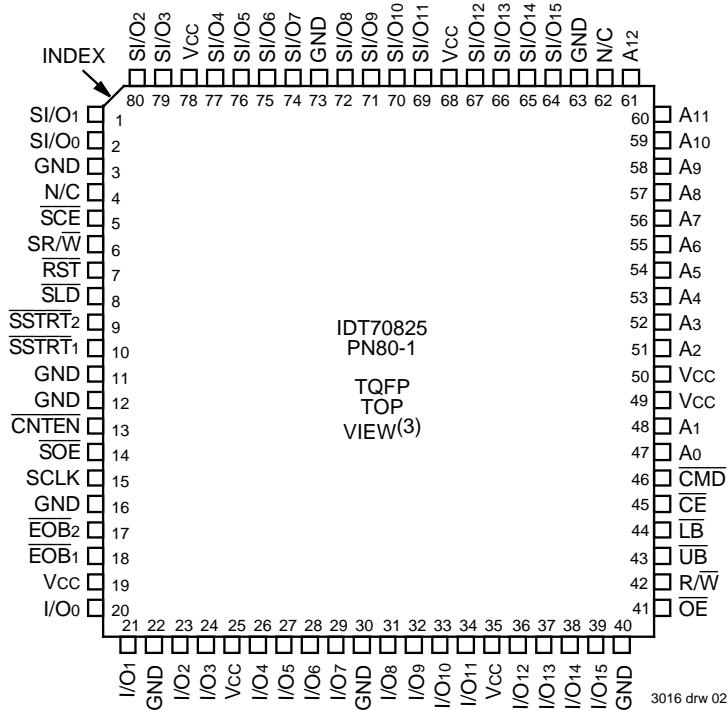
3016 drw 01

The IDT logo is a registered trademark and SARAM is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

OCTOBER 1996

PIN CONFIGURATIONS^(1,2)



NOTES:

1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part-marking.

PIN DESCRIPTIONS: RANDOM ACCESS PORT

SYMBOL	NAME	I/O ⁽¹⁾	DESCRIPTION
A0-A12	Address Lines	I	Address inputs to access the 8192-word (16 bit) memory array.
I/O0-I/O15	Inputs/Outputs	I	Random access data inputs/outputs for 16-bit wide data.
\overline{CE}	Chip Enable	I	When \overline{CE} is LOW, the random access port is enabled. When \overline{CE} is HIGH, the random access port is disabled into power-down mode and the I/O outputs are in the high-impedance state. All data is retained during $\overline{CE} = VIH$, unless it is altered by the sequential port. \overline{CE} and \overline{CMD} may not be LOW at the same time.
\overline{CMD}	Control Register Enable	I	When \overline{CMD} is LOW, Address lines A0-A2, R/\overline{W} , and inputs/outputs I/O0-I/O11, are used to access the control register, the flag register, and the start and end of buffer registers. \overline{CMD} and \overline{CE} may not be LOW at the same time.
R/\overline{W}	Read/Write Enable	I	If \overline{CE} is LOW and \overline{CMD} is HIGH, data is written into the array when R/\overline{W} is LOW and read out of the array when R/\overline{W} is HIGH. If \overline{CE} is HIGH and \overline{CMD} is LOW, R/\overline{W} is used to access the buffer command registers. \overline{CE} and \overline{CMD} may not be LOW at the same time.
\overline{OE}	Output Enable	I	When \overline{OE} is LOW and R/\overline{W} is HIGH, I/O0-I/O15 outputs are enabled. When \overline{OE} is HIGH, the I/O outputs are in the high-impedance state.
$\overline{LB}, \overline{UB}$	Lower Byte, Upper Byte Enables	I	When \overline{LB} is LOW, I/O0-I/O7 are accessible for read and write operations. When \overline{LB} is HIGH, I/O0-I/O7 are tri-stated and blocked during read and write operations. \overline{UB} controls access for I/O8-I/O15 in the same manner and is asynchronous from \overline{LB} .
VCC	Power Supply		Seven +5V power supply pins. All Vcc pins must be connected to the same +5V VCC supply.
GND	Ground		Ten Ground pins. All Ground pins must be connected to the same Ground supply.

3016 tbl 01

PIN DESCRIPTIONS: SEQUENTIAL ACCESS PORT

SYMBOL	NAME	I/O ⁽¹⁾	DESCRIPTION
SI/O0-15	Inputs	I/O	Sequential data inputs/outputs for 16-bit wide data.
SCLK	Clock	I	SI/O0-SI/O15, \overline{SCE} , SR/\overline{W} , and \overline{SLD} are registered on the LOW-to-HIGH transition of SCLK. Also, the sequential access port address pointer increments by 1 on each LOW-to-HIGH transition of SCLK when \overline{CNTEN} is LOW.
\overline{SCE}	Chip Enable	I	When \overline{SCE} is LOW, the sequential access port is enabled on the LOW-to-HIGH transition of SCLK. When \overline{SCE} is HIGH, the sequential access port is disabled into powered-down mode on the LOW-to-HIGH transition of SCLK, and the SI/O outputs are in the high-impedance state. All data is retained, unless altered by the random access port.
\overline{CNTEN}	Counter Enable	I	When \overline{CNTEN} is LOW, the address pointer increments on the LOW-to-HIGH transition of SCLK. This function is independent of \overline{SCE} .
SR/\overline{W}	Read/Write Enable	I	When SR/\overline{W} and \overline{SCE} are LOW, a write cycle is initiated on the LOW-to-HIGH transition of SCLK. When SR/\overline{W} is HIGH, and \overline{SCE} and \overline{SOE} are LOW, a read cycle is initiated on the LOW-to-HIGH transition of SCLK. Termination of a Write cycle is done on the Low-to-High transition of SCLK if SR/\overline{W} or \overline{SCE} is High.
\overline{SLD}	Address Pointer Load Control	I	When \overline{SLD} is sampled LOW, there is an internal delay of one cycle before the address pointer changes. When \overline{SLD} is LOW, data on the inputs SI/O0-SI/O11 is loaded into a data-in register on the LOW-to-HIGH transition of SCLK. On the cycle following \overline{SLD} , the address pointer changes to the address location contained in the data-in register. $\overline{SSTRT1}$ and $\overline{SSTRT2}$ may not be LOW while \overline{SLD} is LOW or during the cycle following \overline{SLD} .
$\overline{SSTRT1}, \overline{SSTRT2}$	Load Start of Address Register	I	When $\overline{SSTRT1}$ or $\overline{SSTRT2}$ is LOW, the start of address register #1 or #2 is loaded into the address pointer on the LOW-to-HIGH transition of SCLK. The start addresses are stored in internal registers. $\overline{SSTRT1}$ and $\overline{SSTRT2}$ may not be LOW while \overline{SLD} is LOW or during the cycle following \overline{SLD} .
$\overline{EOB1}, \overline{EOB2}$	End of Buffer Flag	O	$\overline{EOB1}$ or $\overline{EOB2}$ is output LOW when the address pointer is incremented to match the address stored in the end of buffer registers. The flags can be cleared by either asserting \overline{RST} LOW or by writing zero into bit 0 and/or bit 1 of the control register at address 101. $\overline{EOB1}$ and $\overline{EOB2}$ are dependent on separate internal registers, and therefore separate match addresses.
\overline{SOE}	Output Enable	I	\overline{SOE} controls the data outputs and is independent of SCLK. When \overline{SOE} is LOW, output buffers and the sequentially addressed data is output. When \overline{SOE} is HIGH, the SI/O output bus is in the high-impedance state. \overline{SOE} is asynchronous to SCLK.
\overline{RST}	Reset	I	When \overline{RST} is LOW, all internal registers are set to their default state, the address pointer is set to zero and the $\overline{EOB1}$ and $\overline{EOB2}$ flags are set HIGH. \overline{RST} is asynchronous to SCLK.

NOTE:

1. "I/O" is bidirectional Input and Output. "I" is Input and "O" is Output.

3016 tbl 02

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

- NOTES:** 3016 tbl 03
- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
 - VTERM must not exceed $V_{CC} + 0.5V$ for more than 25% of the cycle time or 10ns maximum, and is limited to $\leq 20mA$ for the period of $V_{TERM} \geq V_{CC} + 0.5V$.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Military	-55°C to +125°C	0V	5.0V \pm 10%
Commercial	0°C to +70°C	0V	5.0V \pm 10%

3016 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0 ⁽²⁾	V
VIL	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

- NOTES:** 3016 tbl 05
- $V_{IL} \geq -1.5V$ for pulse width less than 10ns.
 - VTERM must not exceed $V_{CC} + 0.5V$.

CAPACITANCE⁽¹⁾

($T_A = +25^\circ C$, $F = 1.0MHz$) TQFP ONLY

Symbol	Parameter	Conditions ⁽²⁾	Max.	Unit
CIN	Input Capacitance	$V_{IN} = 3dV$	9	pF
COUT	Output Capacitance	$V_{OUT} = 3dV$	10	pF

- NOTES:** 3016 tbl 06
- This parameter is determined by device characterization, but is not production tested.
 - 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	Test Conditions	IDT70825S		IDT70825L		Unit
			Min.	Max.	Min.	Max.	
ILI	Input Leakage Current ⁽¹⁾	$V_{CC} = \text{Max. } V_{IN} = \text{GND to } V_{CC}$	—	5.0	—	1.0	μA
ILO	Output Leakage Current	$V_{CC} = \text{Max. } \overline{CE} \text{ and } \overline{SCE} = V_{IH}$ $V_{OUT} = \text{GND to } V_{CC}$	—	5.0	—	1.0	μA
VOL	Output Low Voltage	$I_{OL} = 4mA, V_{CC} = \text{Min.}$	—	0.4	—	0.4	V
VOH	Output High Voltage	$I_{OH} = -4mA, V_{CC} = \text{Min.}$	2.4	—	2.4	—	V

- NOTE:** 3016 tbl 07
- At $V_{CC} \leq 2.0V$ input leakages are undefined.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE⁽¹⁾ (VCC = 5.0V ± 10%)


Symbol	Parameter	Test Condition	Version	70825X20		70825X25		70825X35		70825X45		Unit
				Com'l. Only Typ. ⁽²⁾	Max.	Com'l. Only Typ. ⁽²⁾	Max.	Typ. ⁽²⁾	Max.	Typ. ⁽²⁾	Max.	
ICC	Dynamic Operating Current (Both Ports Active)	$\overline{CE} = V_{IL}$, Outputs Open, $\overline{SCE} = V_{IL}$ ⁽⁵⁾ $f = f_{MAX}$ ⁽³⁾	MIL. S L	—	—	—	—	160	400	155	400	mA
				COM'L. S L	180 180	380 330	170 170	360 310	160 160	340 290	155 155	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	\overline{SCE} and $\overline{CE} \geq V_{IH}$ ⁽⁷⁾ $\overline{CMD} = V_{IH}$ $f = f_{MAX}$ ⁽³⁾	MIL. S L	—	—	—	—	20	85	16	85	mA
				COM'L. S L	25 25	70 50	25 25	70 50	20 20	70 50	16 16	
ISB2	Standby Current (One Port - TTL Level Input)	\overline{CE} or $\overline{SCE} = V_{IH}$ Active Port Outputs Open, $f = f_{MAX}$ ⁽³⁾	MIL. S L	—	—	—	—	95	290	90	290	mA
				COM'L. S L	115 115	260 230	105 105	250 220	95 95	240 210	90 90	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports \overline{CE} and $\overline{SCE} \geq V_{CC} - 0.2V$ ^(6,7) $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0$ ⁽⁴⁾	MIL. S L	—	—	—	—	1.0	30	1.0	30	mA
				COM'L. S L	1.0 0.2	15 5	1.0 0.2	15 5	1.0 0.2	15 5	1.0 0.2	
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	One Port \overline{CE} or $\overline{SCE} \geq V_{CC} - 0.2V$ ⁽⁶⁾ Outputs Open (Active port), $f = f_{MAX}$ ⁽³⁾ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	MIL. S L	—	—	—	—	90	260	85	260	mA
				COM'L. S L	110 110	240 200	100 100	230 190	90 90	220 180	85 85	

NOTES:

- "X" in part number indicates power rating (S or L).
- VCC = 5V, Ta = +25°C; guaranteed by device characterization but not production tested.
- At f = fMAX, address, control lines (except Output Enable), and SCLK are cycling at the maximum frequency read cycle of 1/tRC.
- f = 0 means no address or control lines change.
- \overline{SCE} may transition, but is Low ($\overline{SCE} = V_{IL}$) when clocked in by SCLK.
- \overline{SCE} may be ≤ 0.2V, after it is clocked in, since SCLK=V_{IH} must be clocked in prior to powerdown.
- If one port is enabled (either CE or SCE = Low) then the other port is disabled (SCE or CE = High, respectively). CMOS High ≥ Vcc - 0.2V and Low ≤ 0.2V, and TTL High = V_{IH} and Low = V_{IL}.

3016 tbl 08

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES (L VERSION ONLY) (VLC ≤ 0.2V, VHC ≥ VCC - 0.2V)

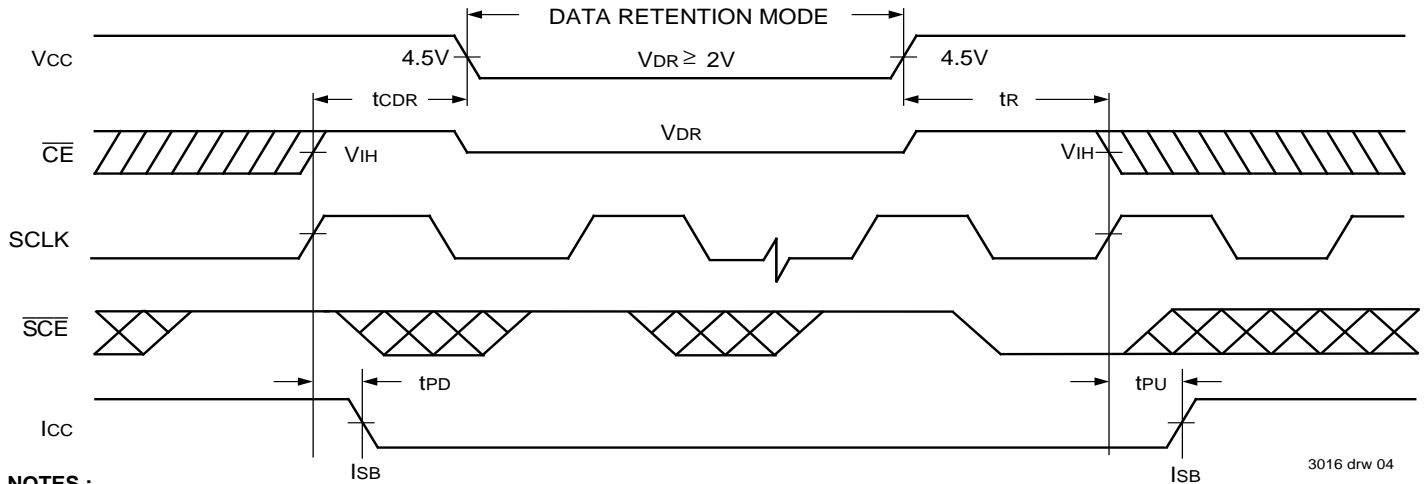
Symbol	Parameter	Test Condition	Min.	Typ. ⁽¹⁾	Max.	Unit	
VDR	VCC for Data Retention	VCC = 2V	2.0	—	—	V	
ICCDR	Data Retention Current	$\overline{CE} = V_{HC}$ $V_{IN} = V_{HC}$ or V_{LC}	MIL.	—	100	4000	μA
			COM'L.	—	100	1500	
tCDR ⁽³⁾	Chip Deselect to Data Retention Time	$\overline{SCE} = V_{HC}$ ⁽⁴⁾ when SCLK = 	0	—	—	ns	
tR ⁽³⁾	Operation Recovery Time	$\overline{CMD} = V_{HC}$	tRC ⁽²⁾	—	—	ns	

NOTES:

- Ta = +25°C, Vcc = 2V; guaranteed by device characterization but not production tested.
- tRC = Read Cycle Time
- This parameter is guaranteed by device characterization, but is not production tested.
- To initiate data retention, $\overline{SCE} = V_{IH}$ must be clocked in.

3016 tbl 09

DATA RETENTION AND POWER DOWN/UP WAVEFORM (RANDOM AND SEQUENTIAL PORT) (1,2)



NOTES :

1. \overline{SCE} is synchronized to the sequential clock input.
2. $\overline{CMD} \geq V_{cc} - 0.2V$.

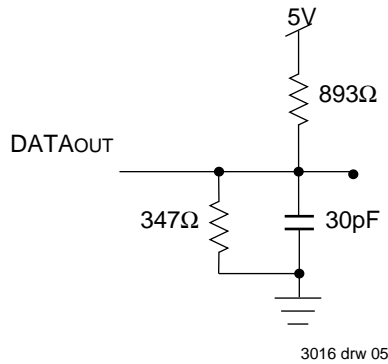


Figure 1. AC Output Test Load

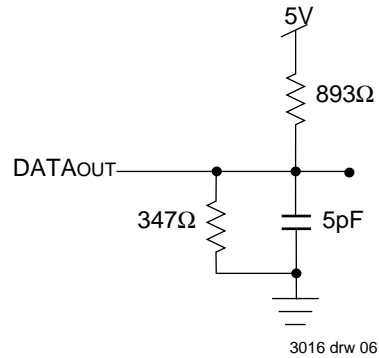


Figure 2. Output Test Load (for tCLZ, tBLZ, tOLZ, tCHZ, tBHZ, tOHZ, tWHZ, tCKHZ, and tCKLZ) Including scope and jig.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	Figures 1, 2, and 3

3016 tbl 10

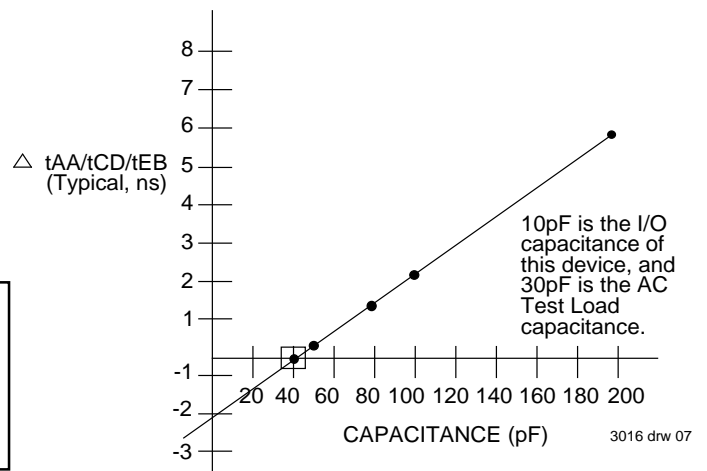


Figure 3. Lumped Capacitance Load Typical Derating Curve

TRUTH TABLE I – RANDOM ACCESS READ AND WRITE (1,2)

Inputs/Outputs								MODE
CE	CMD	R/W	OE	LB	UB	I/O0-I/O7	I/O8-I/O-	
L	H	H	L	L	L	DATAOUT	DATAOUT	Read both Bytes.
L	H	H	L	L	H	DATAOUT	High-Z	Read lower Byte only.
L	H	H	L	H	L	High-Z	DATAOUT	Read upper Byte only.
L	H	L	H ⁽³⁾	L	L	DATAIN	DATAIN	Write to both Bytes.
L	H	L	H ⁽³⁾	L	H	DATAIN	High-Z	Write to lower Byte only.
L	H	L	H ⁽³⁾	H	L	High-Z	DATAIN	Write to upper Byte only.
H	H	X	X	X	X	High-Z	High-Z	Both Bytes deselected and powered down.
L	H	H	H	X	X	High-Z	High-Z	Outputs disabled but not powered down.
L	H	X	X	H	H	High-Z	High-Z	Both Bytes deselected but not powered down.
H	L	L	H ⁽³⁾	L ⁽⁴⁾	L ⁽⁴⁾	DATAIN	DATAIN	Write I/O0-I/O12 to the Buffer Command Register.
H	L	H	L	L ⁽⁴⁾	L ⁽⁴⁾	DATAOUT	DATAOUT	Read contents of the Buffer Command Register via I/O0-I/O12.

NOTES:

3016 tbl 11

- H = V_{IH}, L = V_{IL}, X = Don't Care, and High-Z = High-impedance.
- RST, SCE, CNTEN, SR/W, SLD, SSTR1, SSTR2, SCLK, SI/O0-SI/O15, EOB1, EOB2, and SOE are unrelated to the random access port control and operation.
- If OE = V_{IL} during write, t_{WHZ} must be added to the t_{WP} or t_{WC} write pulse width to allow the bus to float prior to being driven.
- Byte operations to control register using UB and LB separately are also allowed.

TRUTH TABLE II – SEQUENTIAL READ (1,2,3,6,8)

Inputs/Outputs								MODE
SCLK	SCE	CNTEN	SR/W	EOB1	EOB2	SOE	S/O	
	L	L	H	LOW	LAST	L	[EOB1]	Counter Advanced Sequential Read with EOB1 reached.
	L	H	H	LAST	LAST	L	[EOB1 - 1]	Non-Counter Advanced Sequential Read, without EOB1 reached.
	L	L	H	LAST	LOW	L	[EOB2]	Counter Advanced Sequential Read with EOB2 reached.
	L	H	H	LAST	LAST	L	[EOB2 - 1]	Non-Counter Advanced Sequential Read without EOB2 reached.
	L	L	H	LOW	LOW	H	HIGH-Z	Counter Advanced Sequential Non-Read with EOB1 and EOB2 reached.

3016 tbl 12

TRUTH TABLE III – SEQUENTIAL WRITE (1,2,3,4,5,6,7,8)

Inputs/Outputs								MODE
SCLK	SCE	CNTEN	SR/W	EOB1	EOB2	SOE	S/O	
	L	H	L	LAST	LAST	H	SI/OIN	Non-Counter Advanced Sequential Write, without EOB1 or EOB2 reached.
	L	L	L	LOW	LOW	H	SI/OIN	Counter Advanced Sequential Write with EOB1 and EOB2 reached.
	H	H	X	LAST	LAST	X	High-Z	No Write or Read due to Sequential port Deselect. No counter advance.
	H	L	X	NEXT	NEXT	X	High-Z	No Write or Read due to Sequential port Deselect. Counter does advance.

NOTES:

3016 tbl 13

- H = V_{IH}, L = V_{IL}, X = Don't Care, and High-Z = High-impedance. LOW = V_{OL}.
- RST, SLD, SSTR1, SSTR2 are continuously HIGH during a sequential write access, other than pointer access operations.
- CE, OE, R/W, CMD, LB, UB, and I/O0-I/O15 are unrelated to the sequential port control and operation except for CMD which must not be used concurrently with the sequential port operation (due to the counter and register control). CMD should be HIGH (CMD = V_{IH}) during sequential port access.
- SOE must be HIGH (SOE = V_{IH}) prior to write conditions only if the previous cycle is a read cycle, since the data being written must be an input at the rising edge of the clock during the cycle in which SR/W = V_{IL}.
- SI/OIN refers to SI/O0-SI/O15 inputs.
- "LAST" refers to the previous value still being output, no change.
- Termination of a write is done on the Low-to-High transition of SCLK if SR/W or SCE is High.
- When CLKEN=Low, the address is incremented on the next rising edge before any operation takes place. See the diagrams called "Sequential Counter Enable Cycle after Reset, Read (and write) Cycle".

TRUTH TABLE IV – SEQUENTIAL ADDRESS POINTER OPERATIONS (1,2,3,4,5)

Inputs/Outputs					MODE
SCLK	SLD	SSTRT1	SSTRT2	SOE	
	H	L	H	X	Start address for Buffer #1 loaded into Address Pointer.
	H	H	L	X	Start address for Buffer #2 loaded into Address Pointer.
	L	H	H	H ⁽⁶⁾	Data on SI/O ₀ -SI/O ₁₂ loaded into Address Pointer.

NOTES:

3016 tbl 14

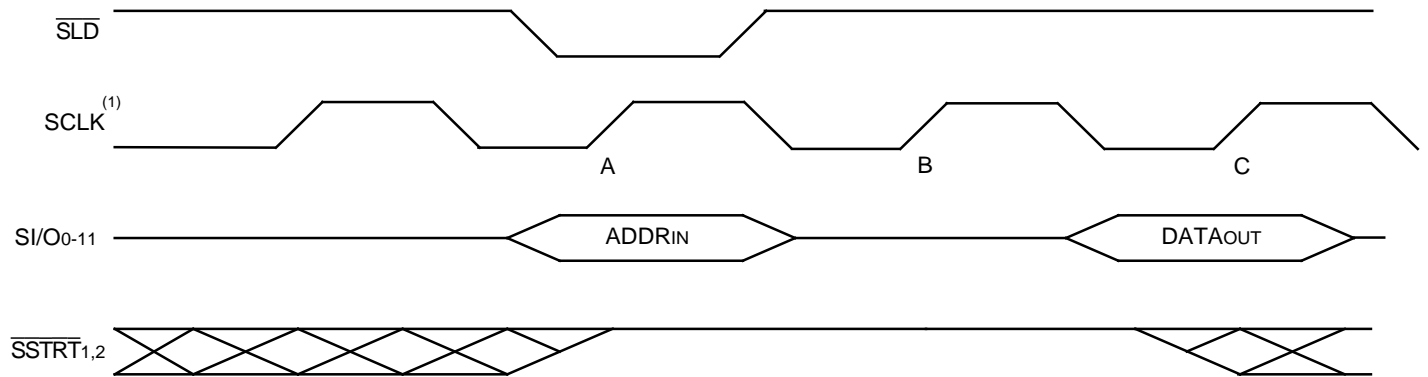
- H = V_{IH}, L = V_{IL}, X = Don't Care, and High-Z = High-impedance.
- RST is continuously HIGH. The conditions of SCE, CNTEN, and SR/W are unrelated to the sequential address pointer operations.
- CE, OE, R/W, LB, UB, and I/O₀-I/O₁₅ are unrelated to the sequential port control and operation, except for CMD which must not be used concurrently with the sequential port operation (due to the counter and register control). CMD should be HIGH (CMD = V_{IH}) during sequential port access.
- Address pointer can also change when it reaches an end of buffer address. See Flow Control Bits table.
- When SLD is sampled LOW, there is an internal delay of one cycle before the address pointer changes. The state of CNTEN is ignored and the address is not incremented during the two cycles.
- SOE may be LOW with SCE deselect or in the write mode using SR/W.

ADDRESS POINTER LOAD CONTROL (SLD)

In SLD mode, there is an internal delay of one cycle before the address pointer changes in the cycle following SLD. When SLD is LOW, data on the inputs SI/O₀-SI/O₁₂ is loaded into a data-in register on the LOW-to-HIGH transition of SCLK. On the cycle following SLD, the address pointer changes to the

address location contained in the data-in register. SSTRT₁, SSTRT₂ may not be low while SLD is LOW, or during the cycle following SLD. The SSTRT₁ and SSTRT₂ require only one clock cycle, since these addresses are pre-loaded in the registers already.

SLD MODE (1)

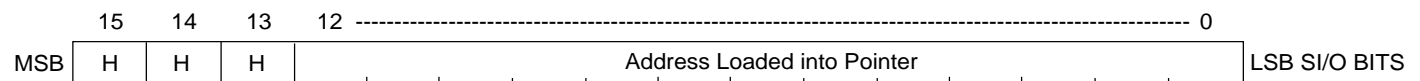


3016 drw 08

NOTE:

- At SCLK edge (A), SI/O₀-SI/O₁₂ data is loaded into a data-in register. At edge (B), contents of the data-in register are loaded into the address pointer (i.e. address pointer changes). At SCLK edge (A), SSTRT₁ and SSTRT₂ must be high to ensure for proper sequential address pointer loading. At SCLK edge (B), SLD and SSTRT_{1,2} must be high to ensure for proper sequential address pointer loading. For SSTRT₁ or SSTRT₂, the data to be read will be ready for edge (B), while data will not be ready at edge (B) when SLD is used, but will be ready at edge (C).

SEQUENTIAL LOAD OF ADDRESS INTO POINTER/COUNTER (1)



3016 drw 09

NOTE:

- "H" = V_{IH} for the SI/O input state.

Reset (\overline{RST})

Setting \overline{RST} LOW resets the control state of the SARAM. \overline{RST} functions asynchronously of SCLK, (i.e. not registered). The default states after a reset operation are as follows:

Register	Contents
Address Pointer	0
EOB Flags	Cleared to High state
Buffer Flow Mode	BUFFER CHAINING
Start Address Buffer #1	0 (1)
End Address Buffer #1	4095 (4K)
Start Address Buffer #2	4096 (4K+1)
End Address Buffer #2	8191 (8K)
Registered State	$\overline{SCE} = VIH, SR/\overline{W} = VIL$

3016 tbl 15

BUFFER COMMAND MODE (\overline{CMD})

Buffer Command Mode (\overline{CMD}) allows the random access port to control the state of the two buffers. Address pins A0-A2 and I/O pins I/O0-I/O12 are used to access the start of buffer and the end of buffer addresses and to set the flow control mode of each buffer. The Buffer Command Mode also allows

reading and clearing the status of the EOB flags. Seven different CMD cases are available depending on the conditions of A0-A2 and R/W. Address bits A3-A12 and data I/O bits I/O13-I/O15 are not used during this operation.

RANDOM ACCESS PORT \overline{CMD} MODE⁽¹⁾

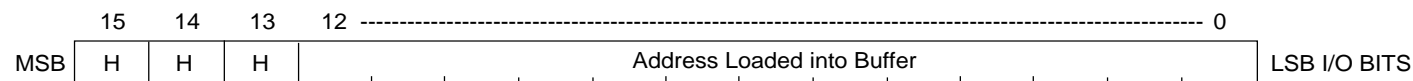
Case #	A2-A0	R/ \overline{W}	DESCRIPTIONS
1	000	0 (1)	Write (read) the start address of Buffer #1 through I/O0-I/O12.
2	001	0 (1)	Write (read) the end address of Buffer #1 through I/O0-I/O12.
3	010	0 (1)	Write (read) the start address of Buffer #2 through I/O0-I/O12.
4	011	0 (1)	Write (read) the end address of Buffer #2 through I/O0-I/O12.
5	100	0 (1)	Write (read) flow control register
6	101	0	Write only – clear EOB1 and/or EOB2 flag
7	101	1	Read only – flag status register
8	110/111	(X)	(Reserved)

NOTE:

1. R/ \overline{W} input "0(1)" indicates a write(0) or read(1) occurring with the same address input.

3016 tbl 16

CASES 1 THROUGH 4: START AND END OF BUFFER REGISTER DESCRIPTION^(1,2)



NOTES:

1. "H" = V_{OH} for I/O in the output state and "Don't Cares" for I/O in the input state.
2. A write into the buffer occurs when $R/\overline{W} = V_{IL}$ and a read when $R/\overline{W} = V_{IH}$. $\overline{EOB1}/\overline{SOB1}$ and $\overline{EOB2}/\overline{SOB2}$ are chosen through address A0-A2 while $\overline{CMD} = V_{IL}$ and $\overline{CE} = V_{IH}$.

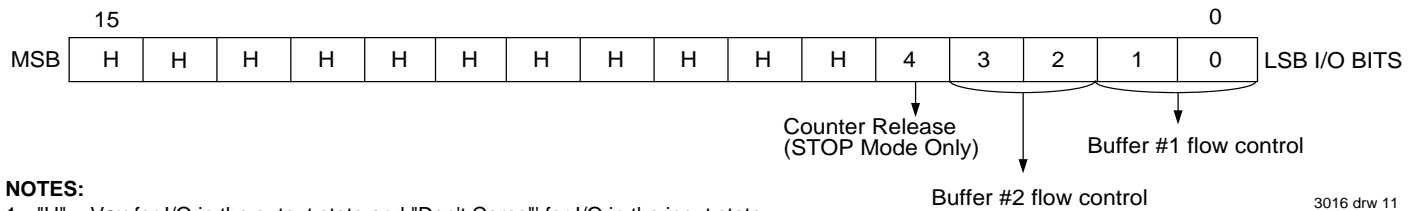
3016 drw 10

CASE 5: BUFFER FLOW MODES

Within the SARAM, the user can designate one of four buffer flow modes for each buffer. Each buffer flow mode defines a unique set of actions for the sequential port address pointer and EOB flags. In BUFFER CHAINING mode, after the address pointer reaches the end of the buffer, it sets the corresponding EOB flag and continues from the start address

of the other buffer. In STOP mode, the address pointer stops incrementing after it reaches the end of the buffer. In LINEAR mode, the address pointer ignores the end of buffer address and increments past it, but sets the EOB flag. MASK mode is the same as LINEAR mode except EOB flags are not set.

FLOW CONTROL REGISTER DESCRIPTION^(1,2)



NOTES:

- "H" = V_{OH} for I/O in the output state and "Don't Cares" for I/O in the input state.
- Writing a 0 into bit 4 releases the address pointer after it is stopped due to the STOP mode and allows sequential write operations to resume. This occurs asynchronously of SCLK, and therefore caution should be taken. The pointer will be at address EOB+2 on the next rising edge of SCLK that is enabled by CNTEN. The pointer is also released by RST, SLD, SSTR1 and SSTR2 operations.

3016 drw 11

FLOW CONTROL BITS

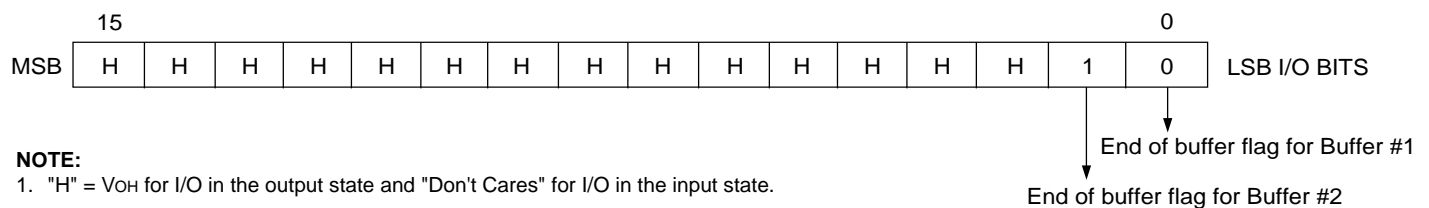
Flow Control Bits		Functional Description
Bit 1 & Bit 0 (Bit 3 & Bit 2)	Mode	
00	BUFFER CHAINING	$\overline{EOB1}$ ($\overline{EOB2}$) is asserted (Active Low output) when the pointer matches the end address of Buffer #1 (Buffer #2). The pointer value is changed to the start address of Buffer #2 (Buffer #1). ^(1,3)
01	STOP	$\overline{EOB1}$ ($\overline{EOB2}$) is asserted when the pointer matches the end address of Buffer #1 (Buffer #2). The address pointer will stop incrementing when it reaches the next address (\overline{EOB} address + 1), if CNTEN is Low on the next clock's rising edge. Otherwise, the address pointer will stop incrementing on \overline{EOB} . Sequential write operations are inhibited after the address pointer is stopped. The pointer can be released by bit 4 of the flow control register. ^(1,2,4)
10	LINEAR	$\overline{EOB1}$ ($\overline{EOB2}$) is asserted when the pointer matches the end address of Buffer #1 (Buffer #2). The pointer keeps incrementing for further operations. ⁽¹⁾
11	MASK	$\overline{EOB1}$ ($\overline{EOB2}$) is not asserted when the pointer reaches the end address of Buffer #1 (Buffer #2), although the flag status bits will be set. The pointer keeps incrementing for further operations.

NOTES:

- $\overline{EOB1}$ and $\overline{EOB2}$ may be asserted (set) at the same time, if both end addresses have been loaded with the same value.
- CMD Flow Control bits are unchanged, the count does not continue advancement.
- If $\overline{EOB1}$ and $\overline{EOB2}$ are equal, then the pointer will jump to the start of Buffer #1.
- If counter has stopped at EOBx and was released by bit 4 of the flow control register, CNTEN must be LOW on the next rising edge of SCLK otherwise the flow control will remain in the STOP mode.

3016 tbl 17

CASES 6 AND 7: FLAG STATUS REGISTER BIT DESCRIPTION⁽¹⁾



NOTE:

- "H" = V_{OH} for I/O in the output state and "Don't Cares" for I/O in the input state.

3016 drw 12

CASE 6: FLAG STATUS REGISTER WRITE CONDITIONS⁽¹⁾

Flag Status Bit 0, (Bit 1)	Functional Description
0	Clears Buffer Flag $\overline{EOB1}$, ($\overline{EOB2}$).
1	No change to the Buffer Flag. ⁽²⁾

NOTES:

- Either bit 0 or bit 1, or both bits, may be changed simultaneously. One may be cleared while the second is left alone or cleared.
- Remains as it was prior to the CMD operation, either HIGH (1) or LOW (0).

3016 tbl 18

CASE 7: FLAG STATUS REGISTER READ CONDITIONS

Flag Status Bit 0, (Bit 1)	Functional Description
0	$\overline{EOB1}$ ($\overline{EOB2}$) flag has not been set, the Pointer has not reached the End of the Buffer.
1	$\overline{EOB1}$ ($\overline{EOB2}$) flag has been set, the Pointer has reached the End of the Buffer.

3016 tbl 19

CASES 8 AND 9: (RESERVED)

Illegal operations. All outputs will be HIGH on the I/O bus during a READ.

RANDOM ACCESS PORT: AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (2,3)

Symbol	Parameter	IDT70825X20 Com'l. Only		IDT70825X25 Com'l. Only		IDT70825X35		IDT70825X45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
tRC	Read Cycle Time	20	—	25	—	35	—	45	—	ns
tAA	Address Access Time	—	20	—	25	—	35	—	45	ns
tACE	Chip Enable Access Time	—	20	—	25	—	35	—	45	ns
tBE	Byte Enable Access Time	—	20	—	25	—	35	—	45	ns
tOE	Output Enable Access Time	—	10	—	10	—	15	—	20	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
tCLZ	Chip Select Low-Z Time ⁽¹⁾	3	—	3	—	3	—	3	—	ns
tBLZ	Byte Enable Low-Z Time ⁽¹⁾	3	—	3	—	3	—	3	—	ns
tOLZ	Output Enable Low-Z Time ⁽¹⁾	2	—	2	—	2	—	2	—	ns
tCHZ	Chip Select High-Z Time ⁽¹⁾	—	10	—	12	—	15	—	15	ns
tBHZ	Byte Enable High-Z Time ⁽¹⁾	—	10	—	12	—	15	—	15	ns
tOHZ	Output Enable High-Z Time ⁽¹⁾	—	9	—	11	—	15	—	15	ns
tPU	Chip Select Power-Up Time	0	—	0	—	0	—	0	—	ns
tPD	Chip Select Power-Down Time	—	20	—	25	—	35	—	45	ns

NOTES:

3016 tbl 20

- Transition measured at ±200mV from steady state. This parameter is guaranteed with the AC Test Load (Figure 2) by device characterization, but is not production tested.
- "X" in part number indicates power rating (S or L).
- CMD access follows standard timing listed for both read and write accesses, ($\overline{CE} = V_{IH}$ when $\overline{CMD} = V_{IL}$) or ($\overline{CMD} = V_{IH}$ when $\overline{CE} = V_{IL}$).

RANDOM ACCESS PORT: AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (2,4)

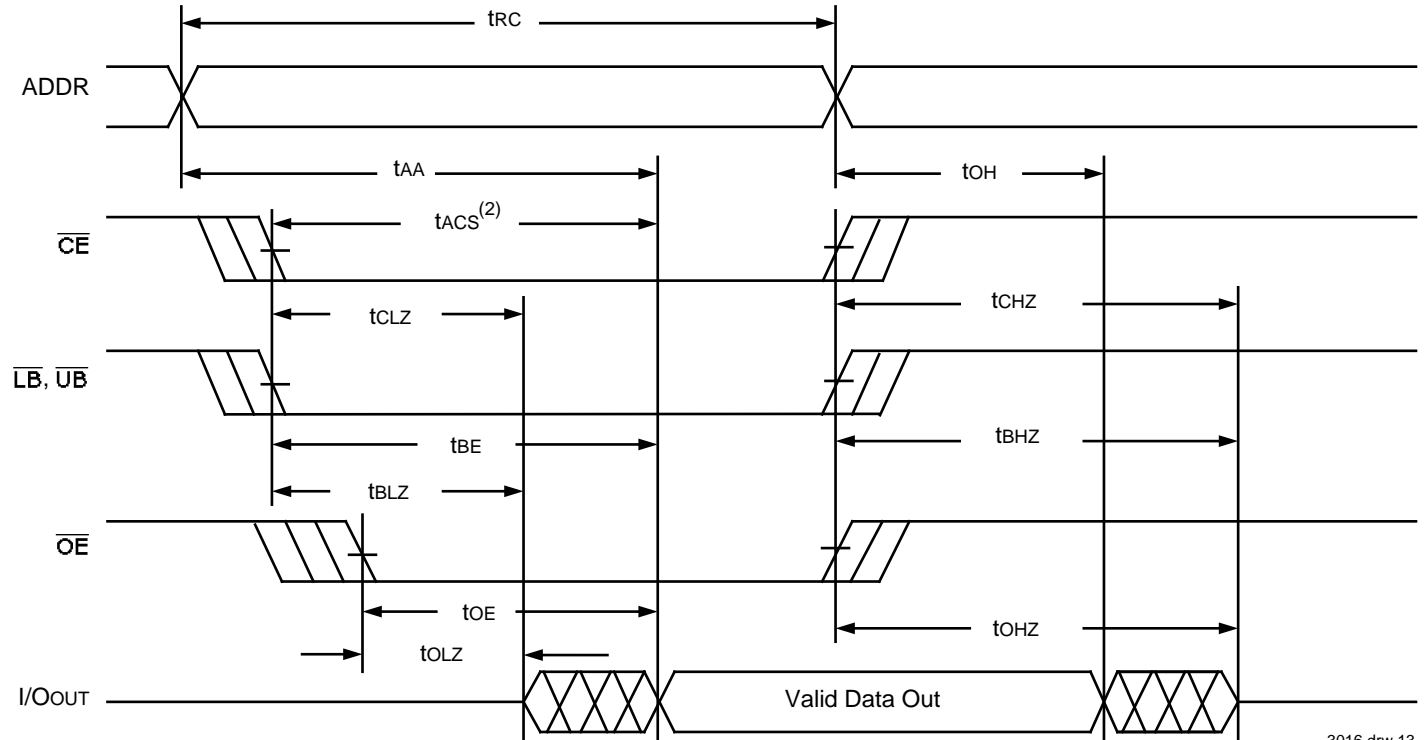
Symbol	Parameter	IDT70825X20 Com'l. Only		IDT70825X25 Com'l. Only		IDT70825X35		IDT70825X45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
tWC	Write Cycle Time	20	—	25	—	35	—	45	—	ns
tCW	Chip Select to End-of-Write	15	—	20	—	25	—	30	—	ns
tAW	Address Valid to End-of-Write ⁽³⁾	15	—	20	—	25	—	30	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width ⁽³⁾	13	—	20	—	25	—	30	—	ns
tBP	Byte Enable Pulse Width ⁽³⁾	15	—	20	—	25	—	30	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable Output High-Z Time ⁽¹⁾	—	10	—	12	—	15	—	15	ns
tDW	Data Set-up Time	13	—	15	—	20	—	25	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tOW	Output Active from End-of-Write	3	—	3	—	3	—	3	—	ns

NOTES:

3016 tbl 21

- Transition measured at ±200mV from steady state. This parameter is guaranteed with the AC Test Load (Figure 2) by device characterization, but is not production tested.
- "X" in part number indicates power rating (S or L).
- \overline{OE} is continuously HIGH, $\overline{OE} = V_{IH}$. If during the R/\overline{W} controlled write cycle the \overline{OE} is LOW, t_{WP} must be greater or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and on the data to be placed on the bus for the required t_{DW} . If \overline{OE} is HIGH during the R/\overline{W} controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP} . For the \overline{CE} controlled write cycle, \overline{OE} may be LOW with no degradation to t_{CW} timing.
- CMD access follows standard timing listed for both read and write accesses, ($\overline{CE} = V_{IH}$ when $\overline{CMD} = V_{IL}$) or ($\overline{CMD} = V_{IH}$ when $\overline{CE} = V_{IL}$).

RANDOM ACCESS PORT WAVEFORM: READ CYCLES (1,2)

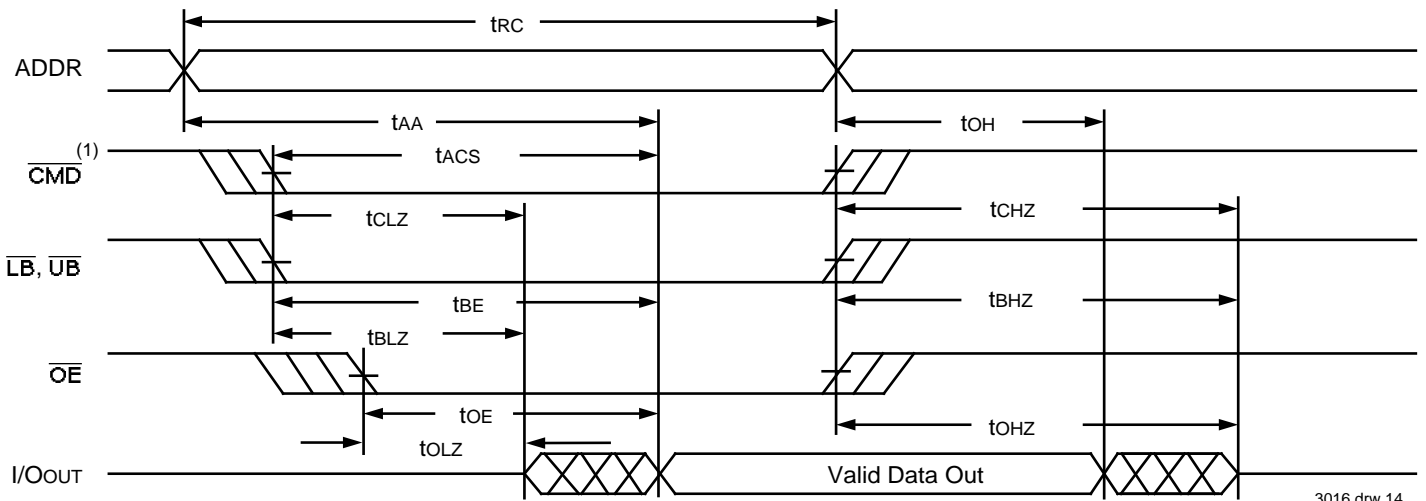


3016 drw 13

NOTES:

1. R/\overline{W} is HIGH for Read cycle.
2. Address valid prior to or coincident with \overline{CE} transition LOW; otherwise t_{AA} is the limiting parameter.

RANDOM ACCESS PORT WAVEFORM: READ CYCLES BUFFER COMMAND MODE

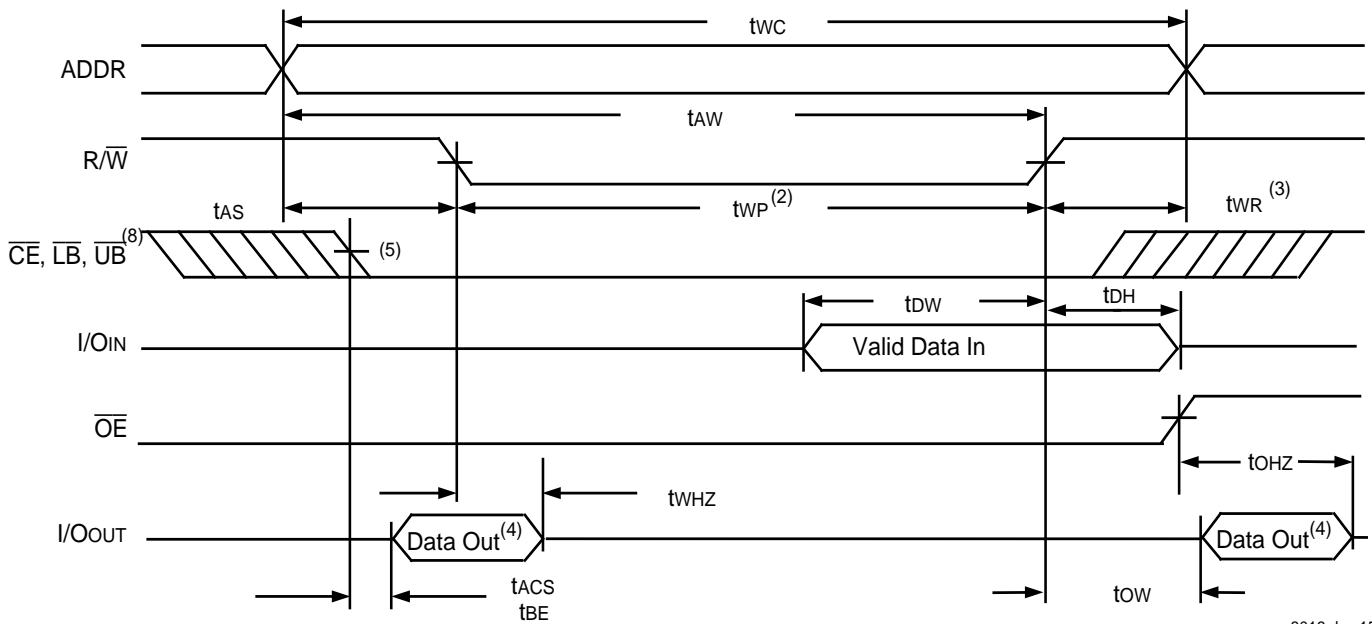


3016 drw 14

NOTE:

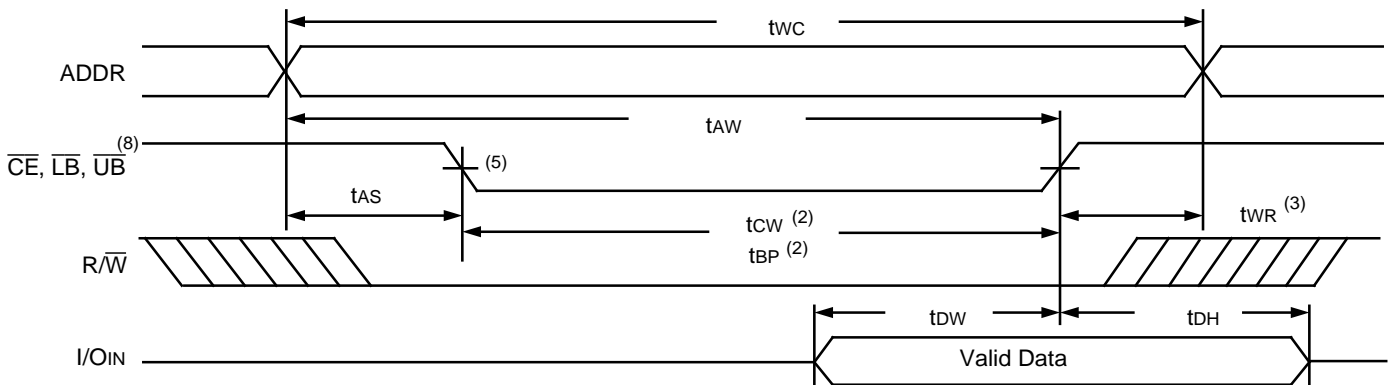
1. $\overline{CE} = V_{IH}$ when $\overline{CMD} = V_{IL}$.

RANDOM ACCESS PORT WAVEFORM: WRITE CYCLE NO.1 (R/W CONTROLLED TIMING) (1,6)



3016 drw 15

RANDOM ACCESS PORT WAVEFORM: WRITE CYCLE NO.2 (CE, LB, AND/OR UB CONTROLLED TIMING) (1,6,7)



3016 drw 16

NOTES:

1. R/W, CE, or LB and UB must be inactive during all address transitions.
2. A write occurs during the overlap of R/W = V_{IL}, CE = V_{IL} and LB = V_{IL} and/or UB = V_{IL}.
3. tWR is measured from the earlier of CE (and LB and/or UB) or R/W going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state and the input signals must not be applied.
5. If the CE LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in the High-impedance state.
6. OE is continuously HIGH, OE = V_{IH}. If during the R/W controlled write cycle the OE is LOW, tWP must be greater or equal to tWHZ + tDW to allow the I/O drivers to turn off and on the data to be placed on the bus for the required tDW. If OE is HIGH during the R/W controlled write cycle, this requirement does not apply and the minimum write pulse is the specified tWP. For the CE controlled write cycle, OE may be LOW with no degradation to tcw timing.
7. I/O_{OUT} is never enabled, therefore the output is in High-Z state during the entire write cycle.
8. CMD access follows the standard CE access described above. If CMD = V_{IL}, then CE must = V_{IH} or, when CE = V_{IL}, CMD must = V_{IH}.

SEQUENTIAL PORT: AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE⁽²⁾

Symbol	Parameter	IDT70825X20 Com'l. Only		IDT70825X25 Com'l. Only		IDT70825X35		IDT70825X45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
tCYC	Sequential Clock Cycle Time	25	—	30	—	40	—	50	—	ns
tCH	Clock Pulse High	10	—	12	—	15	—	18	—	ns
tCL	Clock Pulse Low	10	—	12	—	15	—	18	—	ns
tES	Count Enable and Address Pointer Set-up Time	5	—	5	—	6	—	6	—	ns
tEH	Count Enable and Address Pointer Hold Time	2	—	2	—	2	—	2	—	ns
tSOE	Output Enable to Data Valid	—	8	—	10	—	15	—	20	ns
tOLZ	Output Enable Low-Z Time ⁽¹⁾	2	—	2	—	2	—	2	—	ns
tOHZ	Output Enable High-Z Time ⁽¹⁾	—	9	—	11	—	15	—	15	ns
tCD	Clock to Valid Data	—	20	—	25	—	35	—	45	ns
tCKHZ	Clock High-Z Time ⁽¹⁾	—	12	—	14	—	17	—	20	ns
tCKLZ	Clock Low-Z Time ⁽¹⁾	3	—	3	—	3	—	3	—	ns
tEB	Clock to EOB	—	13	—	15	—	18	—	23	ns

NOTES:

3016 tbl 23

1. Transition measured at ±200mV from steady state. This parameter is guaranteed with the AC Test Load (Figure 2) by device characterization, but is not production tested.
2. "X" in part numbers indicates power rating (S or L).

SEQUENTIAL PORT: AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE⁽¹⁾

Symbol	Parameter	IDT70825X20 Com'l. Only		IDT70825X25 Com'l. Only		IDT70825X35		IDT70825X45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
tCYC	Sequential Clock Cycle Time	25	—	30	—	40	—	50	—	ns
tFS	Flow Restart Time	13	—	15	—	20	—	20	—	ns
tWS	Chip Select and Read/Write Set-up Time	5	—	5	—	6	—	6	—	ns
tWH	Chip Select and Read/Write Hold Time	2	—	2	—	2	—	2	—	ns
tDS	Input Data Set-up Time	5	—	5	—	6	—	6	—	ns
tDH	Input Data Hold Time	2	—	2	—	2	—	2	—	ns

NOTE:

3016 tbl 23

1. "X" in part numbers indicates power rating (S or L).

SEQUENTIAL PORT: AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE⁽¹⁾

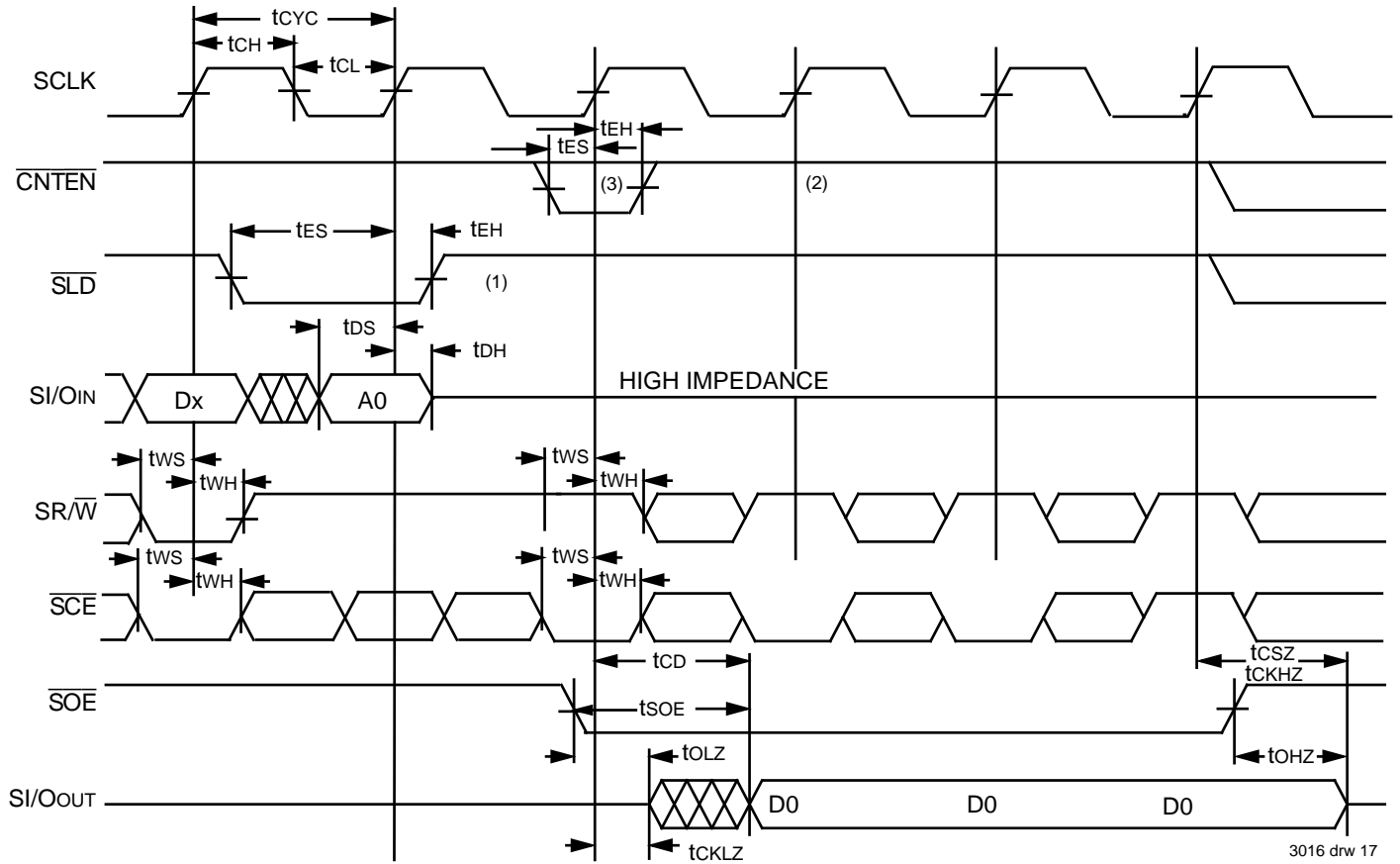
Symbol	Parameter	IDT70825X20 Com'l. Only		IDT70825X25 Com'l. Only		IDT70825X35		IDT70825X45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
RESET CYCLE										
tRSPW	Reset Pulse Width	13	—	15	—	20	—	20	—	ns
tWERS	Write Enable High to Reset High	10	—	10	—	10	—	10	—	ns
tRSRC	Reset High to Write Enable Low	10	—	10	—	10	—	10	—	ns
tRSFV	Reset High to Flag Valid	15	—	20	—	25	—	25	—	ns

NOTE:

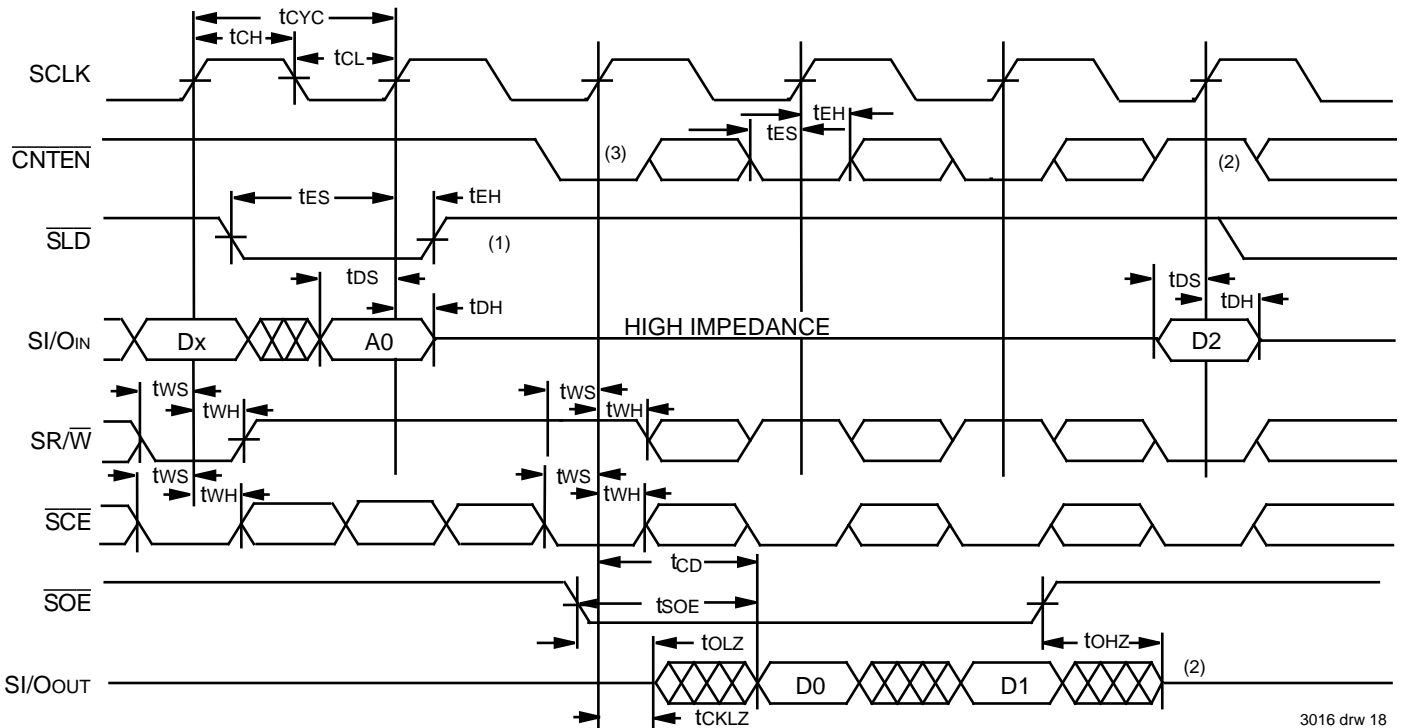
3016 tbl 24

1. "X" in part numbers indicates power rating (S or L).

SEQUENTIAL PORT WAVEFORM: WRITE, POINTER LOAD, NON-INCREMENTING READ



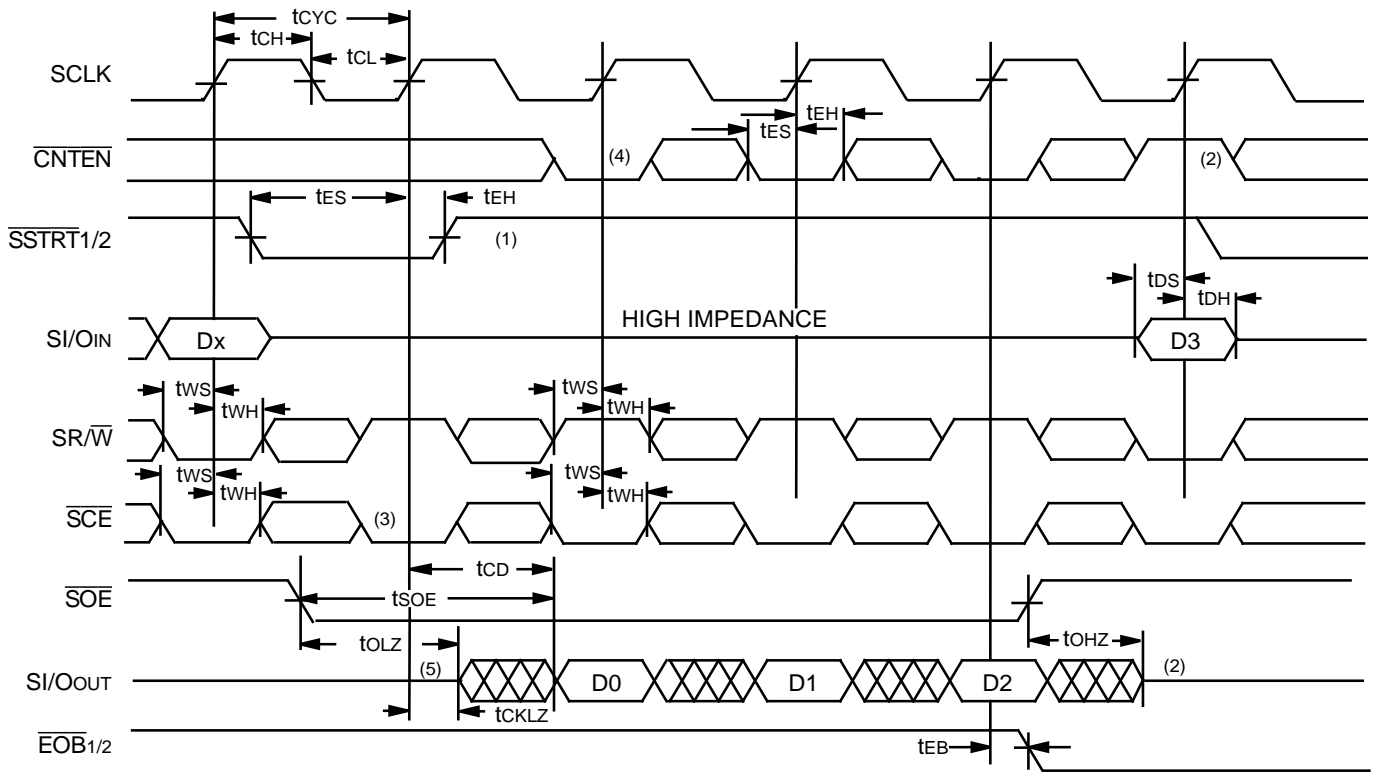
SEQUENTIAL PORT WAVEFORM: WRITE, POINTER LOAD, BURST READ



NOTES:

1. If $\overline{SLD} = V_{IL}$, then address will be clocked in on the SCLK's rising edge.
2. If $\overline{CNTEN} = V_{IH}$ for the SCLK's rising edge, the internal address counter will not advance.
3. Pointer is not incremented on cycle immediately following \overline{SLD} even if \overline{CNTEN} is LOW.

SEQUENTIAL PORT WAVEFORM: READ STRT/EOB FLAG TIMING

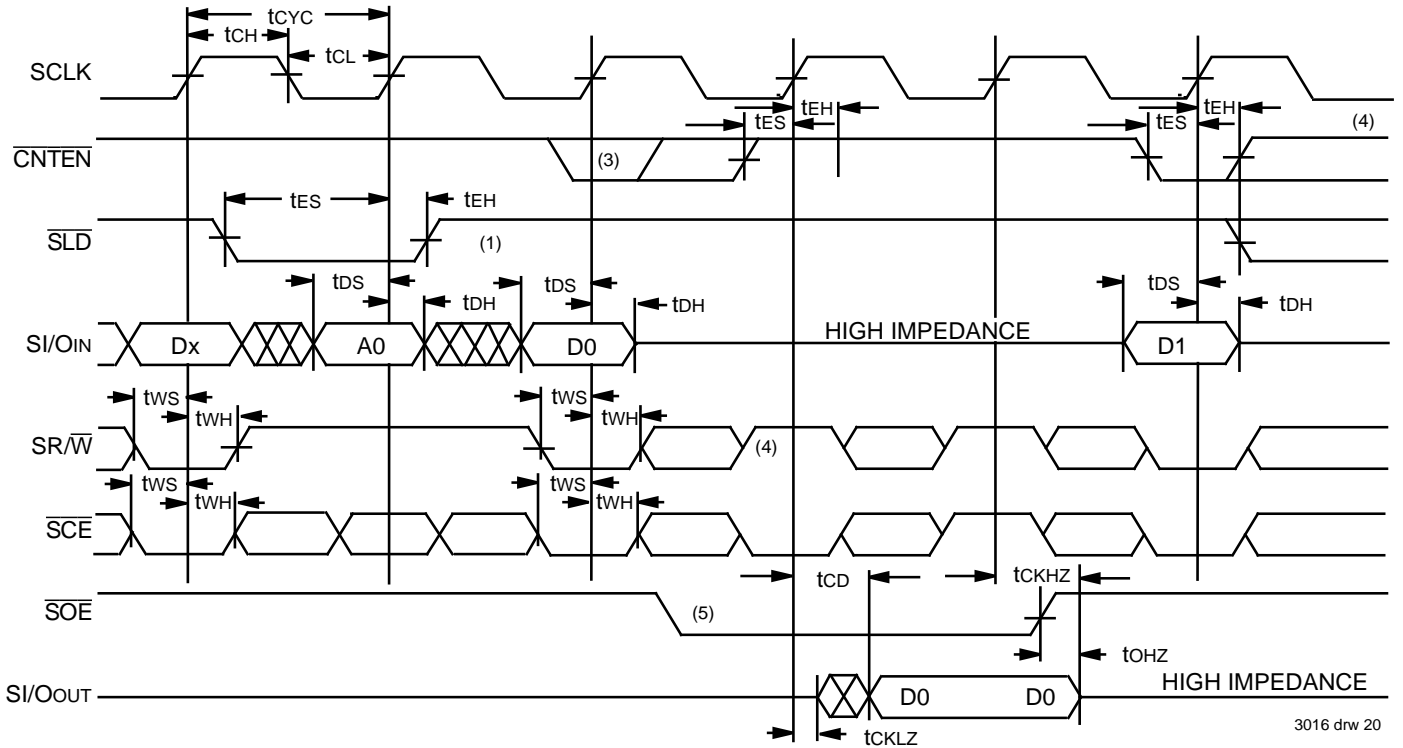


3016 drw 19

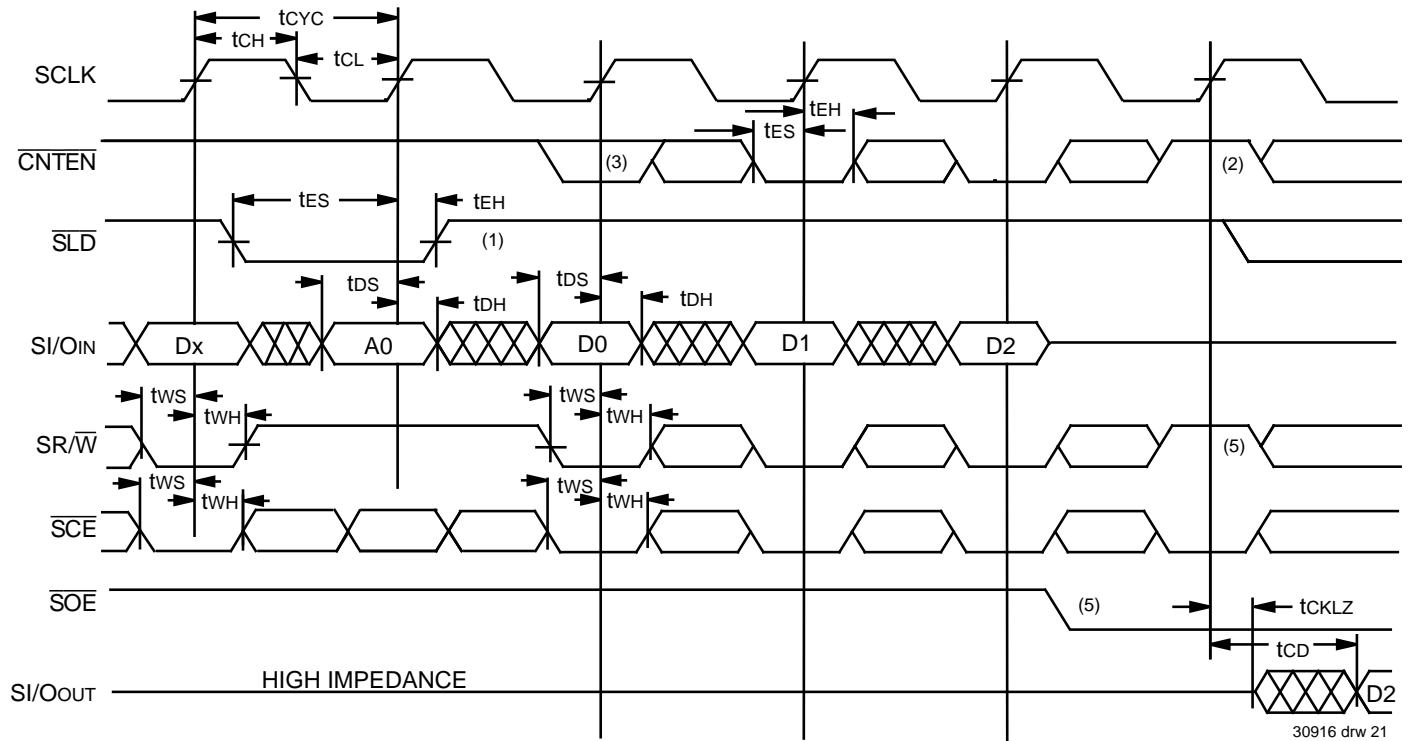
NOTES:

1. If \overline{SSTRT}_1 or $\overline{SSTRT}_2 = V_{IL}$, then address will be clocked in on the SCLK's rising edge.
2. If $CNTEN = V_{IH}$ for the SCLK's rising edge, the internal address counter will not advance.
3. \overline{SOE} will control the output and should be High on Power-Up. If $\overline{SCE} = V_{IL}$ and is clocked in while $SR/\overline{W} = V_{IH}$, the data addressed will be read out within that cycle. If $\overline{SCE} = V_{IL}$ and is clocked in while $SR/\overline{W} = V_{IL}$, the data addressed will be written to if the last cycle was a Read. \overline{SOE} may be used to control the bus contention and permit a Write on this cycle.
4. Unlike SLD case, \overline{CNTEN} is not disabled on cycle immediately following \overline{SSTRT} .
5. If $SR/\overline{W} = V_{IL}$, data would be written to D0 again since $\overline{CNTEN} = V_{IH}$.
6. $\overline{SOE} = V_{IL}$ makes no difference at this point since the $SR/\overline{W} = V_{IL}$ disables the output until $SR/\overline{W} = V_{IH}$ is clocked in on the next rising clock edge.

SEQUENTIAL PORT WAVEFORM: WRITE CYCLES



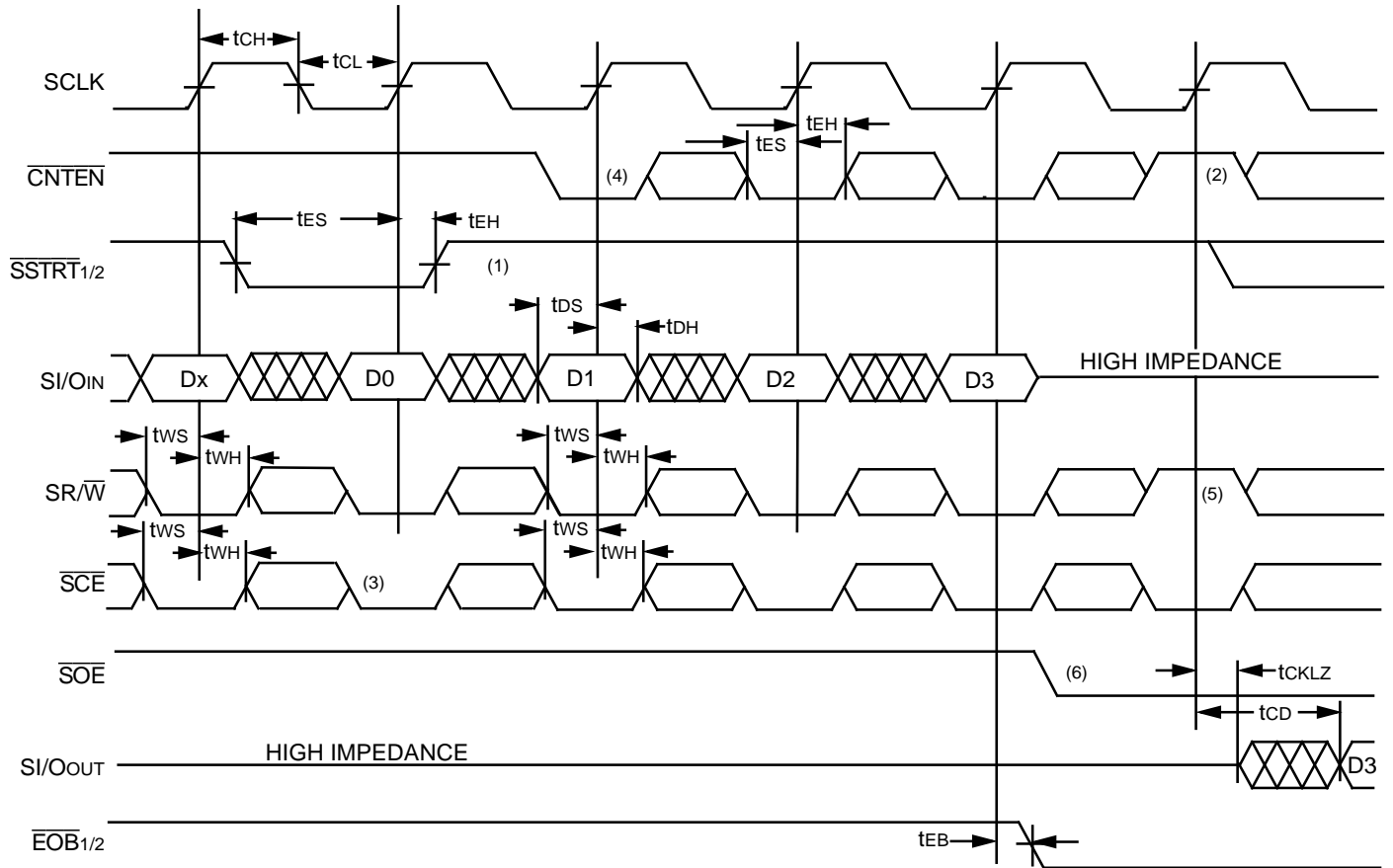
SEQUENTIAL PORT WAVEFORM: BURST WRITE CYCLES



NOTES :

1. If $\overline{SLD} = V_{IL}$, then address will be clocked in on the SCLK's rising edge.
2. If $CNTEN = V_{IH}$ for the SCLK's rising edge, the internal address counter will not advance.
3. Pointer is not incrementing on cycle immediately following \overline{SLD} even if $CNTEN$ is Low.
4. If $SR/\overline{W} = V_{IL}$, data would be written to D0 again since $CNTEN = V_{IH}$.
5. $\overline{SOE} = V_{IL}$ makes no difference at this point since the $SR/\overline{W} = V_{IL}$ disables the output until $SR/\overline{W} = V_{IH}$ is clocked in on the next rising clock edge.

SEQUENTIAL PORT WAVEFORM: WRITE CYCLES (STRT/EOB FLAG TIMING)

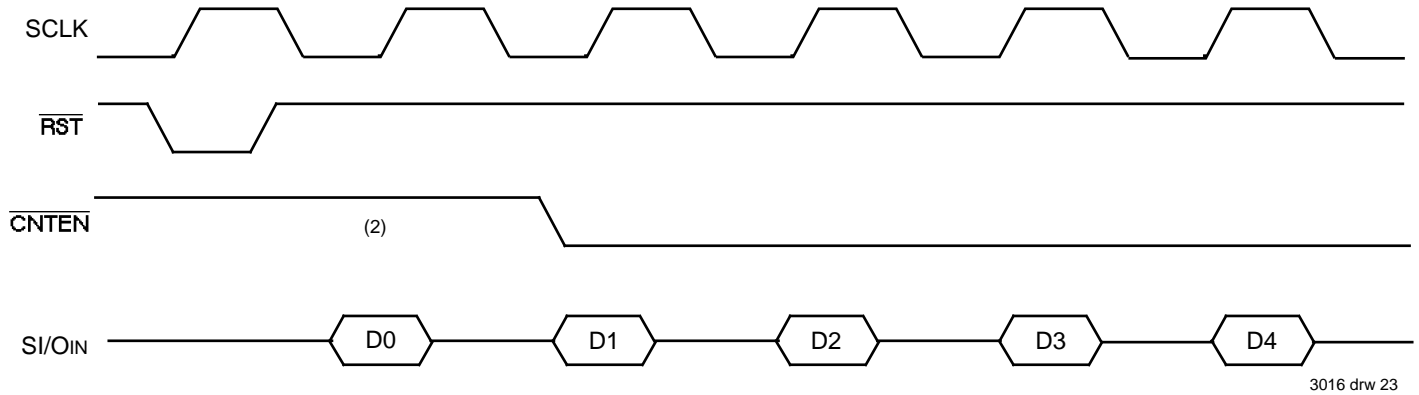


3016 drw 22

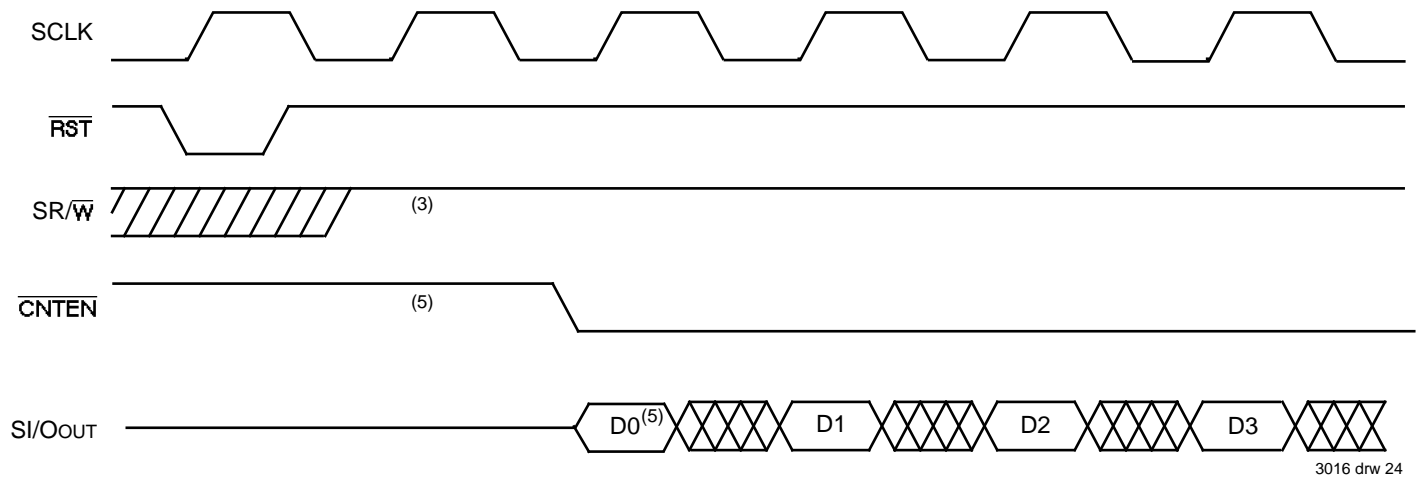
NOTES:

1. If \overline{SSTRT}_1 or $\overline{SSTRT}_2 = V_{IL}$, then address will be clocked in on the SCLK's rising edge.
2. If $\overline{CNTEN} = V_{IH}$ for the SCLK's rising edge, the internal address counter will not advance.
3. \overline{SOE} will control the output and should be High on Power-Up. If $\overline{SCE} = V_{IL}$ and is clocked in while $\overline{SR/W} = V_{IH}$, the data addressed will be read out within that cycle. If $\overline{SCE} = V_{IL}$ and is clocked in while $\overline{SR/W} = V_{IL}$, the data addressed will be written to if the last cycle was a Read. \overline{SOE} may be used to control the bus contention and permit a Write on this cycle.
4. Unlike SLD case, \overline{CNTEN} is not disabled on cycle immediately following \overline{SSTRT} .
5. If $\overline{SR/W} = V_{IL}$, data would be written to D0 again since $\overline{CNTEN} = V_{IH}$.
6. $\overline{SOE} = V_{IL}$ makes no difference at this point since the $\overline{SR/W} = V_{IL}$ disables the output until $\overline{SR/W} = V_{IH}$ is clocked in on the next rising clock edge.

SEQUENTIAL COUNTER ENABLE CYCLE AFTER RESET, WRITE CYCLE^(2, 4, 6)



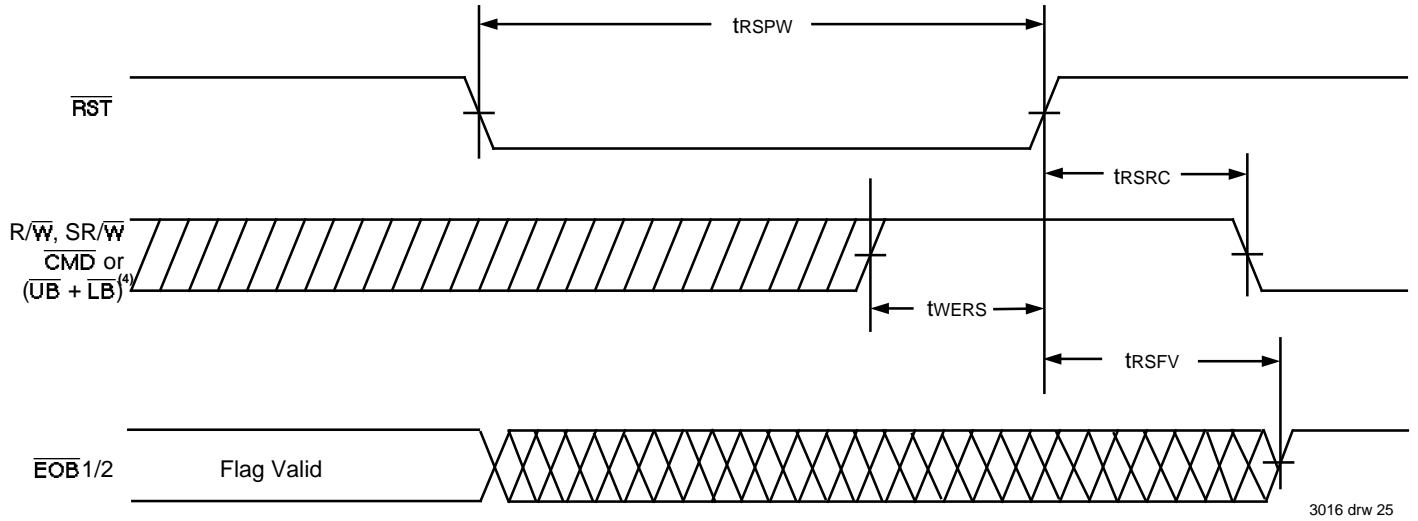
SEQUENTIAL COUNTER ENABLE CYCLE AFTER RESET, READ CYCLE^(2, 4)



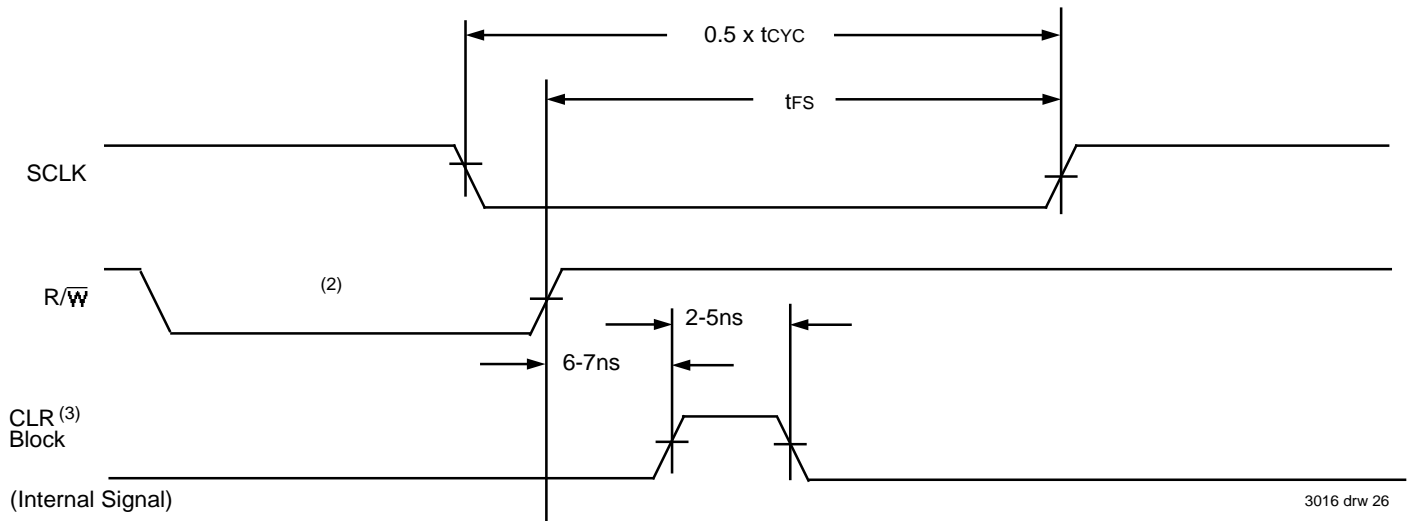
NOTES:

1. 'D0' represents data input for Address=0, 'D1' represents data input for Address=1, etc.
1. If $\overline{\text{CNTEN}} = \text{VIL}$ then 'D1' would be written into 'A1' at this point.
3. Data output is available at t_{CD} after the $\overline{\text{SR}}/\overline{\text{W}} = \text{VIH}$ is clocked. The $\overline{\text{RST}}$ sets $\overline{\text{SR}}/\overline{\text{W}} = \text{Low}$ internally and therefore disables the output until the next clock.
4. $\overline{\text{SCE}} = \text{VIL}$ throughout all cycles.
5. If $\overline{\text{CNTEN}} = \text{VIL}$ then 'D1' would be clocked out (read) at this point.
6. $\overline{\text{SR}}/\overline{\text{W}} = \text{VIL}$.

RANDOM ACCESS PORT WAVEFORM: RESET TIMING



RANDOM ACCESS PORT WAVEFORM: RESTART TIMING OF SEQUENTIAL PORT (1)



NOTES:

1. The sequential port is in the STOP mode and is being restarted from the random port by the Bit 4 Counter Release (see Case 5).
2. "0" is written to Bit 4 from the random port at address [A2 - A0] = 100, when $\overline{CMD} = V_{IL}$ and $\overline{CE} = V_{IH}$. The device is in the Buffer Command Mode (see Case 5).
3. CLR is an internal signal only and is shown for reference only.
4. Sequential port must also prohibit $\overline{SR/W}$ or \overline{SCE} from being low for t_{WERS} and t_{RSRC} periods, or SCLK must not toggle from Low-to-High until after t_{RSRC} .

