



Integrated Device Technology, Inc.

CMOS STATIC RAMs 64K (16K x 4-BIT) Added Chip Select and Output Controls

IDT7198S
IDT7198L

FEATURES:

- Fast Output Enable (\overline{OE}) pin available for added system flexibility
- Multiple Chip Selects (\overline{CS}_1 , \overline{CS}_2) simplify system design and operation
- High speed (equal access and cycle times)
— Military: 20/25/35/45/55/70/85ns (max.)
- Low power consumption
- Battery back-up operation—2V data retention (L version only)
- 24-pin CERDIP, high-density 28-pin leadless chip carrier, and 24-pin CERPACK packaging available
- Produced with advanced CMOS technology
- Bidirectional data inputs and outputs
- Inputs/outputs TTL-compatible
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7198 is a 65,536 bit high-speed static RAM orga-

nized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications.

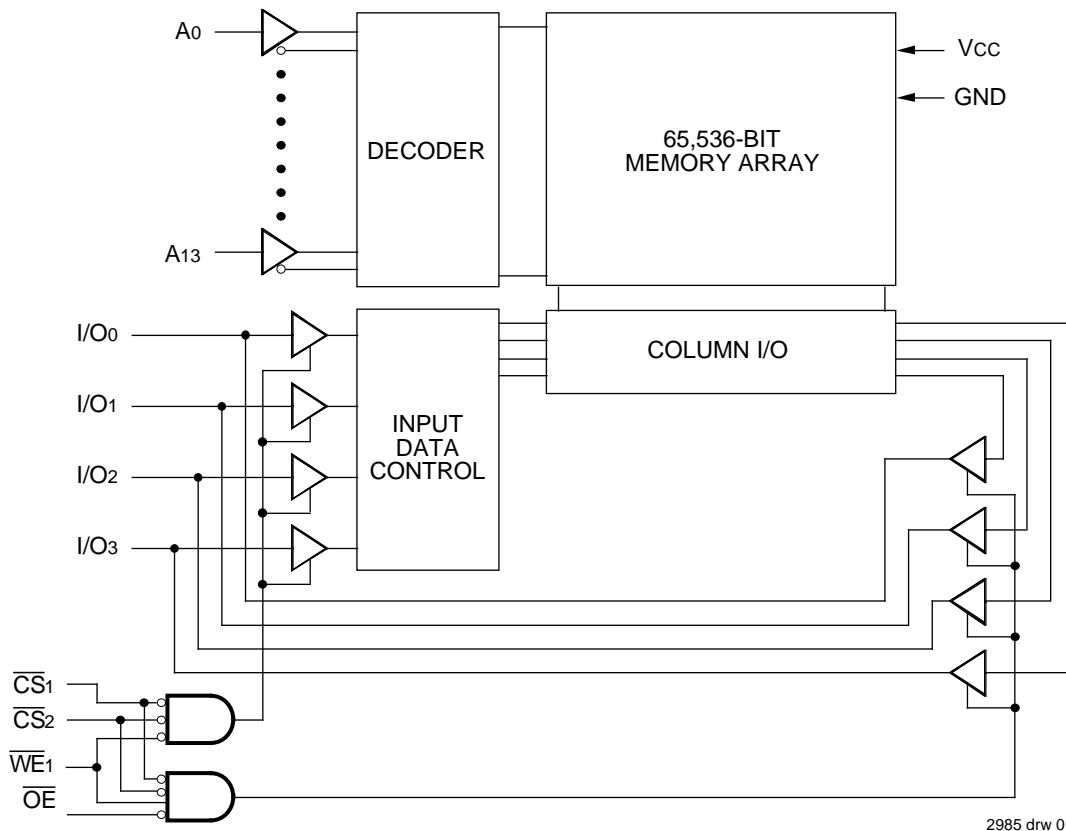
Access times as fast as 20ns are available. The IDT7198 offers a reduced power standby mode, ISB_1 , which is activated when \overline{CS}_1 or \overline{CS}_2 goes HIGH. This capability decreases power, while enhancing system reliability. The low-power version (L) also offers a battery backup data retention capability where the circuit typically consumes only 30 μ W when operating from a 2V battery.

All inputs and outputs are TTL-compatible and operate from a single 5V supply.

The IDT7198 is packaged in either a 24-pin ceramic DIP, 28-pin leadless chip carrier, and 24-pin CERPACK.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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MILITARY TEMPERATURE RANGE

MAY 1994

MEMORY CONTROL

The IDT7198 64K high-speed CMOS static RAM incorporates two additional memory control features (an extra chip select and an output enable pin) which offer additional benefits in many system memory applications.

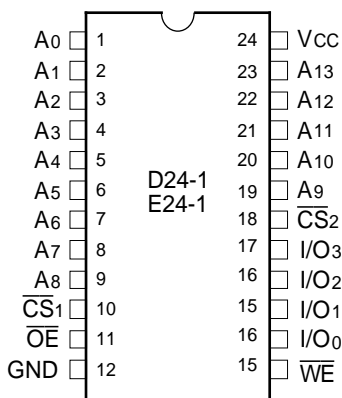
Both chip selects, Chip Select 1 (\overline{CS}_1) and Chip Select 2 (\overline{CS}_2), must be LOW to select the memory. If either chip select is pulled HIGH, the memory will be deselected and remain in the standby mode. This dual chip select feature (\overline{CS}_1 , \overline{CS}_2) also brings the convenience of improved system speeds to the large memory designer by reducing the external logic required to perform decoding.

PIN DESCRIPTIONS

Name	Description
A0–A13	Address Inputs
\overline{CS}_1	Chip Select 1
\overline{CS}_2	Chip Select 2
\overline{WE}	Write Enable
\overline{OE}	Output Enable
I/O0–I/O3	Data I/O
VCC	Power
GND	Ground

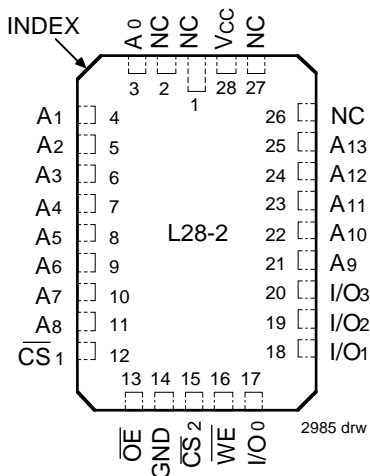
2985 tbl 01

PIN CONFIGURATIONS



2985 drw 02

DIP/SOJ/CERPACK
TOP VIEW



2985 drw 03

LCC
TOP VIEW

TRUTH TABLE⁽¹⁾

Mode	\overline{CS}_1	\overline{CS}_2	\overline{WE}	\overline{OE}	I/O	Power
Standby	H	X	X	X	High-Z	Standby
Standby	X	H	X	X	High-Z	Standby
Read	L	L	H	L	DOUT	Active
Write	L	L	L	X	DIN	Active
Read	L	L	H	H	High-Z	Active

NOTE:

1. H = V_{IH} , L = V_{IL} , X = don't care.

2985 tbl 02

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TA	Operating Temperature	-55 to +125	°C
TBIAS	Temperature Under Bias	-65 to +135	°C
TSTG	Storage Temperature	-65 to +150	°C
PT	Power Dissipation	1.0	W
IOUT	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2985 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	6.0	V
V _{IL}	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE: ^{2985 tbl 05}
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	V _{CC}
Military	-55°C to +125°C	0V	5V ± 10%

^{2985 tbl 06}

CAPACITANCE (T_A = +25°C, f = 1.0MHz, V_{CC} = 0V)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	7	pF
C _{I/O}	I/O Capacitance	V _{OUT} = 0V	7	pF

NOTE: ^{2985 tbl 04}
1. This parameter is determined by device characterization, but is not production tested.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%, Military Temperature Range Only

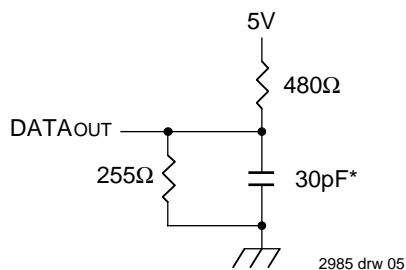
Symbol	Parameter	Test Condition	IDT7198S		IDT7198L		Unit
			Min.	Max.	Min.	Max.	
I _L	Input Leakage Current	V _{CC} = Max., V _{IN} = GND to V _{CC}	—	10	—	5	μA
I _{LO}	Output Leakage Current	V _{CC} = Max., $\overline{CS} = V_{IH}$, V _{OUT} = GND to V _{CC}	—	10	—	5	μA
V _{OL}	Output Low Voltage	I _{OL} = 10mA, V _{CC} = Min.	—	0.5	—	0.5	V
		I _{OL} = 8mA, V _{CC} = Min.	—	0.4	—	0.4	
V _{OH}	Output High Voltage	I _{OH} = -4mA, V _{CC} = Min.	2.4	—	2.4	—	V

^{2985 tbl 07}

AC TEST CONDITIONS

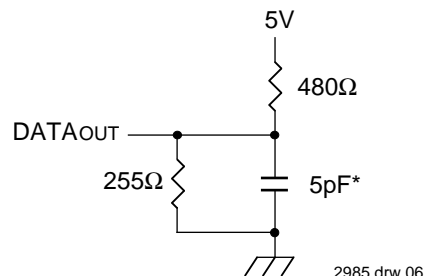
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

^{2985 tbl 10}



^{2985 drw 05}

Figure 1. AC Test Load



^{2985 drw 06}

Figure 2. AC Test Load
(for t_{CLZ1,2}, t_{OLZ}, t_{CHZ1,2}, t_{OHZ}, t_{OW} and t_{WHZ})

*Includes scope and jig capacitances

DC ELECTRICAL CHARACTERISTICS⁽¹⁾

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	7198S20	7198S25	7198S35	7198S45	7198S55/70	7198S85	Unit	
			7198L20	7198L25	7198L35	7198L45	7198L55/70	7198L85		
			Military	Military	Military	Military	Military	Military		
I _{CC1}	Operating Power Supply Current, \overline{CS}_1 and $\overline{CS}_2 \leq V_{IL}$, Outputs Open V _{CC} = Max., f = 0 ⁽²⁾	S	105	105	105	105	105	105	mA	
		L	80	80	80	80	80	80		
I _{CC2}	Dynamic Operating Current, \overline{CS}_1 and $\overline{CS}_2 \leq V_{IL}$, Outputs Open V _{CC} = Max., f = f _{MAX} ⁽²⁾	S	160	155	140	140	140	140	mA	
		L	130	120	115	110	110	105		
I _{SB}	Standby Power Supply Current (TTL Level), \overline{CS}_1 or $\overline{CS}_2 \geq V_{IH}$, V _{CC} = Max., Outputs Open, f = f _{MAX} ⁽²⁾	S	70	60	50	50	50	50	mA	
		L	50	40	35	35	35	35		
I _{SB1}	Full Standby Power Supply Current (CMOS Level) \overline{CS}_1 or $\overline{CS}_2 \geq V_{HC}$, V _{CC} = Max., V _{IN} ≥ V _{HC} or V _{IN} ≤ V _{LC} , f = 0 ⁽²⁾	S	25	20	20	20	20	20	mA	
		L	1.5	1.5	1.5	1.5	1.5	1.5		

NOTES:

- All values are maximum guaranteed values.
- At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/trc. f = 0 means no input lines change.

2985 tbl 06

DATA RETENTION CHARACTERISTICS OVER MILITARY TEMPERATURE RANGE

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

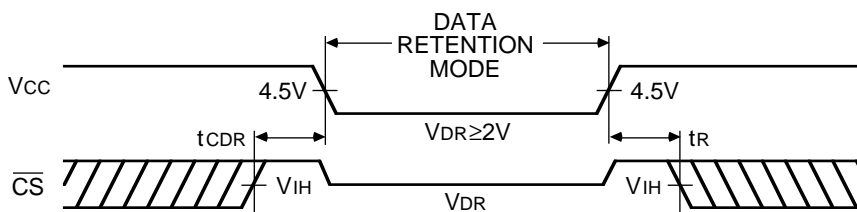
Symbol	Parameter	Test Condition	Min.	Typ. ⁽¹⁾ V _{CC} @		Max. V _{CC} @		Unit
				2.0v	3.0V	2.0V	3.0V	
V _{DR}	V _{CC} for Data Retention	—	2.0	—	—	—	—	V
I _{CCDR}	Data Retention Current	\overline{CS}_1 or $\overline{CS}_2 \geq V_{HC}$ V _{IN} ≥ V _{HC} or ≤ V _{LC}	—	10	15	600	900	μA
t _{CDR} ⁽³⁾	Chip Deselect to Data Retention Time		0	—	—	—	—	ns
t _R ⁽³⁾	Operation Recovery Time		t _{RC} ⁽²⁾	—	—	—	—	ns
I _{LI} ⁽³⁾	Input Leakage Current		—	—	—	2	2	μA

NOTES:

- T_A = +25°C.
- t_{RC} = Read Cycle Time.
- This parameter is guaranteed by device characterization but is not production tested.

2985 tbl 09

LOW V_{CC} DATA RETENTION WAVEFORM



2985 drw 04

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0V \pm 10\%$, Military Temperature Range)

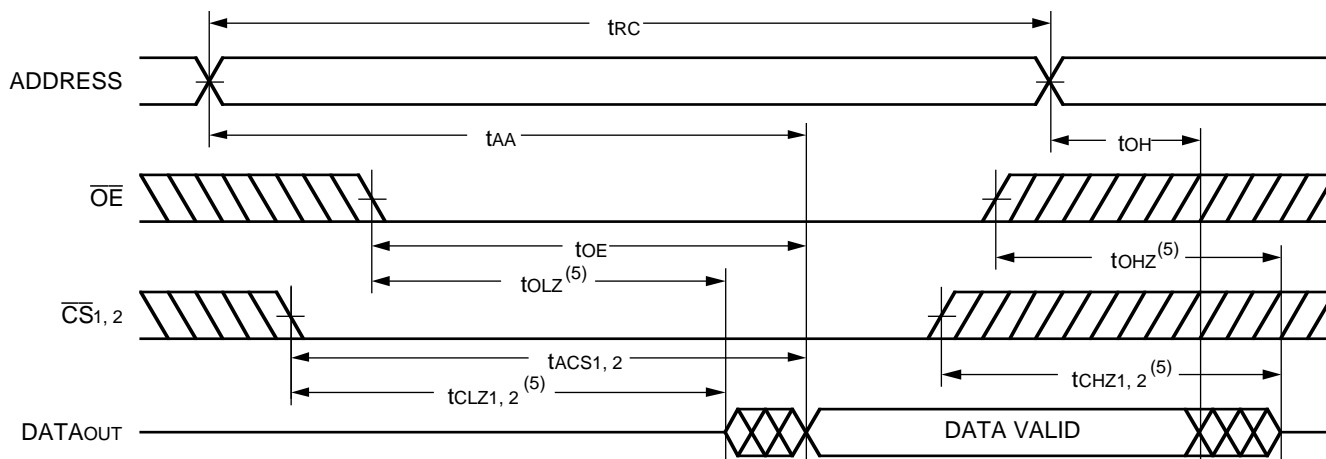
Symbol	Parameter	7198S20 7198L20		7198S25 7198L25		7198S35/45 7198L35/45		7198S55 7198L55		7198S70 7198L70		7198S85 7198L85		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle														
t _{RC}	Read Cycle Time	20	—	25	—	35/45	—	55	—	70	—	85	—	ns
t _{AA}	Address Access Time	—	19	—	25	—	35/45	—	55	—	70	—	85	ns
t _{ACS1,2} ⁽¹⁾	Chip Select-1,2 Access Time	—	20	—	25	—	35/45	—	55	—	70	—	85	ns
t _{CLZ1,2} ⁽²⁾	Chip Select-1,2 to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
t _{OE}	Output Enable to Output Valid	—	9	—	11	—	20/25	—	35	—	45	—	55	ns
t _{OLZ} ⁽²⁾	Output Enable to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
t _{CHZ1,2} ⁽²⁾	Chip Select 1,2 to Output in High-Z	—	8	—	10	—	14	—	20	—	25	—	30	ns
t _{OHZ} ⁽²⁾	Output Disable to Output in High-Z	—	8	—	9	—	15	—	20	—	25	—	30	ns
t _{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
t _{PU} ⁽²⁾	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t _{PD} ⁽²⁾	Chip Deselect to Power Down Time	—	20	—	25	—	35/45	—	55	—	70	—	85	ns

NOTES:

- Both chip selects must be active low for the device to be selected.
- This parameter is guaranteed by device characterization but is not production tested.

2985 tbl 11

TIMING WAVEFORM OF READ CYCLE NO. 1⁽¹⁾

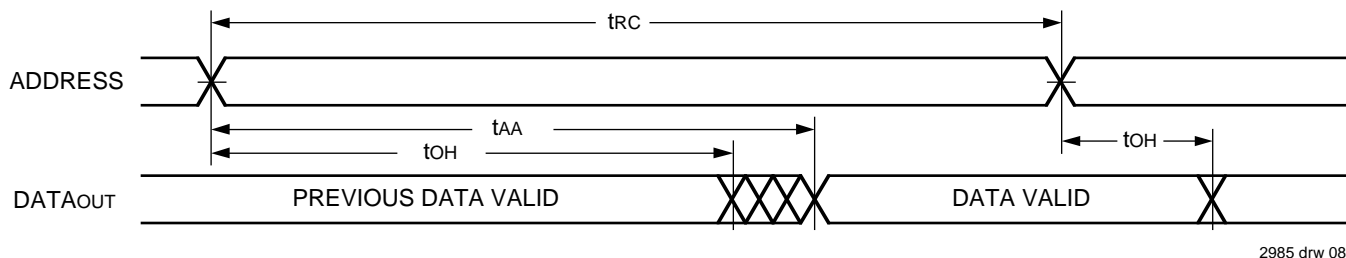


2985 drw 07

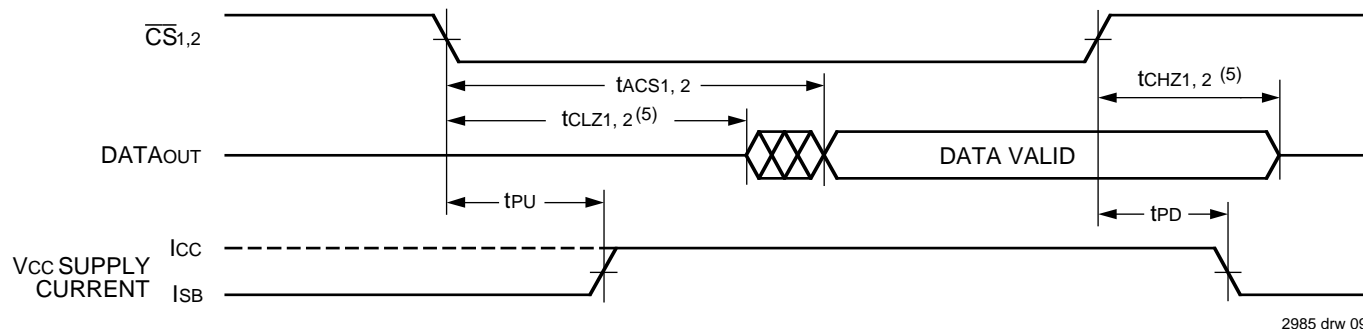
NOTES:

- \overline{WE} is HIGH for Read cycle.
- Device is continuously selected, $\overline{CS1}$ is LOW, $\overline{CS2}$ is LOW.
- Address valid prior to or coincident with $\overline{CS1}$ and or $\overline{CS2}$ transition LOW.
- \overline{OE} is LOW.
- Transition is measured $\pm 200mV$ from steady state voltage.

TIMING WAVEFORM OF READ CYCLE NO. 2^(1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3^(1, 3, 4)



NOTES:

1. \overline{WE} is HIGH for Read cycle.
2. Device is continuously selected, $\overline{CS1}$ is LOW, $\overline{CS2}$ is LOW.
3. Address valid prior to or coincident with $\overline{CS1}$ and or $\overline{CS2}$ transition LOW.
4. \overline{OE} is LOW.
5. Transition is measured $\pm 200mV$ from steady state voltage.

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0V \pm 10\%$, All Temperature Ranges)

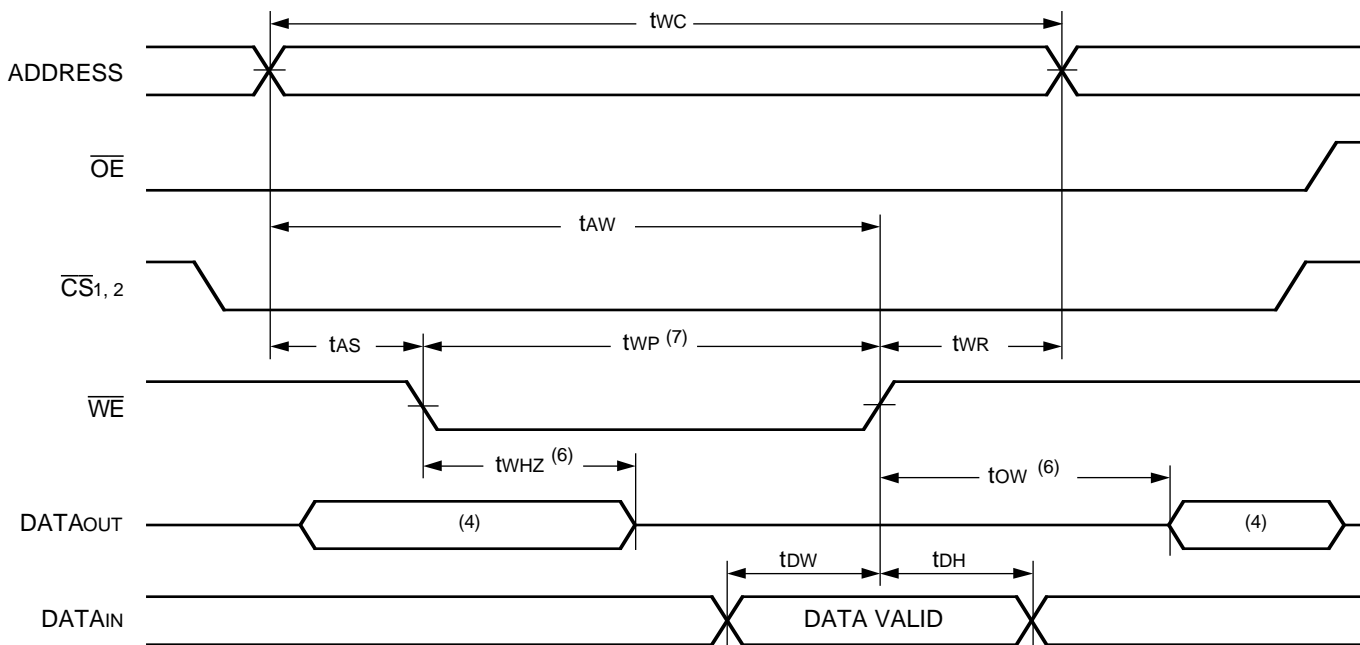
Symbol	Parameter	7198S20 7198L20		7198S25 7198L25		7198S35/45 7198L35/45		7198S55 7198L55		7198S70 7198L70		7198S85 7198L85		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle														
tWC	Write Cycle Time	17	—	20	—	30/40	—	50	—	60	—	75	—	ns
tCW _{1,2} ⁽¹⁾	Chip Select to End-of-Write	17	—	20	—	25/35	—	50	—	60	—	75	—	ns
tAW	Address Valid to End-of-Write	17	—	20	—	25/35	—	50	—	60	—	75	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	17	—	20	—	25/35	—	50	—	60	—	75	—	ns
tWR _{1,2}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWHZ ⁽²⁾	Write Enable to Output in High-Z	—	5/6	—	7	—	10/15	—	25	—	30	—	40	ns
tDW	Data Valid to End-of-Write	10	—	13	—	15/20	—	25	—	30	—	35	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tOW ⁽²⁾	Output Active from End-of-Write	5	—	5	—	5	—	5	—	5	—	5	—	ns

NOTES:

1. Both chip selects must be active low for the device to be selected.
2. This parameter is guaranteed by device characterization but is not production tested.

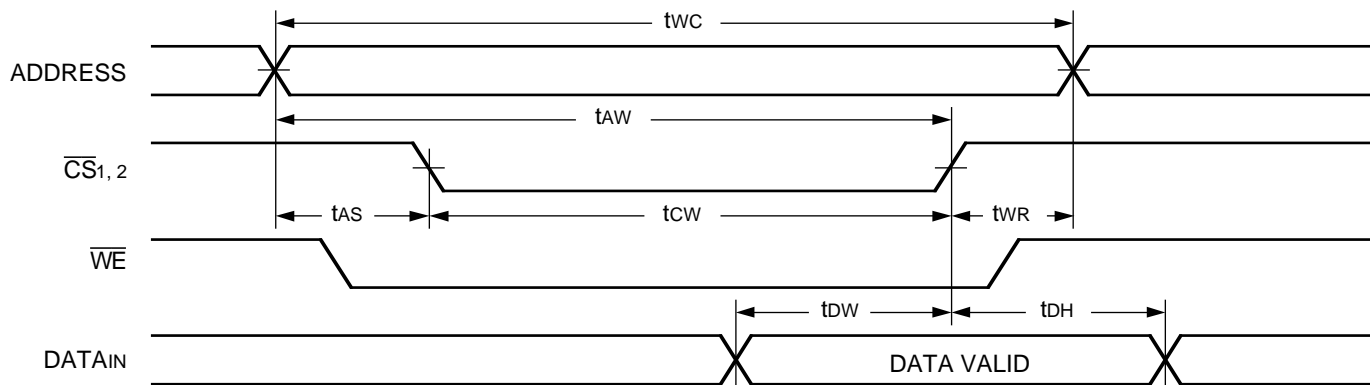
2985 tbl 12

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} CONTROLLED TIMING)^(1, 2, 3, 7)



2985 drw 10

TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CS} CONTROLLED TIMING)⁽¹⁾

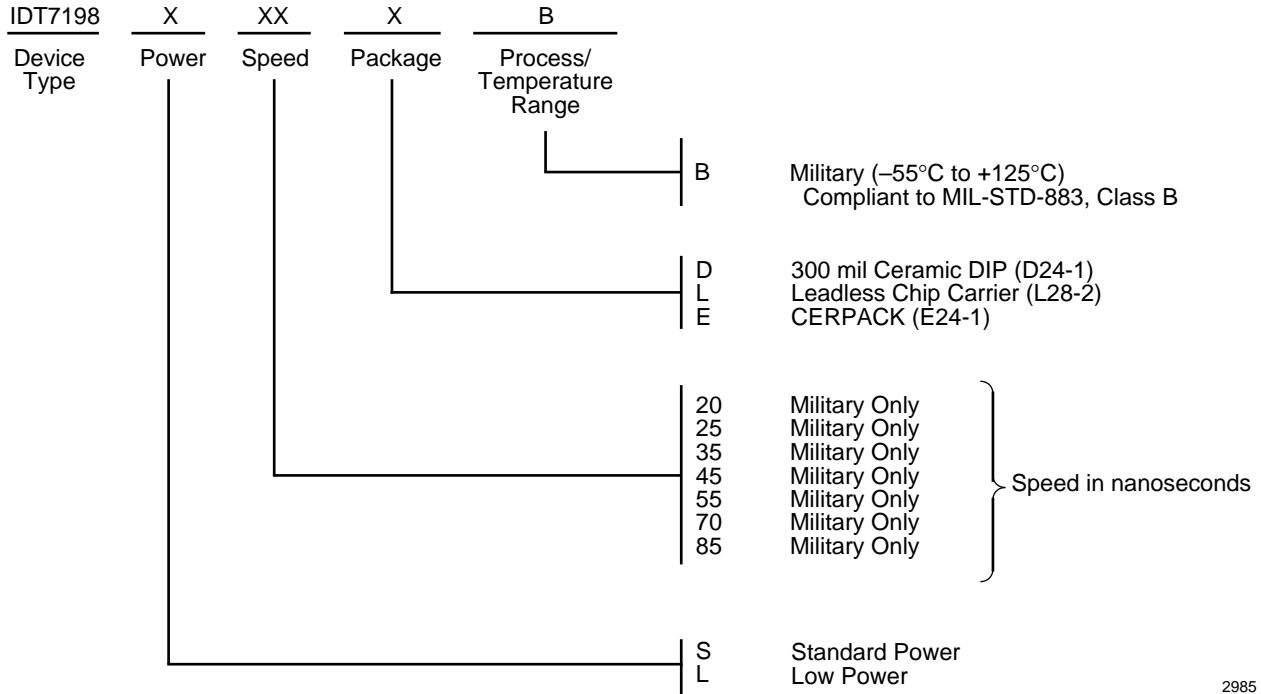


2985 drw 11

NOTES:

1. \overline{WE} , \overline{CS}_1 or \overline{CS}_2 must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a LOW \overline{WE} , a LOW \overline{CS}_1 and a LOW \overline{CS}_2 .
3. t_{WR} is measured from the earlier of \overline{CS}_1 , \overline{CS}_2 or \overline{WE} going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the CS LOW transition occurs simultaneously with or after the \overline{WE} LOW transition, outputs remain in the high-impedance state.
6. Transition is measured $\pm 200\text{mV}$ from steady state.
7. If \overline{OE} is LOW during a \overline{WE} controlled write cycle, the write pulse width must be the larger of t_{WP} or $(t_{WHZ} + t_{DW})$ to allow the I/O drivers to turn off and data to be placed on the required t_{DW} . If \overline{OE} is HIGH during a \overline{WE} controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} .

ORDERING INFORMATION



2985 drw 12