



Integrated Device Technology, Inc.

# CMOS PARALLEL-TO-SERIAL FIFO

2048 x 9

4096 x 9

IDT72131

IDT72141

## FEATURES:

- 35ns parallel port access time, 45ns cycle time
- 50MHz serial port shift rate
- Expandable in depth and width with no external components
- Programmable word lengths including 7-9, 16-18, 32-36 bit using Flexishift™ serial output without using any additional components
- Multiple status flags: Full, Almost-Full (1/8 from full), Half-Full, Almost Empty (1/8 from empty), and Empty
- Asynchronous and simultaneous read and write operations
- Dual-Port zero fall-through architecture
- Retransmit capability in single device mode
- Produced with high-performance, low power CMOS technology
- Available in 28-pin plastic DIP
- Industrial temperature range (-40°C to +85°C) is available, tested to military electrical specifications

## DESCRIPTION:

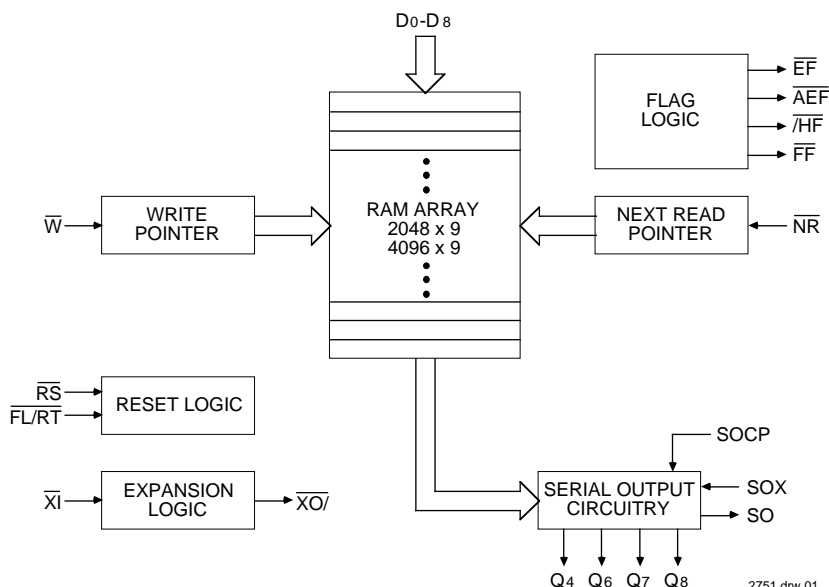
The IDT72131/72141 are high-speed, low power parallel-to-serial FIFOs. These FIFOs are ideally suited to serial communications applications, tape/disk controllers, and local area networks (LANs). The IDT72131/72141 can be configured with the IDT's serial-to-parallel FIFOs (IDT72132/72142) for bidirectional serial data buffering.

The FIFO has a 9-bit parallel input port and a serial output port. Wider and deeper parallel-to-serial data buffers can be built using multiple IDT72131/72141 chips. IDT's unique Flexishift serial expansion logic (SOX,  $\overline{NR}$ ) makes width expansion possible with no additional components. These FIFOs will expand to a variety of word widths including 8, 9, 16, and 32 bits. The IDT72131/141 can also be directly connected for depth expansion.

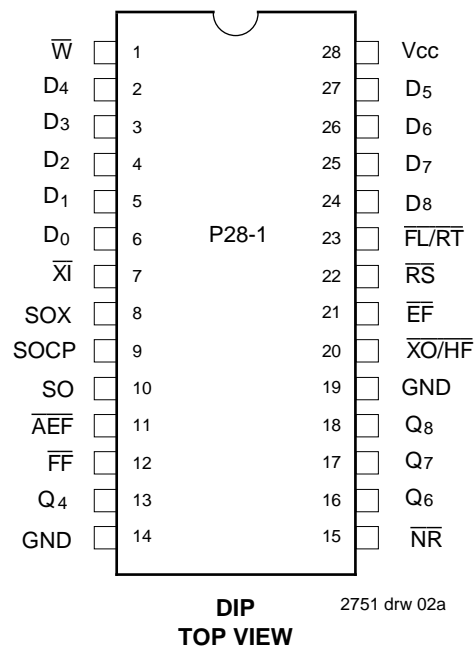
Five flags are provided to monitor the FIFO. The full and empty flags prevent any FIFO data overflow or underflow conditions. The almost-full (7/8), half-full, and almost empty (1/8) flags signal memory utilization within the FIFO.

The IDT72131/72141 is fabricated using IDT's high-speed submicron CMOS technology.

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



The IDT logo is a registered trademark of Integrated Device Technology, Inc.

## PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D <sub>0</sub> –D <sub>8</sub>	Inputs	I	Data inputs for 9-bit wide data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set LOW, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{HF}$ and $\overline{FF}$ go HIGH, and $\overline{AEF}$ and $\overline{EF}$ go LOW. A reset is required before an initial WRITE after power-up. $\overline{W}$ must be HIGH and SOCP must be LOW during $\overline{RS}$ cycle.
$\overline{W}$	Write	I	A write cycle is initiated on the falling edge of WRITE if the Full Flag ( $\overline{FF}$ ) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of WRITE. Data is stored in the RAM array sequentially and independently of any ongoing read operation.
SOCP	Serial Output Clock	I	A serial bit read cycle is initiated on the rising edge of SOCP if the Empty Flag ( $\overline{EF}$ ) is not set. In both Depth and Serial Word Width Expansion modes, all of the SOCP pins are tied together.
$\overline{NR}$	Next Read	I	To program the Serial Out data word width, connect $\overline{NR}$ with one of the Data Set pins (Q <sub>4</sub> , Q <sub>6</sub> , Q <sub>7</sub> and Q <sub>8</sub> ). For example, $\overline{NR}$ - Q <sub>7</sub> programs for a 8-bit Serial Out word width.
$\overline{FL/RT}$	First Load/ Retransmit	I	This is a dual purpose input. In the single device configuration ( $\overline{XI}$ grounded), activating retransmit ( $\overline{FL/RT}$ -LOW) will set the internal READ pointer to the first location. There is no effect on the WRITE pointer. $\overline{W}$ must be high and SOCP must be low before setting $\overline{FL/RT}$ LOW. Retransmit is not compatible with depth expansion. In the depth expansion configuration, $\overline{FL/RT}$ grounded indicates the first activated device.
$\overline{XI}$	Expansion In	I	In the single device configuration, $\overline{XI}$ is grounded. In depth expansion or daisy chain expansion, $\overline{XI}$ is connected to $\overline{XO}$ (expansion out) of the previous device.
SOX	Serial Output Expansion	I	In the Serial Output Expansion mode, the SOX pin of the least significant device is tied HIGH. The SOX pin of all other devices is connected to the Q <sub>8</sub> pin of the previous device. Data is then clocked out least significant bit first. For single device operation, SOX is tied HIGH.
SO	Serial Output	O	Serial data is output on the Serial Output (SO) pin. Data is clocked out Least Significant Bit first. In the Serial Width Expansion mode the SO pins are tied together and each SO pin is tristated at the end of the byte.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ goes LOW, the device is full and further WRITE operations are inhibited. When $\overline{FF}$ is HIGH, the device is not full.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ goes LOW, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is HIGH, the device is not empty. See the description on page 6 for more details.
$\overline{AEF}$	Almost-Empty/ Almost-Full Flag	O	When $\overline{AEF}$ is LOW, the device is empty to 1/8 full or 7/8 to completely full. When $\overline{AEF}$ is HIGH, the device is greater than 1/8 full, but less than 7/8 full.
$\overline{XO/HF}$	Expansion Out/ Half-Full Flag	O	This is a dual-purpose output. In the single device configuration ( $\overline{XI}$ grounded), the device is more than half full when HF is LOW. In the depth expansion configuration ( $\overline{XO}$ connected to $\overline{XI}$ of the next device), a pulse is sent from $\overline{XO}$ to $\overline{XI}$ when the last location in the RAM array is filled.
Q <sub>4</sub> , Q <sub>6</sub> , Q <sub>7</sub> and Q <sub>8</sub>	Data Set	O	The appropriate Data Set pin (Q <sub>4</sub> , Q <sub>6</sub> , Q <sub>7</sub> and Q <sub>8</sub> ) is connected to $\overline{NR}$ to program the Serial Out data word width. For example: Q <sub>6</sub> - $\overline{NR}$ programs a 7-bit word width, Q <sub>8</sub> - $\overline{NR}$ programs a 9-bit word width, etc.
V <sub>CC</sub>	Power Supply		Single Power Supply of 5V.
GND	Ground		Single ground at 0V.

2751 tbl 01

## STATUS FLAGS

Number of Words in FIFO		$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
IDT72131	IDT72141				
0	0	H	L	H	L
1-255	1-511	H	L	H	H
256-1024	512-2048	H	H	H	H
1025-1792	2049-3584	H	H	L	H
1793-2047	3585-4095	H	L	L	H
2048	4096	L	L	L	H

2751 tbl 02

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	50	mA

**NOTE:** 2751 tbl 03

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage Commercial	2.0	—	—	V
VIL <sup>(1)</sup>	Input Low Voltage	—	—	0.8	V

**NOTE:** 2751 tbl 04

- 1.5V undershoots are allowed for 10ns once per cycle.

### CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	10	pF
COUT	Output Capacitance	VOUT = 0V	12	pF

**NOTE:** 2751 tbl 05

- This parameter is sampled and not 100% tested.

### DC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 5.0V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	IDT72131/IDT72141 Commercial			Unit
		Min.	Typ.	Max.	
IIL <sup>(1)</sup>	Input Leakage Current (Any Input)	-1	—	1	μA
IOL <sup>(2)</sup>	Output Leakage Current	-10	—	10	μA
VOH	Output Logic "1" Voltage, IOUT = -8mA	2.4	—	—	V
VOL	Output Logic "0" Voltage IOUT = 16mA	—	—	0.4	V
ICC1 <sup>(3)</sup>	Power Supply Current	—	90	140	mA
ICC2 <sup>(3)</sup>	Average Standby Current (W = RS = FL/RT = VIH) (SOCP = VIL)	—	8	12	mA
ICC3(L) <sup>(3,4)</sup>	Power Down Current	—	—	2	mA

**NOTES:** 2751 tbl 06

- Measurements with  $0.4 \leq V_{IN} \leq V_{CC}$ .
- $SOCP \leq V_{IL}$ ,  $0.4 \leq V_{OUT} \leq V_{CC}$ .
- ICC measurements are made with outputs open.
- $RS = FL/RT = W = V_{CC} - 0.2V$ ;  $SOCP \leq 0.2V$ ; all other inputs  $\geq V_{CC} - 0.2V$  or  $\leq 0.2V$ .

## AC ELECTRICAL CHARACTERISTICS

(Commercial:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = 0^{\circ}C$  to  $+70^{\circ}C$ )

Symbol	Parameter	Commercial				Unit
		IDT72131L35 IDT72141L35		IDT72131L50 IDT72141L50		
		Min.	Max.	Min.	Max.	
tS	Parallel Shift Frequency	—	22.2	—	15	MHz
tSOCP	Serial-Out Shift Frequency	—	50	—	40	MHz
<b>PARALLEL INPUT TIMINGS</b>						
tDS	Data Set-up Time	18	—	30	—	ns
tDH	Data Hold Time	0	—	5	—	ns
tWC	Write Cycle Time	45	—	65	—	ns
tWPW	Write Pulse Width	35	—	50	—	ns
tWR	Write Recovery Time	10	—	15	—	ns
tWEF	Write High to $\overline{EF}$ HIGH	—	30	—	45	ns
tWFF	Write Low to $\overline{FF}$ LOW	—	30	—	45	ns
tWF	Write Low to Transitioning $\overline{HF}$ , $\overline{AEF}$	—	45	—	65	ns
tWPF	Write Pulse Width After $\overline{FF}$ HIGH	35	—	50	—	ns
<b>SERIAL OUTPUT TIMINGS</b>						
tSOHZ	SOCP Rising Edge to SO at High-Z <sup>(1)</sup>	5	16	5	26	ns
tSOLZ	SOCP Rising Edge to SO at Low-Z <sup>(1)</sup>	5	22	5	22	ns
tSOPD	SOCP Rising Edge to Valid Data on SO	—	18	—	18	ns
tSOX	SOX Set-up Time to SOCP Rising Edge	5	—	5	—	ns
tSOCW	Serial In Clock Width HIGH/LOW	8	—	10	—	ns
tSOCEF	SOCP Rising Edge (Bit 0 - Last Word) to $\overline{EF}$ LOW	—	20	—	25	ns
tSOCFF	SOCP Rising Edge to $\overline{FF}$ HIGH	—	30	—	40	ns
tSOCF	SOCP Rising Edge to $\overline{HF}$ , $\overline{AEF}$ , HIGH	—	30	—	40	ns
tREFSO	Recovery Time SOCP After $\overline{EF}$ HIGH	35	—	50	—	ns
<b>RESET TIMINGS</b>						
tRSC	Reset Cycle Time	45	—	65	—	ns
tRS	Reset Pulse Width	35	—	50	—	ns
tRSS	Reset Set-up Time	35	—	50	—	ns
tRSR	Reset Recovery Time	10	—	15	—	ns
tRSF1	Reset to $\overline{EF}$ and $\overline{AEF}$ LOW	—	45	—	65	ns
tRSF2	Reset to $\overline{HF}$ and $\overline{FF}$ HIGH	—	45	—	65	ns
tRSQLOW	Reset to Q LOW	20	—	35	—	ns
tRSQHIGH	Reset to Q HIGH	20	—	35	—	ns
<b>RETRANSMIT TIMINGS</b>						
tRTC	Retransmit Cycle Time	45	—	65	—	ns
tRT	Retransmit Pulse Width	35	—	50	—	ns
tRTS	Retransmit Set-up Time	35	—	50	—	ns
tRTR	Retransmit Recovery Time	10	—	15	—	ns
<b>DEPTH EXPANSION MODE TIMINGS</b>						
txOL	Read/Write to $\overline{XO}$ LOW	—	35	—	50	ns
txOH	Read/Write to $\overline{XO}$ HIGH	—	35	—	50	ns
txI	$\overline{XI}$ Pulse Width	35	—	50	—	ns
txIR	$\overline{XI}$ Recovery Time	10	—	10	—	ns
txIS	$\overline{XI}$ Set-up Time	15	—	15	—	ns

**NOTE:**

1. Guaranteed by design minimum times, not tested.

2751 tbl 07

### AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure A

2751 tbl 08

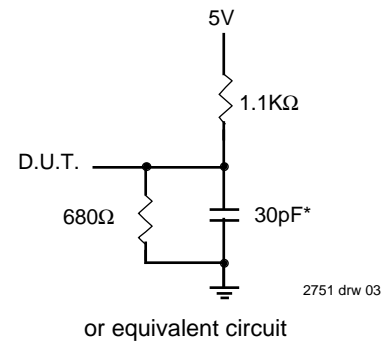


Figure A. Output Load

\*Including jig and scope capacitances

### FUNCTIONAL DESCRIPTION

#### Parallel Data Input

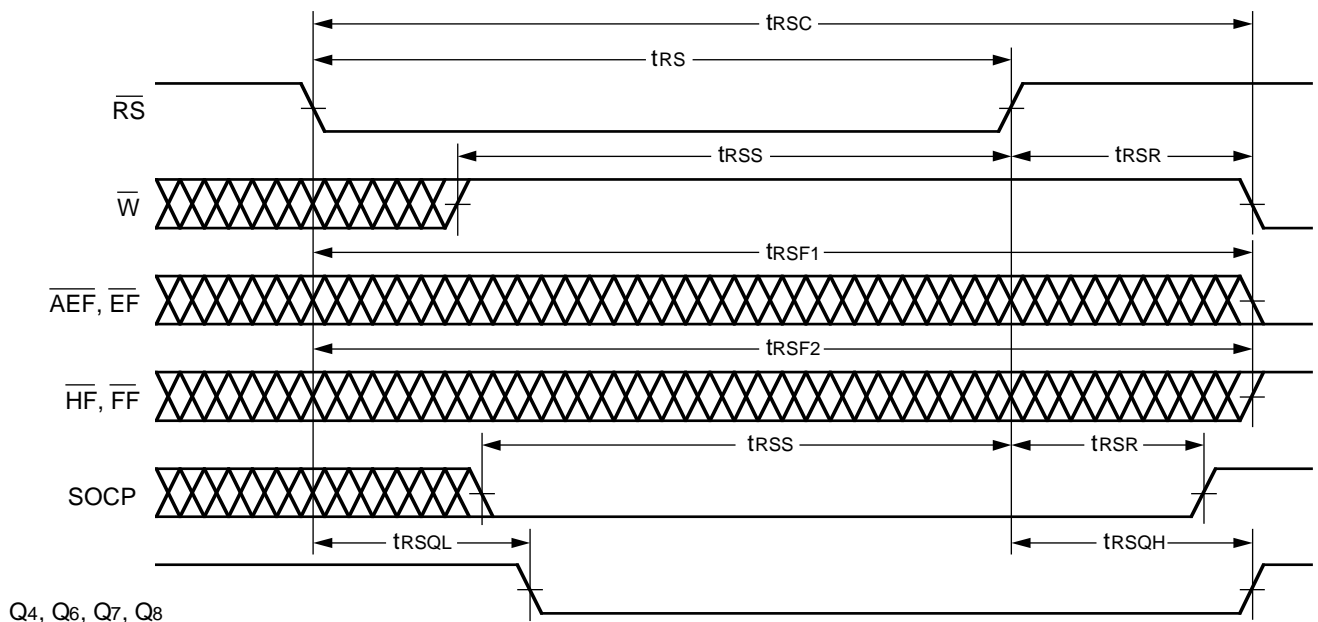
The data is written into the FIFO in parallel through the D0-8 input data lines. A write cycle is initiated on the falling edge of the Write ( $\overline{W}$ ) signal provided the Full Flag ( $\overline{FF}$ ) is not asserted. If the  $\overline{W}$  signal changes from HIGH-to-LOW and the Full-Flag ( $\overline{FF}$ ) is already set, the write line is inhibited internally from incrementing the write pointer and no write operation occurs.

Data set-up and hold times must be met with respect to the rising edge of Write. The data is written to the RAM at the write pointer. On the rising edge of  $\overline{W}$ , the write pointer is incremented. Write operations can occur simultaneously or asynchronously with read operations.

#### Serial Data Output

The serial data is output on the SO pin. The data is clocked out on the rising edge of SOCP providing the Empty Flag ( $\overline{EF}$ ) is not asserted. If the Empty Flag is asserted then the next data word is inhibited from moving to the output register and being clocked out by SOCP. NOTE: SOCP should not be clocked once the last bit of the last word has been clocked out. If it is, then two things will occur. One, the SO pin will go High-Z and two, SOCP will be out of sync with Next Read ( $\overline{NR}$ ).

The serial word is shifted out Least Significant Bit first, that is the first bit will be D0, then D1 and so on up to the serial word width. The serial word width must be programmed by connecting the appropriate Data Set line (Q4, Q6, Q7 or Q8) to the  $\overline{NR}$  input. The Data Set lines are taps off a digital delay line. Selecting one of these taps, programs the width of the serial word to be read and shifted out.



2751 drw 04

Figure 1. Reset

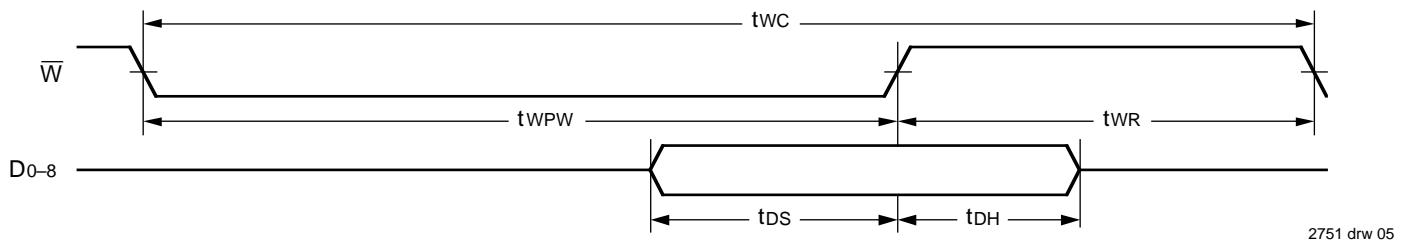


Figure 2. Write Operation

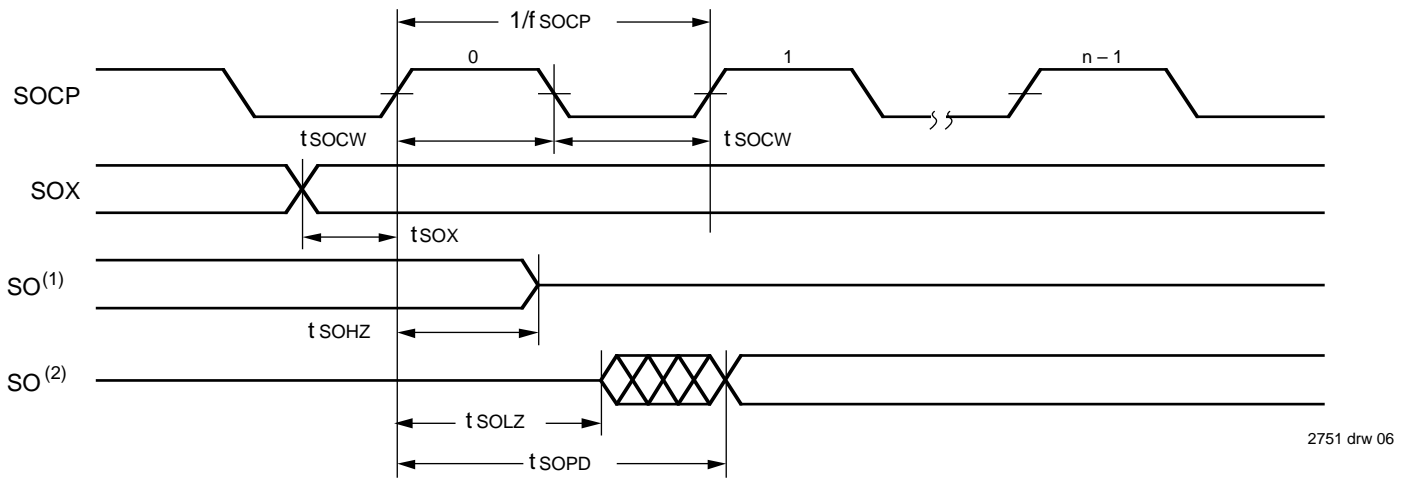


Figure 3. Read Operation

**NOTES:**

1. This timing applies to the Active Device in Width Expansion Mode.
2. This timing applies to Single Device Mode at Empty Boundary ( $\overline{EF} = \text{LOW}$ ) and the Next Active Device in Width Expansion Mode.

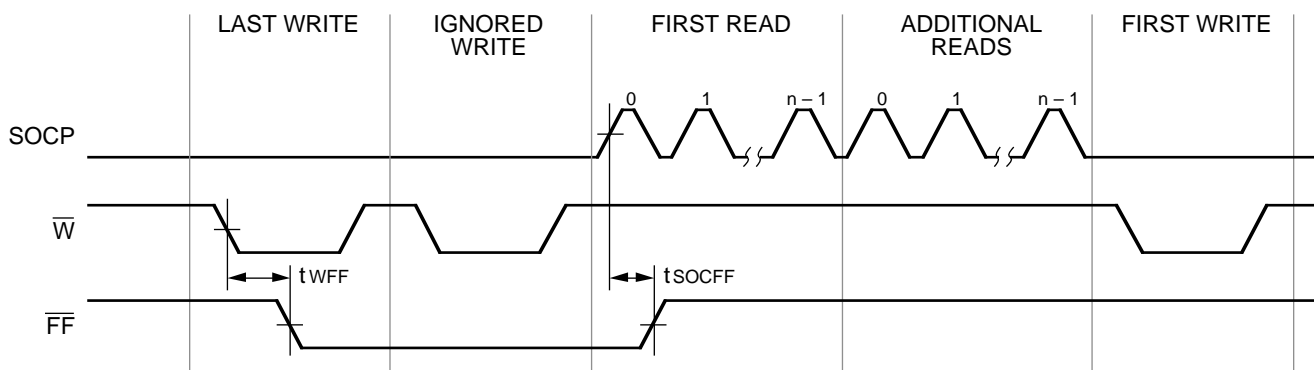
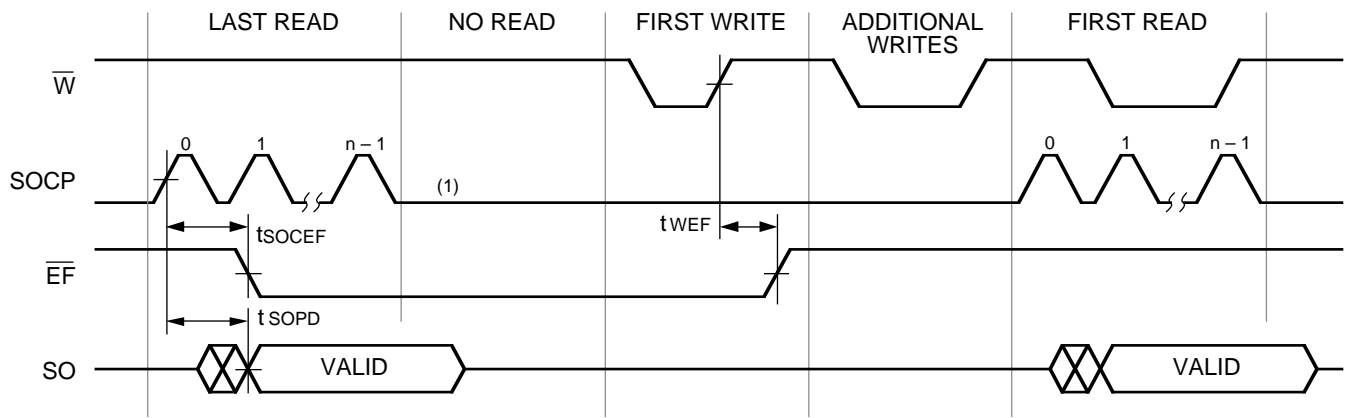


Figure 4. Full Flag from Last Write to First Read

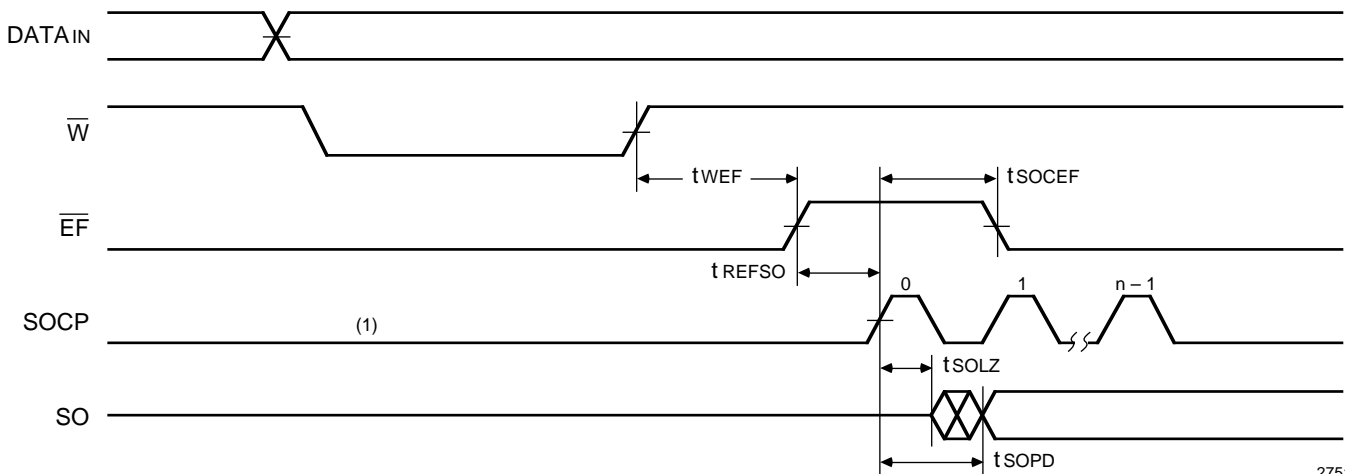


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**NOTE:**

1. Once  $\bar{EF}$  has gone LOW and the last bit of the final word has been shifted out, SOCP should not be clocked until  $\bar{EF}$  goes HIGH.

Figure 5. Empty Flag from Last Read to First Write



2751 drw 09

**NOTE:**

1. SOCP should not be clocked until  $\bar{EF}$  goes HIGH.

Figure 6. Empty Boundary Condition Timing

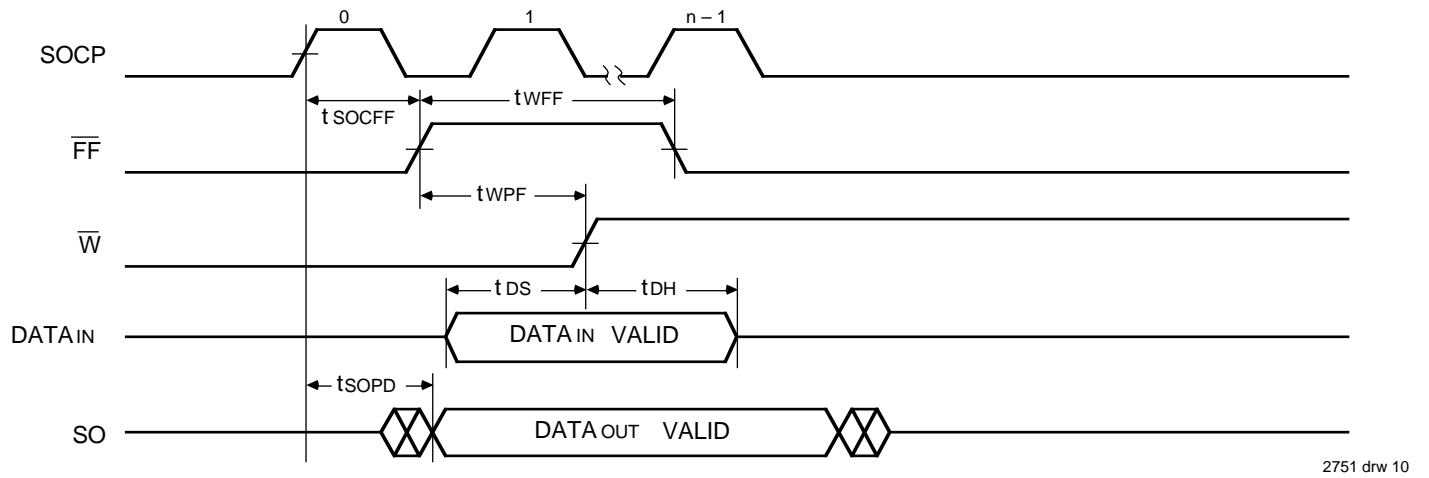


Figure 7. Full Boundary Condition Timing

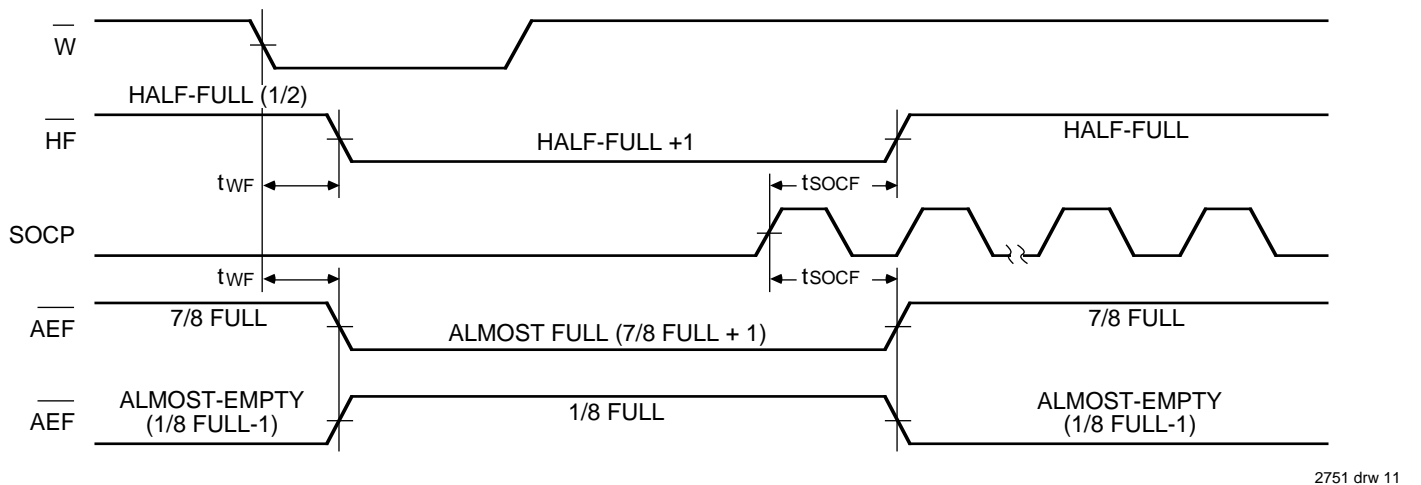
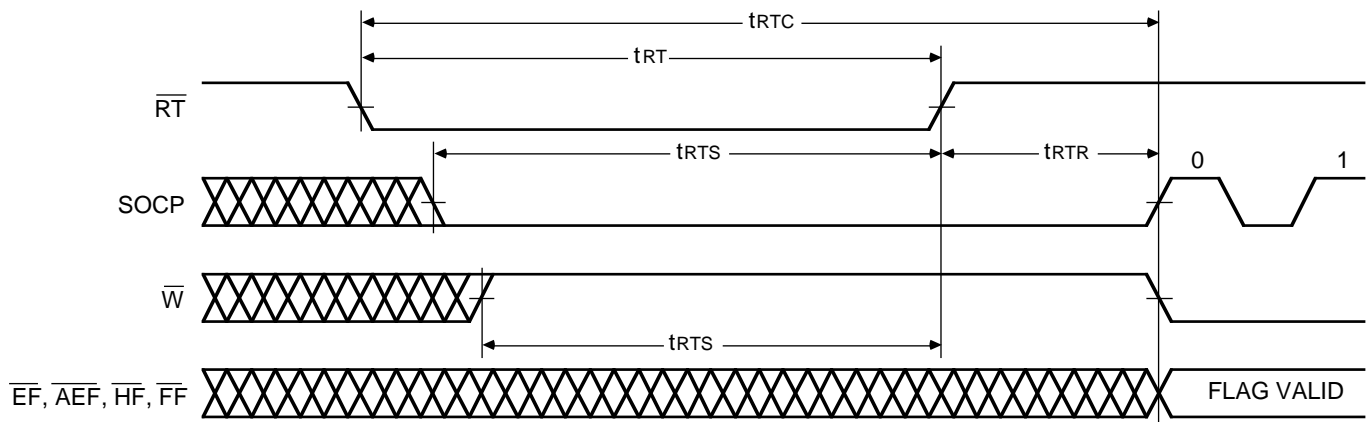


Figure 8. Half Full, Almost Full and Almost Empty Timings

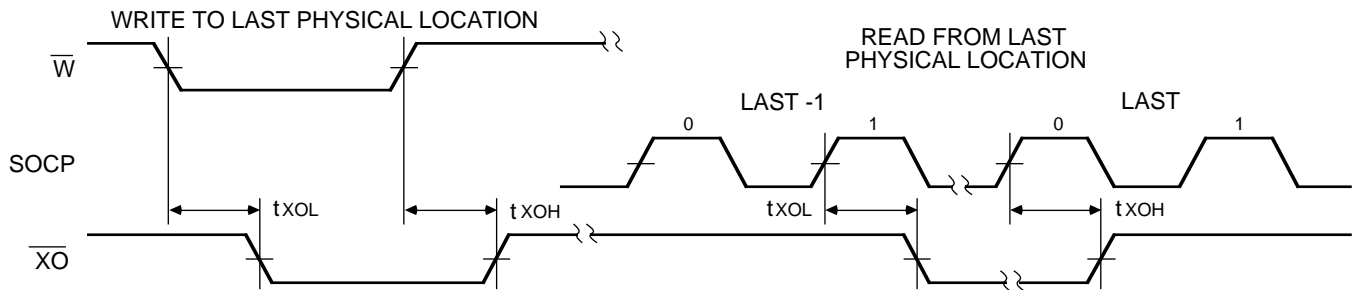




**NOTE:**  
 1.  $\overline{EF}$ ,  $\overline{AEF}$ ,  $\overline{HF}$  and  $\overline{FF}$  may change status during Retransmit, but flags will be valid at  $t_{RTC}$ .

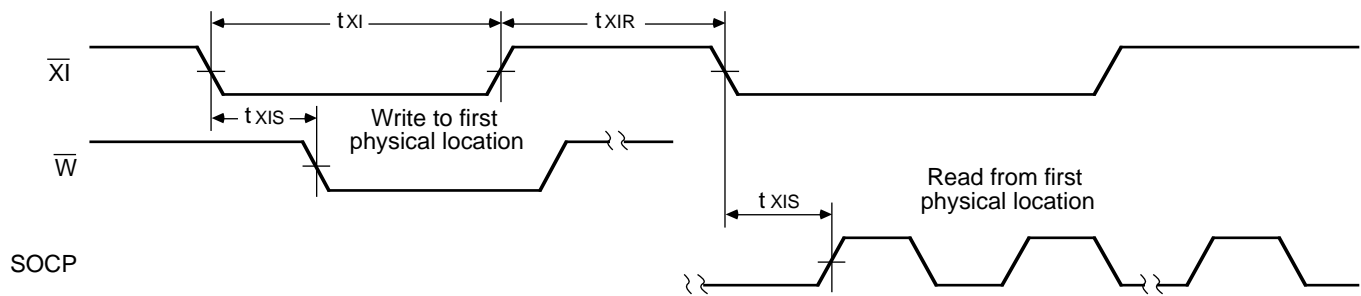
2751 drw 12

Figure 9. Retransmit



2751 drw 13

Figure 10. Expansion-Out



2751 drw 14

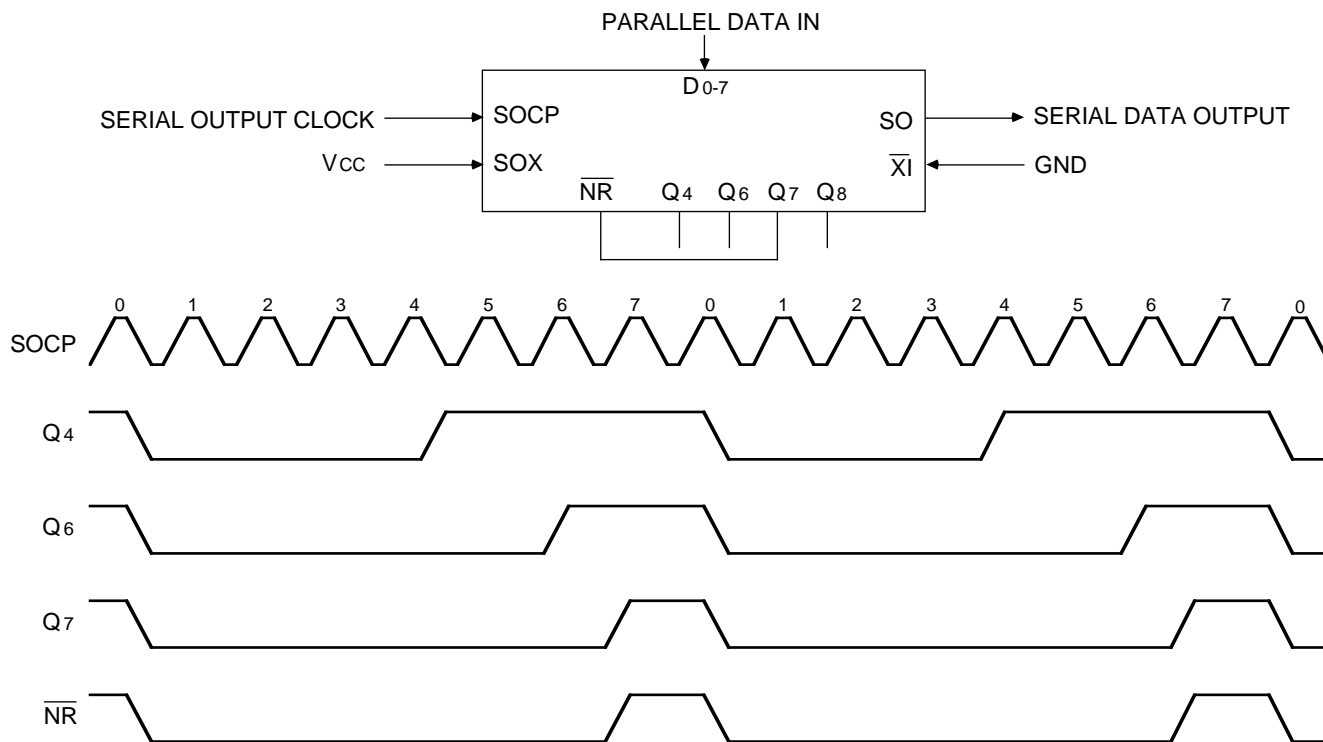
Figure 11. Expansion-In

## OPERATING CONFIGURATIONS

### Single Device Configuration

In the standalone case, the SOX line is tied HIGH and not used. On the first LOW-to-HIGH of the SOCP clock, all of the

Data Set lines (Q4, Q6, Q7, Q8) go LOW and a new serial word is started. The Data Set lines then go HIGH on the equivalent SOCP clock pulse. This continues until the Q line connected to NR goes HIGH completing the serial word. The cycle is then repeated with the next LOW-to-HIGH transition of SOCP.



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Figure 12. Eight-Bit Word Single Device Configuration

## TRUTH TABLES

TABLE 1: RESET AND RETRANSMIT —  
SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL/RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{AEF}$ , $\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment <sup>(1)</sup>	Increment <sup>(1)</sup>	X	X	X

**NOTE:**

1. Pointer will increment if appropriate flag is HIGH.

2751 tbl 09

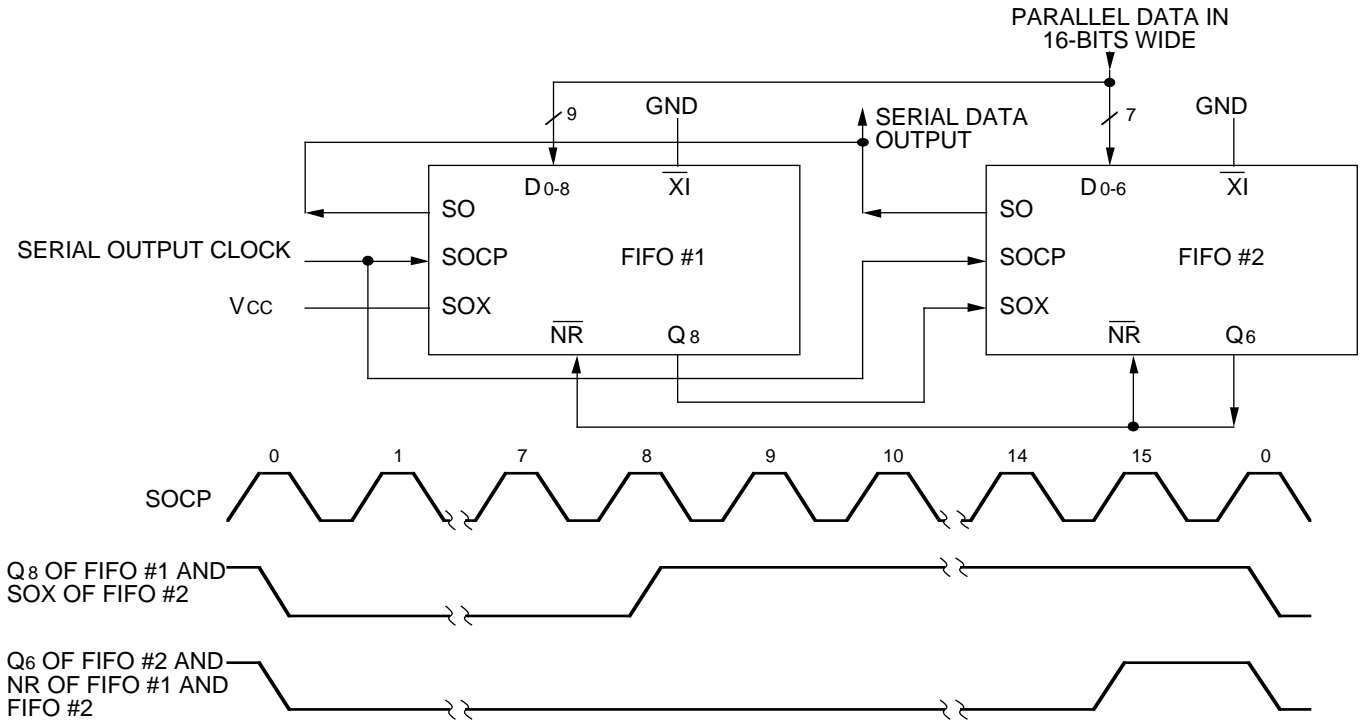
**Width Expansion Configuration**

In the cascaded case, word widths of more than 9 bits can be achieved by using more than one device. By tying the SOX line of the least significant device HIGH and the SOX of the subsequent devices to the appropriate Data Set lines of the previous devices, a cascaded serial word is achieved.

On the first LOW-to-HIGH clock edge of SOCP, all lines go LOW. Just as in the standalone case, on each corresponding clock cycle, the equivalent Data Set line goes HIGH in order of least to most significant. When the Data Set line which is

connected to the SOX input of the next device goes HIGH, the D<sub>0</sub> of that device goes HIGH, the cascading from one device to the next. The Data Set line of the most significant bit programs the serial word width by being connected to all NR inputs.

The Serial Data Output (SO) of each device in the serial word must be tied together. Since the SO pin is three stated, only the device which is currently shifting out is enabled and driving the 1-bit-bus.



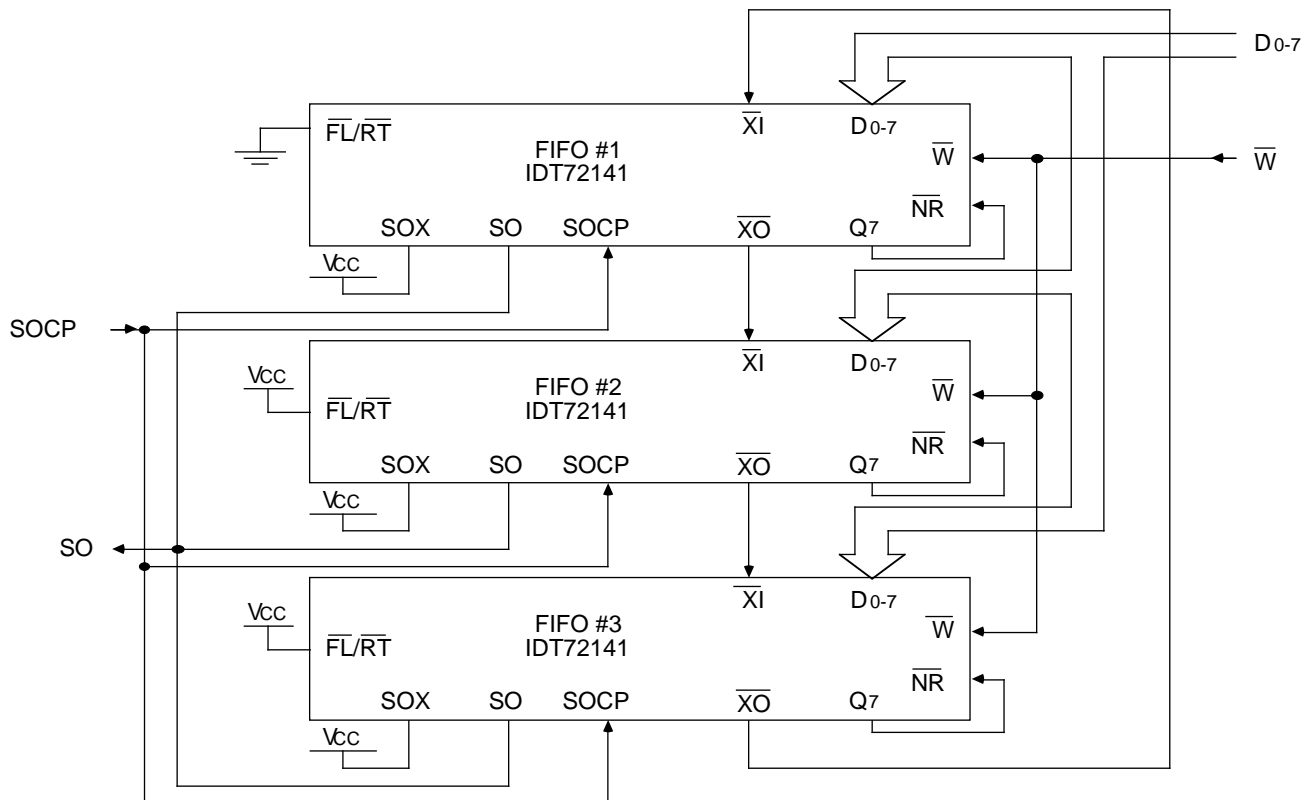
2751 drw 16

Figure 13. Width Wxpansion for 16-bit Parallel Data In. The Parallel Data In is tied to D<sub>0-8</sub> of FIFO #1 and D<sub>0-6</sub> of FIFO #2.

### Depth Expansion (Daisy Chain) Mode

The IDT72131/41 can be easily adapted to applications where the requirements are for greater than 2048/4096 words. Figure 14 demonstrates Depth Expansion using three IDT72131/41. Any depth can be attained by adding additional IDT72131/41 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ( $\overline{FL}$ ) control input.
2. All other devices must have  $\overline{FL}$  in the HIGH state.
3. The Expansion Out ( $\overline{XO}$ ) pin of each device must be tied to the Expansion In ( $\overline{XI}$ ) pin of the next device.
4. External logic is needed to generate a composite Full Flag ( $\overline{FF}$ ) and Empty Flag ( $\overline{EF}$ ). This requires the OR-ing of all  $\overline{EF}$ s and OR-ing of all  $\overline{FF}$ s (i.e., all must be set to generate the correct composite  $\overline{FF}$  or  $\overline{EF}$ ).
5. The Retransmit ( $\overline{RT}$ ) function and Half-Full Flag ( $\overline{HF}$ ) are not available in the Depth Expansion mode.



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Figure 14. A 12K x 8 Parallel-In Serial-Out FIFO

TABLE 2: RESET AND FIRST LOAD TRUTH TABLE —  
DEPTH EXPANSION/COMPOUND EXPANSION MODE

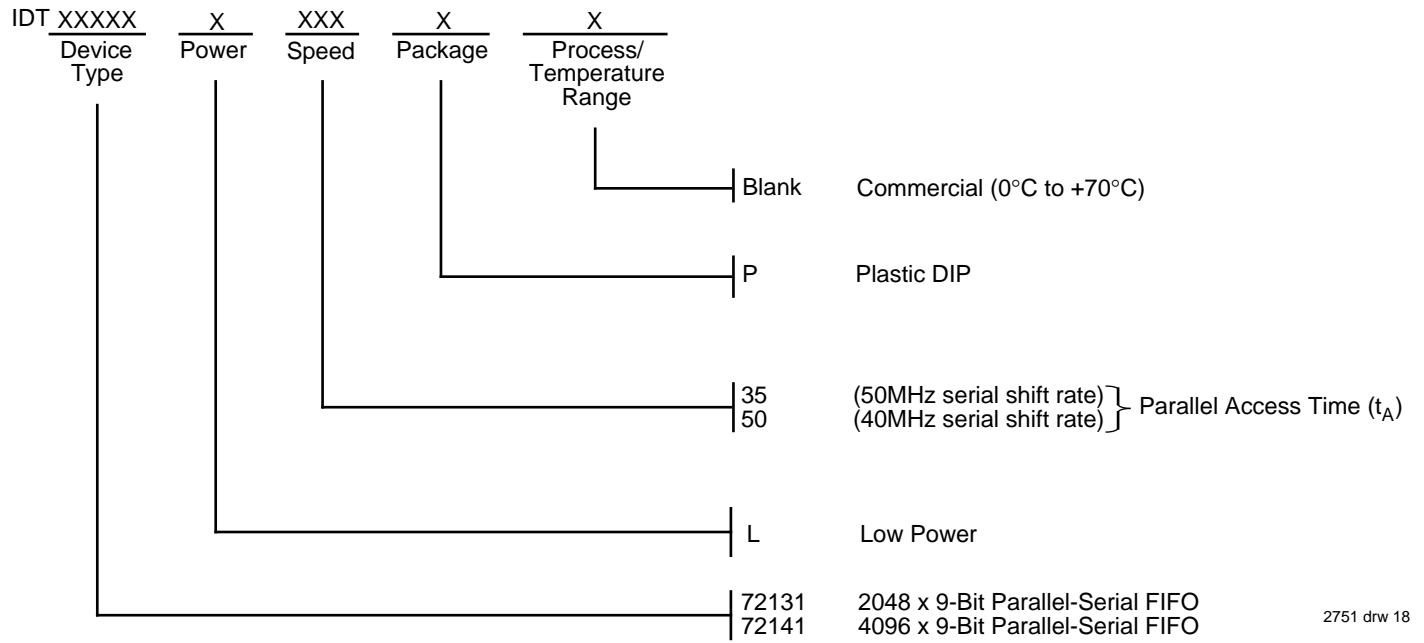
Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset-All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

**NOTES:**

1.  $\overline{XI}$  is connected to  $\overline{XO}$  of previous device.
2.  $\overline{RS}$  = Reset Input,  $\overline{FL/RT}$  = First Load/Retransmit,  $\overline{EF}$  = Empty Flag Output,  $\overline{FF}$  = Full Flag Output,  $\overline{XI}$  = Expansion Input.

2751 tbl 10

**ORDERING INFORMATION**



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