1.8V CMOS 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

IDT74AUCR16245
ADVANCE INFORMATION

FEATURES:

- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **1.8V Optimized**
- **0.8V to 2.7V Operating Range**
- **Inputs/outputs tolerant up to 3.6V**
- **Output drivers: ±4.5mA @ V_{DD} = 2.3V**
- **Low switching noise**
- **Supports hot insertion**
- **Available in TSSOP, TVSOP, and VFBGA packages**

APPLICATIONS:

- **High performance, low voltage communications systems**
- **High performance, low voltage computing systems**

DESCRIPTION:

This 16-bit bus transceiver is built using advanced CMOS technology. The AUCR16245 is designed specifically for asynchronous communications between data buses. The control function implementation minimizes external timing requirements.

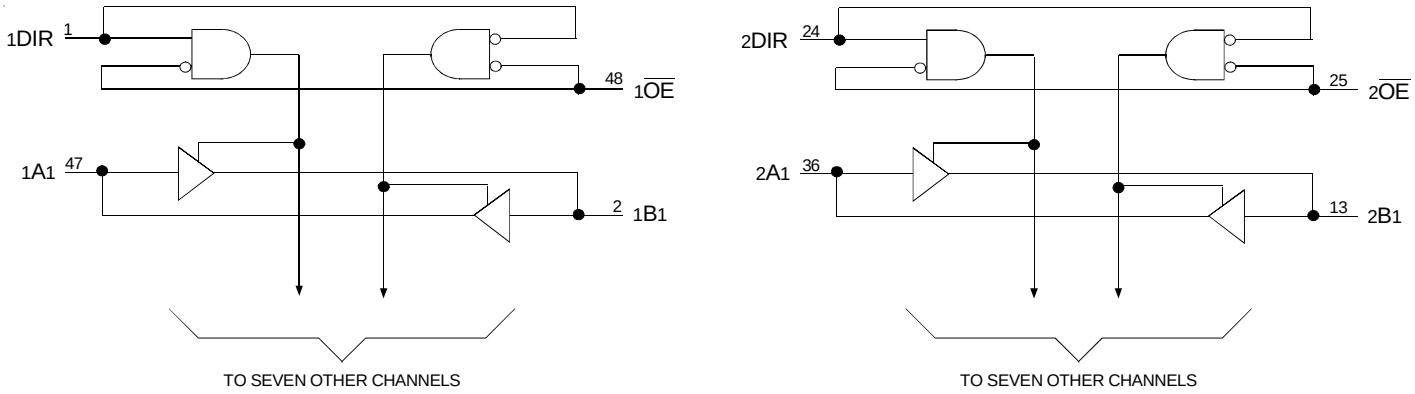
This device can be used as one 16-bit transceiver or two 8-bit transceivers. It allows data transmission from A bus to B bus or from B bus to A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The AUCR16245 has series resistors in the device output structure which will reduce line noise when used with light loads. This driver has been designed with a ±4.5mA output driver at the designated threshold levels.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{DD} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTIONAL BLOCK DIAGRAM



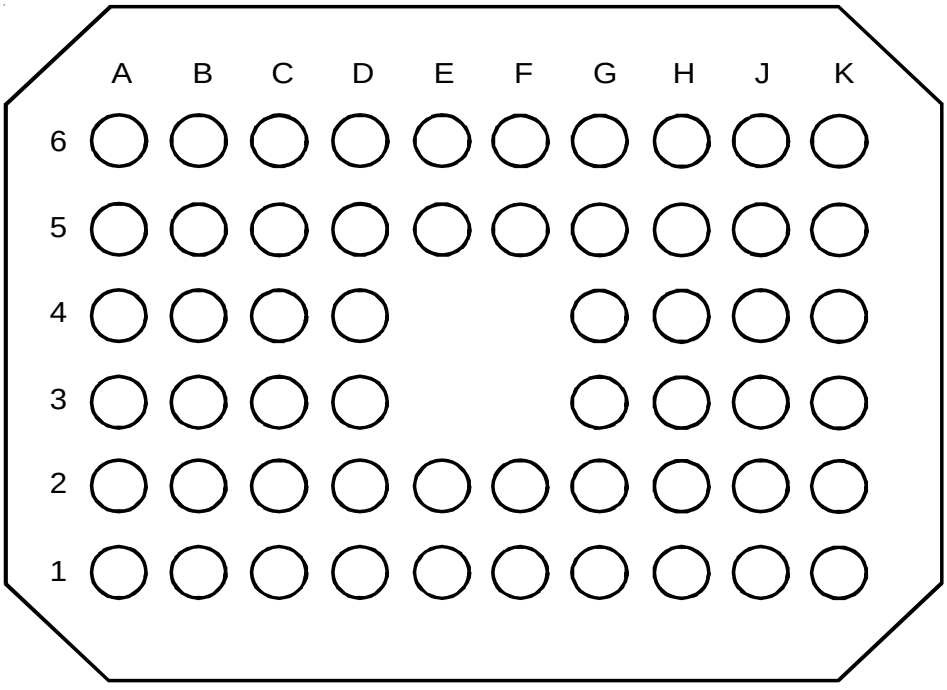
PINOUT CONFIGURATION

	A	B	C	D	E	F	G	H	J	K
6	$1\overline{OE}$	1A2	1A4	1A6	1A8	2A1	2A3	2A5	2A7	$2\overline{OE}$
5	NC	1A1	1A3	1A5	1A7	2A2	2A4	2A6	2A8	NC
4	NC	GND	V_{DD}	GND			GND	V_{DD}	GND	NC
3	NC	GND	V_{DD}	GND			GND	V_{DD}	GND	NC
2	NC	1B1	1B3	1B5	1B7	2B2	2B4	2B6	2B8	NC
1	1DIR	1B2	1B4	1B6	1B8	2B1	2B3	2B5	2B7	2DIR

VFBGA

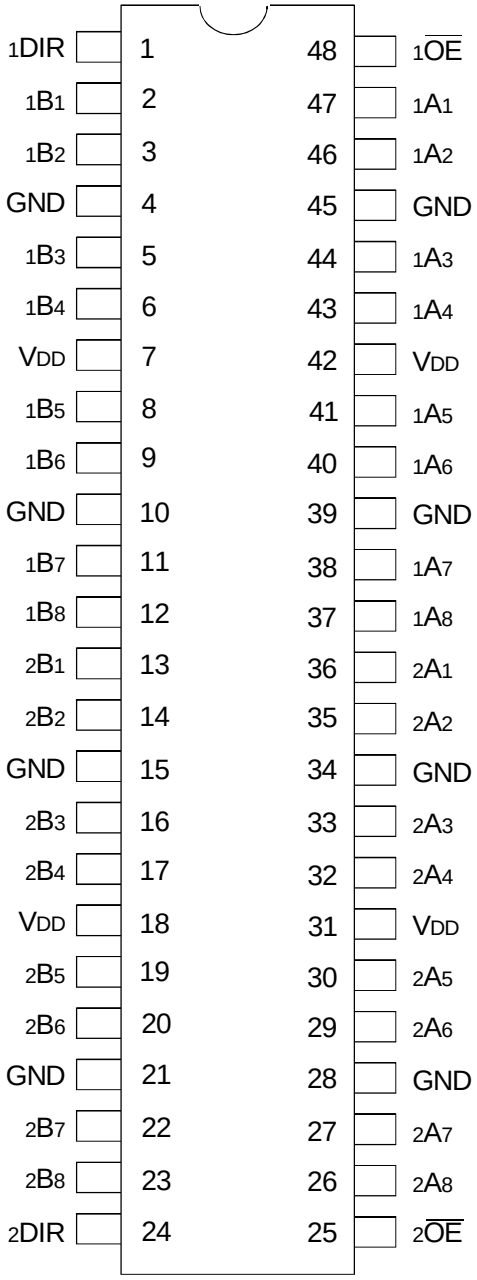
NOTE:
NC = No Internal Connection

56 BALL VFBGA PACKAGE LAYOUT



TOP VIEW

PIN CONFIGURATION



TSSOP/ TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description		Max	Unit
V_{TERM}	Terminal Voltage with Respect to GND (all input and V_{DD} terminals)		–0.5 to +3.6	V
V_{TERM}	Terminal Voltage with Respect to GND (any I/O or Output terminals in high-impedance or power-off state)		–0.5 to +3.6	V
V_{TERM}	Terminal Voltage with Respect to GND (any I/O or Output terminals in high or low state)		–0.5 to +3.6	V
T_{STG}	Storage Temperature		–65 to +150	°C
I_{OUT}	Continuous DC Output Current		±20	mA
I_{IK}	Continuous Clamp Current	$V_I > V_{DD}$	+50	mA
		$V_I < 0$	–50	
I_{OK}	Continuous Clamp Current, $V_O < 0$		–50	mA
I_{DD} I_{SS}	Continuous Current through each V_{DD} or GND		±100	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz, V_{DD} = 2.5V)

Symbol	Parameter	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance(1)	V_{IN} = 0V	3		pF
$C_{I/O}$	I/O Port Capacitance(2)	V_{IN} = 0V	8		pF

NOTES:
1. Applies to the Control Inputs.
2. Applies to ports A and B.

PIN DESCRIPTION

Pin Names	Description
x$\overline{OE}$	3-State Output Enable Inputs (Active Low)
xDIR	Direction Control Inputs
xAx	A Side Inputs or 3-State Outputs
xBx	B Side Inputs or 3-State Outputs

FUNCTION TABLE (EACH 8-BIT SECTION)(1)

Inputs		Outputs
x$\overline{OE}$	xDIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Z

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance

RECOMMENDED OPERATING CHARACTERISTICS(1)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{DD}	Supply Voltage		0.8	2.7	V
V_{IH}	Input HIGH Voltage Level	V_{DD} = 0.8V	V_{DD}	—	V
		V_{DD} = 1.1V to 1.3V	0.65 x V_{DD}	—	
		V_{DD} = 1.4V to 1.6V	0.65 x V_{DD}	—	
		V_{DD} = 1.65V to 1.95V	0.65 x V_{DD}	—	
		V_{DD} = 2.3V to 2.7V	1.7	—	
V_{IL}	Input LOW Voltage Level	V_{DD} = 0.8V	—	0	V
		V_{DD} = 1.1V to 1.3V	—	0.35 x V_{DD}	
		V_{DD} = 1.4V to 1.6V	—	0.35 x V_{DD}	
		V_{DD} = 1.65V to 1.95V	—	0.35 x V_{DD}	
		V_{DD} = 2.3V to 2.7V	—	0.7	
V_I	Input Voltage		0	2.7	V
V_O	Output Voltage	Active State	0	V_{DD}	V
		3-State	0	2.7	
I_{OH}	HIGH Level Output Current	V_{DD} = 0.8V	—	–0.35	mA
		V_{DD} = 1.1V	—	–1.5	
		V_{DD} = 1.4V	—	–2.5	
		V_{DD} = 1.65V	—	–4	
		V_{DD} = 2.3V	—	–4.5	
I_{OL}	LOW Level Output Current	V_{DD} = 0.8V	—	0.35	mA
		V_{DD} = 1.1V	—	1.5	
		V_{DD} = 1.4V	—	2.5	
		V_{DD} = 1.65V	—	4	
		V_{DD} = 2.3V	—	4.5	
$\Delta t/\Delta v$	Input Transition Rise or Fall Time		—	5	ns/V
T_A	Operating Free-Air Temperature		–40	+85	°C

NOTE:
1. All unused inputs of the device must be held at V_{DD} or GND to ensure proper operation.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE(1)

Following Conditions Apply Unless Otherwise Specified:
Operating Conditions: T_A = –40°C to +85°C

Symbol	Parameter		Test Conditions		Min.	Typ.	Max.	Unit
I_{IH}	Input HIGH or LOW Current	Data Inputs	V_{DD} = 2.7V, V_I = V_{DD} or GND		—	—	±10	µA
I_{IL}		Control Inputs			—	—	±5	
I_{OFF}	Input/Output Power Off Leakage		V_{DD} = 0V, V_{IN} or $V_O \leq$ 2.7V		—	—	±10	µA
I_{OZH}(2)	High Impedance Output Current		V_{DD} = 2.7V	V_O = V_{DD}	—	—	±10	µA
I_{OZL}(2)	(3-State Output Pins)			V_O = GND	—	—	±10	
I_{DDL}	Quiescent Power Supply Current		V_{DD} = 0.8V to 2.7V		—	—	20	µA
I_{DDH}			V_{IN} = GND or V_{DD}					
I_{DDZ}								

NOTES:
1. All unused inputs of the device must be held at V_{DD} or GND to ensure proper operation.
2. For the I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = 0.8V - 2.7V	I_{OH} = –100µA	V_{DD} - 0.1	—	—	V
		V_{DD} = 0.8V	I_{OH} = –0.35mA	—	0.55	—	
		V_{DD} = 1.1V[2]	I_{OH} = –1.5mA	0.8	—	—	
		V_{DD} = 1.4V[3]	I_{OH} = –2.5mA	1	—	—	
		V_{DD} = 1.65V[4]	I_{OH} = –4mA	1.2	—	—	
		V_{DD} = 2.3V[5]	I_{OH} = –4.5mA	1.8	—	—	
V_{OL}	Output LOW Voltage	V_{DD} = 0.8V - 2.7V	I_{OH} = 100µA	—	—	0.2	V
		V_{DD} = 0.8V	I_{OL} = 0.35mA	—	0.25	—	
		V_{DD} = 1.1V[2]	I_{OL} = 1.5mA	—	—	0.3	
		V_{DD} = 1.4V[3]	I_{OL} = 25mA	—	—	0.4	
		V_{DD} = 1.65V[4]	I_{OL} = 4mA	—	—	0.45	
		V_{DD} = 2.3V[5]	I_{OH} = 4.5mA	—	—	0.6	

NOTES:
1. V_{IL} and V_{IH} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS table for the appropriate V_{DD} range. T_A = -40°C to +85°C.
2. Demonstrates operation for nominal V_{DD} = 1.2V.
3. Demonstrates operation for nominal V_{DD} = 1.5V.
4. Demonstrates operation for nominal V_{DD} = 1.8V.
5. Demonstrates operation for nominal V_{DD} = 2.5V.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	V_{DD} = 0.8V	V_{DD} = 1.2V	V_{DD} = 1.5V	V_{DD} = 1.8V	V_{DD} = 2.5V	Unit
C_{PD}	Power Dissipation Capacitance Outputs Enabled	C_L = 0pF f = 10MHz	22	23	24	25	29	pF
C_{PD}	Power Dissipation Capacitance Outputs Disabled		1	1	1	1	1	pF

SWITCHING CHARACTERISTICS[1]

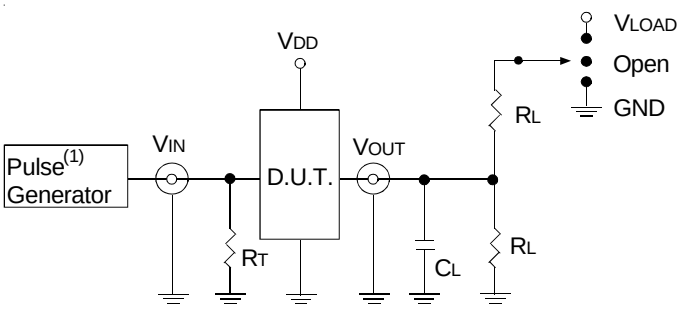
		V_{DD} = 0.8V	V_{DD} = 1.2V±0.1V		V_{DD} = 1.5V±0.1V		V_{DD} = 1.8V±0.15V			V_{DD} = 2.5V±0.2V		
Symbol	Parameter	Typ.	Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay xAx to xBx or xBx to xAx	6.1	0.5	3.6	0.5	2.5	0.5	2	2.5	0.4	2.4	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to xAx or xBx	10.5	0.7	5.1	0.7	3.6	0.7	2.6	3.6	0.7	3.1	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$ to xAx or xBx	13.3	0.8	7.3	0.8	5.5	0.8	3.9	5.3	0.5	3.4	ns

NOTE:
1. See TEST CIRCUITS AND WAVEFORMS. T_A = -40°C to +85°C.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS(1)

Symbol	VDD = 0.8V	VDD = 1.2V±0.1V	VDD = 1.5V±0.1V	VDD = 1.8V±0.15V	VDD = 2.5V±0.2V	Unit
VLOAD	2xVDD	2xVDD	2xVDD	2xVDD	2xVDD	V
VT	VDD/2	VDD/2	VDD/2	VDD/2	VDD/2	V
VLZ	100	100	100	150	150	mV
VHZ	100	100	100	150	150	mV
RL	5	2	2	1	0.5	KΩ
CL	15	15	15	30	30	pF

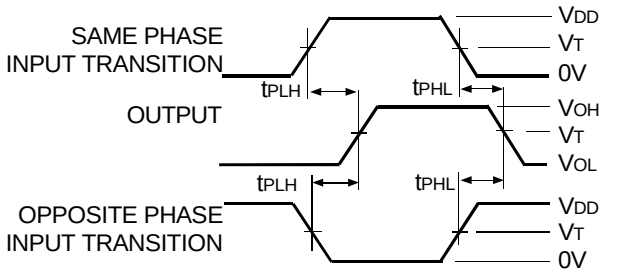


Test Circuits for All Outputs

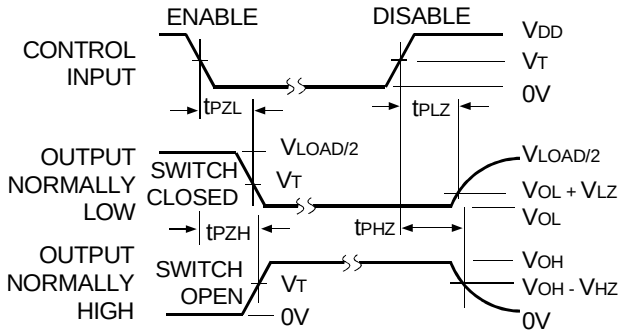
DEFINITIONS:
CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.
NOTE:
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; slew rate ≥ 1V/ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	VLOAD
Disable High Enable High	GND
All Other Tests	Open



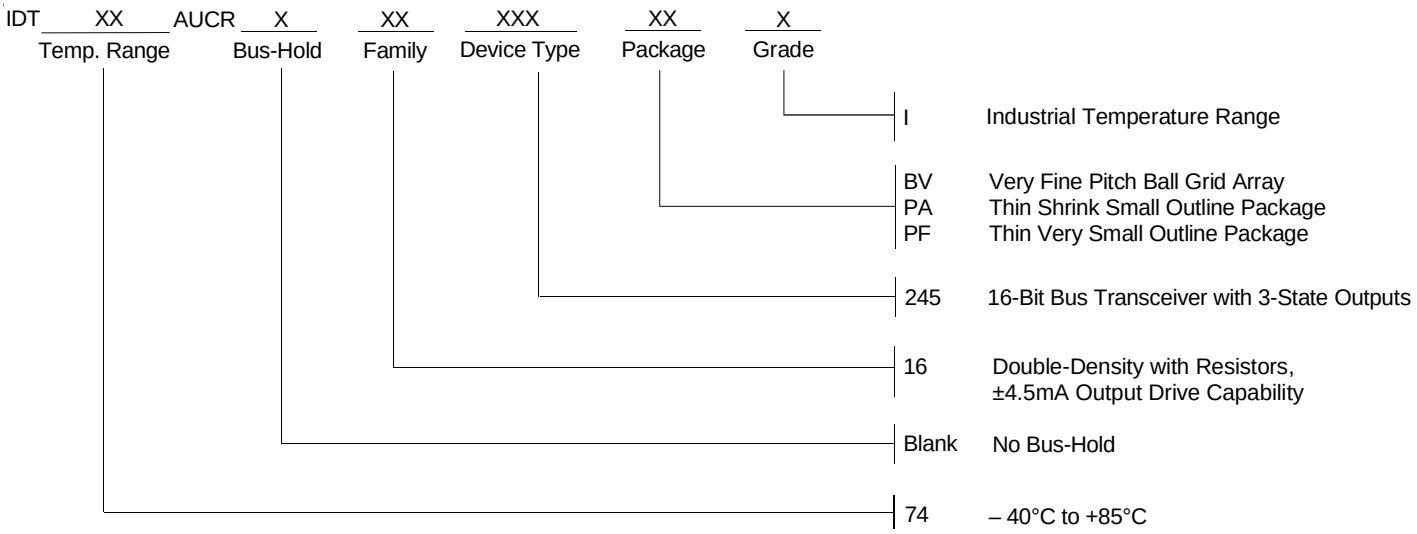
Propagation Delay



NOTE:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

Enable and Disable Times

ORDERING INFORMATION



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