



Integrated Device Technology, Inc.

FAST CMOS 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

IDT74FCT16601AT/CT/ET
IDT74FCT162601AT/CT/ET
PRODUCT PREVIEW

FEATURES:

- **Common features:**
 - 0.5 MICRON CMOS Technology
 - **High-speed, low-power CMOS replacement for ABT functions**
 - **Typical tsk(o) (Output Skew) < 250ps**
 - **Low input and output leakage $\leq 1\mu\text{A}$ (max.)**
 - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
 - Packages include 25 mil pitch SSOP, 19.6 mil pitch TSSOP, 15.7 mil pitch TVSOP and 25 mil pitch Cerpack
 - Extended commercial range of -40°C to +85°C
 - VCC = 5V $\pm 10\%$
- **Features for FCT16601AT/CT/ET:**
 - High drive outputs (-32mA IOH, 64mA IOL)
 - Power off disable outputs permit "live insertion"
 - Typical VOLP (Output Ground Bounce) < 1.0V at VCC = 5V, TA = 25°C
- **Features for FCT162601AT/CT/ET:**
 - Balanced Output Drivers: $\pm 24\text{mA}$
 - Reduced system switching noise
 - Typical VOLP (Output Ground Bounce) < 0.6V at VCC = 5V, TA = 25°C

bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power 18-bit registered bus transceivers combine D-type latches and D-type flip-flops to allow data flow in either direction in a transparent, latched or clocked mode. Each direction has an independent latch enable, an independent clock with a clock enable, and an independent output enable. The package is organized with a flow-through signal pin organization to ease board layout. All inputs are designed with hysteresis for improved noise margin.

This transceiver is ideally suited for high speed memory interfaces which utilize high speed synchronous writes, by clocking the data into a high speed register. Reads can then be performed in a transparent or latched mode utilizing the same transceiver.

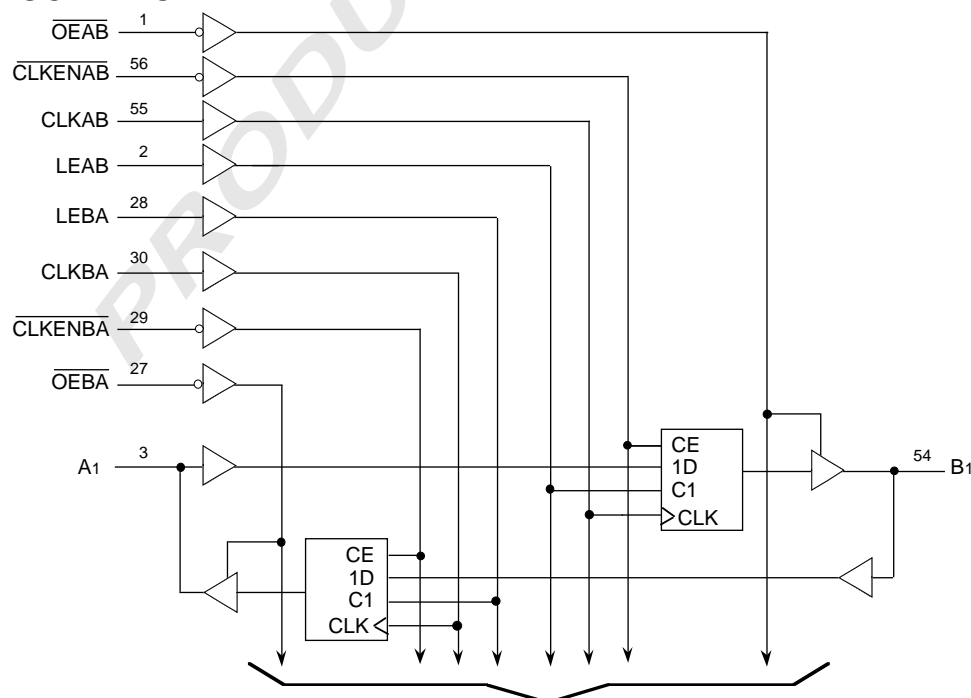
The FCT16601AT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The FCT162601AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors. The FCT162601AT/CT/ET are plug-in replacements for the FCT16601AT/CT/ET and ABT16601 for on-board bus interface applications.

DESCRIPTION:

The FCT16601AT/CT/ET and FCT162601AT/CT/ET 18-

FUNCTIONAL BLOCK DIAGRAM



3247 drw 01

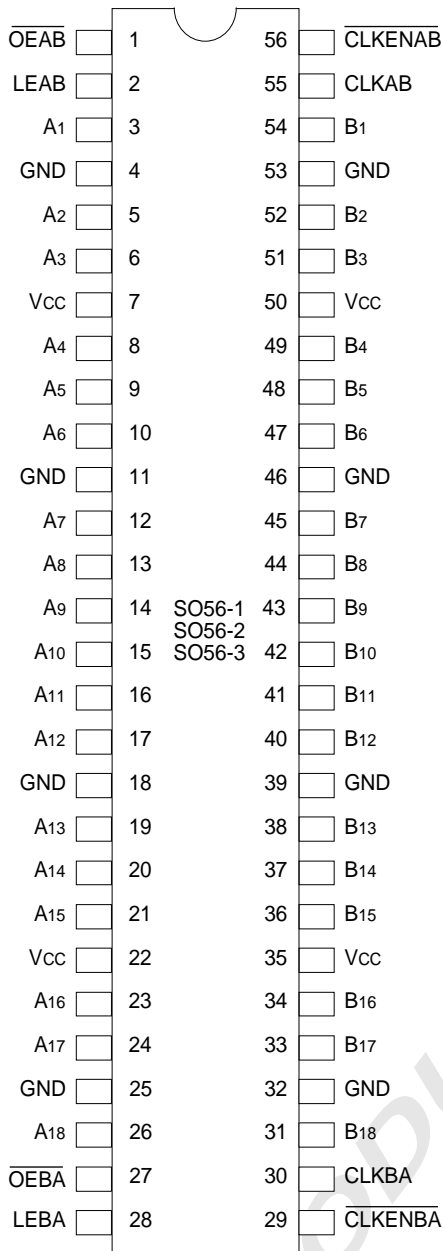
The IDT logo is a registered trademark of Integrated Device Technology, Inc.

TO 17 OTHER CHANNELS

COMMERCIAL TEMPERATURE RANGE

AUGUST 1996

PIN CONFIGURATIONS



SSOP/
TSSOP/TVSOP
TOP VIEW

3247 drw 02

PIN DESCRIPTION

Pin Names	Description
\overline{OEAB}	A-to-B Output Enable Input (Active LOW)
\overline{OEBA}	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs
$\overline{CLKENAB}$	A to B Clock Enable Input
$\overline{CLKENBA}$	B to A Clock Enable Input

3247tbl01

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to VCC +0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +120	mA

NOTES:

3247 Ink 03

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXXT Output and I/O terminals.
- Output and I/O terminals for FCT162XXXT.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	3.5	6.0	pF
C _{I/O}	I/O Capacitance	VOUT = 0V	3.5	8.0	pF

NOTE:

3247 Ink 04

- This parameter is measured at characterization but not tested.

FUNCTION TABLE^(1,4)

Inputs					Outputs
CLKENAB	\overline{OEAB}	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B0 ⁽²⁾
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B0 ⁽²⁾
L	L	L	H	X	B0 ⁽³⁾

NOTES:

3247 tbl 02

- A-to-B data flow is shown. B-to-A data flow is similar but uses \overline{OEBA} , LEBA and CLKBA.
- Output level before the indicated steady-state input conditions were established.
- Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-impedance
↑ = LOW-to-HIGH Transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	± 1	μA
	Input HIGH Current (I/O pins)		$V_I = \text{GND}$	—	—	± 1	
I_{IL}	Input LOW Current (Input pins)	$V_{CC} = \text{Max.}$	$V_I = \text{GND}$	—	—	± 1	μA
	Input LOW Current (I/O pins)		$V_I = \text{GND}$	—	—	± 1	
I_{OZH}	High Impedance Output Current (3-State Output pins)	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}			$V_O = 0.5\text{V}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-80	-140	-225	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}$		—	5	500	μA
I_{CCH}							
I_{CCZ}							

3247 Ink 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16601T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_O	Output Drive Current	$V_{CC} = \text{Max.}, V_O = 2.5\text{V}^{(3)}$		-50	—	-180	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -3\text{mA}$	2.5	3.5	—	V
			$I_{OH} = -15\text{mA}$	2.4	3.5	—	V
			$I_{OH} = -32\text{mA}^{(4)}$	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 64\text{mA}$	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}, V_{IN} \text{ or } V_O \leq 4.5\text{V}$		—	—	± 1	μA

3247 Ink 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162601T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$		60	115	200	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$		-60	-115	-200	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -24\text{mA}$	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 24\text{mA}$	—	0.3	0.55	V

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.

3247 Ink 07

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}, \text{Outputs Open}$ $\overline{OEAB} = V_{CC} \overline{OEBA} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	75	120	$\mu A/$ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}, \text{Outputs Open}$ $f_{CP} = 10\text{MHz (CLKBA)}$ 50% Duty Cycle $\overline{OEAB} = V_{CC}$ $\overline{OEBA} = \text{GND}$ $\overline{LEAB} = \text{GND}$ $\overline{CLKENBA} = \text{GND}$ One Bit Toggling $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.8	1.7	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.3	3.2	
		$V_{CC} = \text{Max.}, \text{Outputs Open}$ $f_{CP} = 10\text{MHz (CLKBA)}$ 50% Duty Cycle $\overline{OEAB} = V_{CC}$ $\overline{OEBA} = \text{GND}$ $\overline{LEAB} = \text{GND}$ $\overline{CLKENBA} = \text{GND}$ Eighteen Bits Toggling $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.8	6.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	8.5	20.8 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V \text{)}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

3247 tbl 09

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT16601AT/ FCT162601AT		FCT16601CT/ FCT162601CT		FCT16601ET/ FCT162601ET		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
f _{MAX}	CLKAB or CLKBA frequency ⁽⁴⁾	CL = 50pF	—	150	—	150	—	150	MHz
t _{PLH} t _{PHL}	Propagation Delay Ax to Bx or Bx to Ax	RL = 500Ω	1.5	4.9	1.5	4.4	1.5	3.8	ns
t _{PLH} t _{PHL}	Propagation Delay LEBA to Ax, LEAB to Bx		1.5	5.2	1.5	4.7	1.5	4.2	ns
t _{PLH} t _{PHL}	Propagation Delay CLKBA to Ax, CLKAB to Bx		1.5	4.7	1.5	4.5	1.5	4.2	ns
t _{PZH} t _{PZL}	Output Enable Time OEBA to Ax, OEAB to Bx		1.5	5.8	1.5	5.3	1.5	4.8	ns
t _{PHZ} t _{PLZ}	Output Disable Time OEBA to Ax, OEAB to Bx		1.5	6.2	1.5	5.7	1.5	5.2	ns
tsu	Set-up Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA		4.0	—	3.0	—	2.4	—	ns
th	Hold Time HIGH or LOW Ax after CLKAB, Bx after CLKBA		0	—	0	—	0	—	ns
tsu	Set-up Time HIGH or LOW Ax to LEAB, Bx to LEBA	Clock LOW	1.0	—	1.0	—	1.0	—	ns
		Clock HIGH	2.5	—	2.0	—	1.5	—	ns
th	Hold Time, HIGH or LOW Ax after LEAB, Bx after LEBA		2.0	—	1.5	—	0.5	—	ns
tsu	Set-up Time, $\overline{\text{CLKEN}}$ to CLK		2.5	—	2.5	—	2.0	—	ns
th	Hold Time, $\overline{\text{CKLEN}}$ after CLK		0	—	0	—	0	—	ns
tw	LEAB or LEBA Pulse Width HIGH ⁽⁴⁾		2.5	—	2.5	—	2.5	—	ns
tw	CLKAB or CLKBA Pulse Width HIGH or LOW ⁽⁴⁾		3.0	—	3.0	—	3.0	—	ns
tsk(o)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	ns

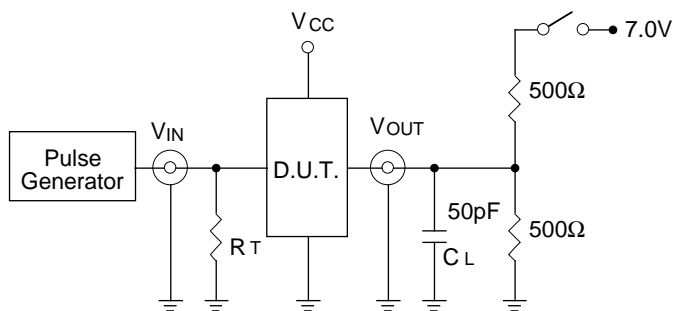
NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.

3247 tbl 09

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



3247 drw 04

SWITCH POSITION

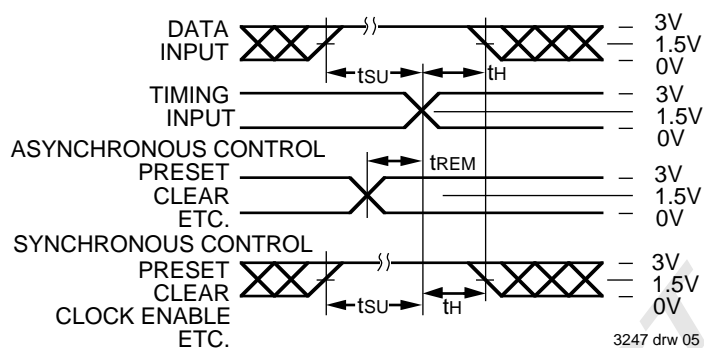
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
 RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

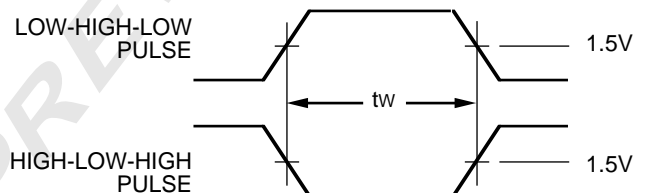
3247 Ink 10

SET-UP, HOLD AND RELEASE TIMES



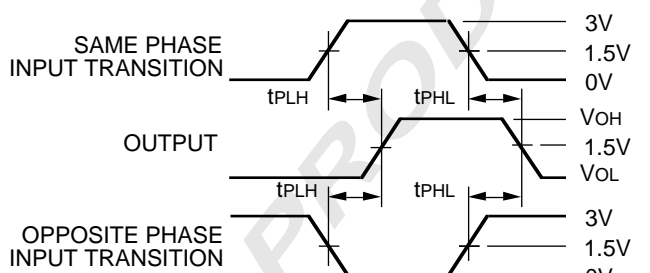
3247 drw 05

PULSE WIDTH



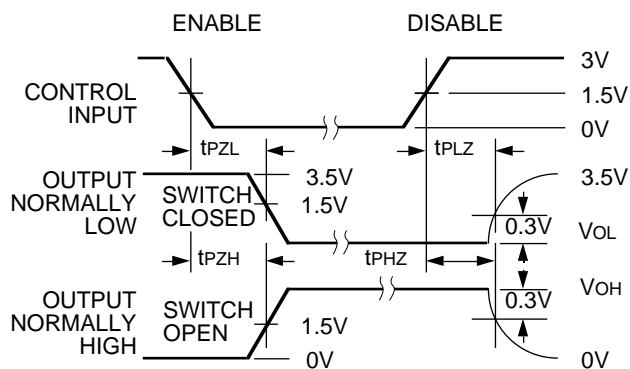
3247 drw 06

PROPAGATION DELAY



3247 drw 07

ENABLE AND DISABLE TIMES

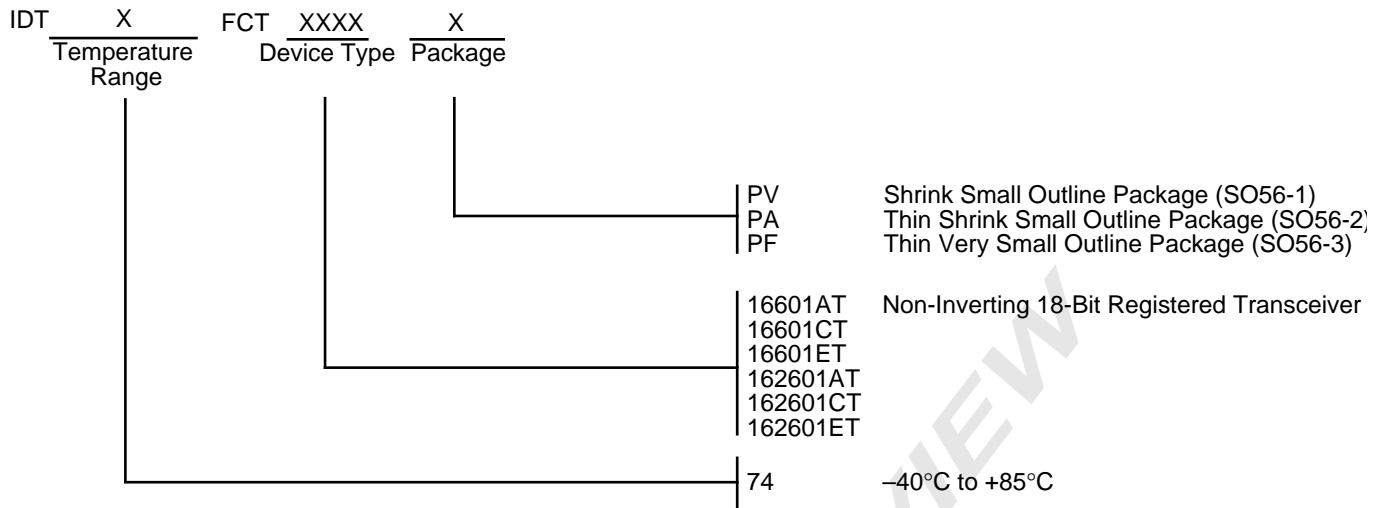


3247 drw 08

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$

ORDERING INFORMATION



PRODUCT PREVIEW