



3.3V PHASE-LOCK LOOP CLOCK DRIVER

IDTCSPF2510C

FEATURES:

- Phase-Lock Loop Clock Distribution for Synchronous DRAM Applications
- Distributes one clock input to one bank of ten outputs
- Output enable bank control
- External feedback (FBIN) pin is used to synchronize the output to the clock input signal
- On-chip series damping resistors with each driver
- No external RC network required for PLL loop stability
- Operates at 3.3V VDD
- tpd Phase Error at 133MHz: $< \pm 150\text{ps}$
- Jitter (cycle-cycle)(peak-to-peak) at 66MHz to 133MHz: $| 70 | \text{ps}$
- Spread Spectrum Compatible
- Operating frequency 25MHz to 140MHz
- Fully conforms to PC133 specifications
- Available in 24-Pin TSSOP package

DESCRIPTION:

The IDTCSPF2510C is a high performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both

frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The CSPF2510C operates at 3.3V and provides integrated series-damping resistors that make it ideal for driving point-to-point loads, single or dual.

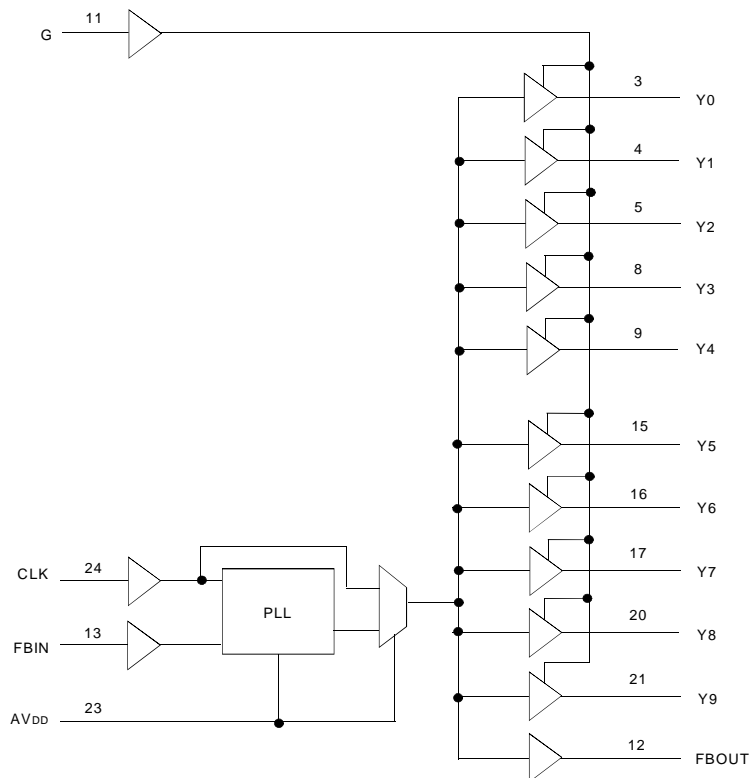
One bank of ten outputs provide low-skew, low-jitter copies of CLK. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at CLK. The outputs can be enabled or disabled via the control G input. When the G input is high, the outputs switch in phase and frequency with CLK; when the G input is low, the outputs are disabled to the logic-low state.

Unlike many products containing PLLs, the CSPF2510C does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CSPF2510C requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLK, as well as following any changes to the PLL reference or feedback signals. The PLL can be bypassed for the test purposes by strapping AVDD to ground.

The CSPF2510C is characterized for operation from 0°C to +85°C. This device is also available (on special order) in Industrial (-40°C to +85°C) temperatures. See Ordering Information for more details.

FUNCTIONAL BLOCK DIAGRAM

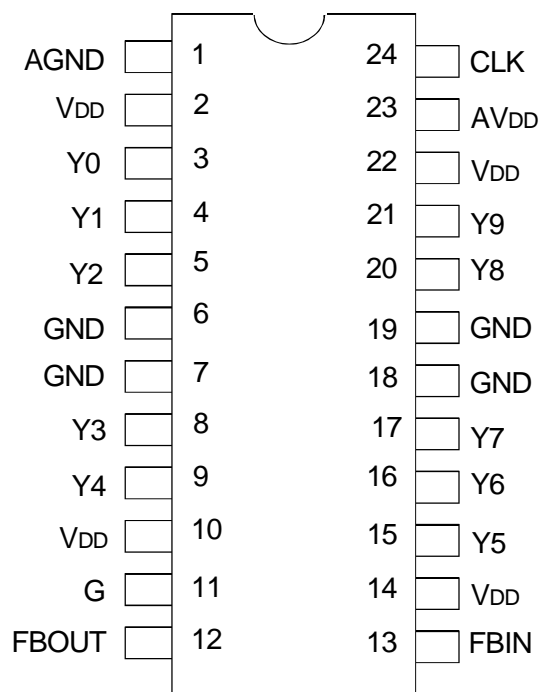


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0°C TO 85°C TEMPERATURE RANGE

AUGUST 2002

PIN CONFIGURATION



TSSOP
TOP VIEW

APPLICATIONS:

- SDRAM Modules
- PC Motherboards
- Workstations

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Rating | Max | Unit |
|--|--|-------------------------------|------|
| V _{DD} | Supply Voltage Range | -0.5 to +4.6 | V |
| V _I ⁽¹⁾ | Input Voltage Range | -0.5 to +6.5 | V |
| V _O ^(1,2) | Voltage range applied to any output in the high or low state | -0.5 to V _{DD} + 0.5 | V |
| I _{IK} (V _I < 0) | Input clamp current | -50 | mA |
| I _{OK} (V _O < 0 or V _O > V _{DD}) | Terminal Voltage with Respect to GND (inputs V _{IH} 2.5, V _{IL} 2.5) | ±50 | mA |
| I _O (V _O = 0 to V _{DD}) | Continuous Output Current | ±50 | mA |
| V _{DD} or GND | Continuous Current | ±100 | mA |
| T _{STG} | Storage Temperature Range | -65 to +150 | °C |
| T _J | Junction Temperature | +150 | °C |

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

CAPACITANCE

| Parameter | Description | Min. | Typ. | Max. | Unit |
|-----------------|---|------|------|------|------|
| C _{IN} | Input Capacitance V _I = V _{DD} or GND | — | 5 | — | pF |
| C _O | Output Capacitance V _C = V _{DD} or GND | — | 6 | — | pF |
| C _L | Load Capacitance | — | 25 | — | pF |

NOTE:

1. Unused inputs must be held high or low to prevent them from floating.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Description | Min. | Max. | Unit |
|------------------------------------|--------------------------------|------|------|------|
| V _{DD} , AV _{DD} | Power Supply Voltage | 3 | 3.6 | V |
| T _A | Operating Free-Air Temperature | 0 | +85 | °C |

PIN DESCRIPTION

| Terminal | | Type | Description |
|----------|-----------------------------------|--------|--|
| Name | No. | | |
| CLK | 24 | I | Clock input. CLK provides the clock signal to be distributed by the CSPF2510C clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal. |
| FBIN | 13 | I | Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN. |
| G | 11 | I | Output bank enable. G is the output enable for outputs Y(0:9). When G is low, outputs Y(0:9) are disabled to a logic-low state. When G is high, all outputs Y(0:9) are enabled and switch at the same frequency as CLK. |
| FBOUT | 12 | O | Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL. FBOUT has an integrated 25Ω series-damping resistor. |
| Y (0:9) | 3, 4, 5, 8, 9, 15, 16, 17, 20, 21 | O | Clock outputs. These outputs provide low-skew copies of CLK. Output bank Y(0:9) is enabled via the G input. These outputs can be disabled to a logic-low state by de-asserting the G control input. Each output has an integrated 25Ω series-damping resistor. |
| AVDD | 23 | Power | Analog power supply. AVDD provides the power reference for the analog circuitry. In addition, AVDD can be used to bypass the PLL for test purposes. When AVDD is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs. |
| AGND | 1 | Ground | Analog ground. AGND provides the ground reference for the analog circuitry. |
| VDD | 2, 10, 14, 22 | Power | Power supply |
| GND | 6, 7, 18, 19 | Ground | Ground |

STATIC FUNCTION TABLE (AVDD = 0V)

| Inputs | | Outputs | |
|--------|---------|---------|---------|
| G | CLK | Y (0:9) | FBOUT |
| L | L | L | L |
| L | H | L | H |
| H | H | H | H |
| H | L | L | L |
| H | running | running | running |

DYNAMIC FUNCTION TABLE (AVDD = 3.3V)

| Inputs | | Outputs | |
|--------|---------|---------------------------|---------------------------|
| G | CLK | Y (0:9) | FBOUT |
| X | L | L | L |
| L | running | L | running in phase with CLK |
| L | H | L | H |
| H | running | running in phase with CLK | running in phase with CLK |
| H | H | H | H |

DC ELECTRICAL CHARACTERISTICS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

| Symbol | Test Conditions | V _{DD} | Min. | Typ. | Max. | Unit |
|---------------------------------|---|-------------------------|-----------------------|------|------|------|
| V _{IH} | Input HIGH Level | — | 2 | — | — | V |
| V _{IL} | Input LOW Level | — | — | — | 0.8 | V |
| V _{IK} | I _I = -18mA | 3V | — | — | -1.2 | V |
| V _{OH} | I _{OH} = -100μA | Min. to Max. | V _{DD} - 0.2 | — | — | V |
| | I _{OH} = -12mA | 3V | 2.1 | — | — | |
| | I _{OH} = -6mA | 3V | 2.4 | — | — | |
| V _{OL} | I _{OL} = 100μA | Min. to Max. | — | — | 0.2 | V |
| | I _{OL} = 12mA | 3V | — | — | 0.8 | |
| | I _{OL} = 6mA | 3V | — | — | 0.55 | |
| I _I | V _I = V _{DD} or GND | 3.6V | — | — | ±5 | μA |
| I _{DD} | V _I = V _{DD} or GND, AV _{DD} = GND, I _o = 0, Outputs: LOW or HIGH | 3.6V | — | — | 10 | μA |
| ΔI _{DD} | One input at V _{DD} - 0.6V, other inputs at V _{DD} or GND | 3.3V to 3.6V | — | — | 500 | μA |
| CPD | Power Dissipation Capacitance | 3.6V | — | 10 | 14 | pF |
| I _{DDA} ⁽²⁾ | AV _{DD} Power Supply Current | AV _{DD} = 3.3V | — | 10 | — | mA |

NOTES:

- For conditions shown as Min. or Max., use the appropriate value specified under recommended operating conditions.
- For I_{DD} of AV_{DD}, see TYPICAL CHARACTERISTICS.

TIMING REQUIREMENTS OVER OPERATING RANGE OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE

| | | Min. | Max. | Unit |
|------------------|-----------------------------------|------|------|------|
| f _{CLK} | Clock frequency | 25 | 140 | MHz |
| | Input clock duty cycle | 40% | 60% | |
| | Stabilization time ⁽¹⁾ | — | 1 | ms |

NOTE:

- Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable.

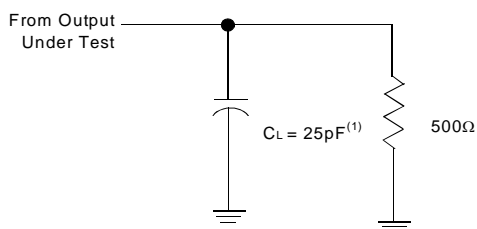
SWITCHING CHARACTERISTICS OVER OPERATING RANGE OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, C_L = 25pF

| Parameter ⁽¹⁾ | From (Input) | To (Output) | V _{DD} = 3.3V ± 0.165V | | | V _{DD} = 3.3V ± 0.3V | | | Unit |
|--|------------------------|---------------|---------------------------------|------|------|-------------------------------|------|------|------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| t _{PHASE error} ⁽²⁾ | 100MHz < CLK↑ < 133MHz | FBIN↑ | — | — | — | -150 | — | 150 | ps |
| t _{PHASE error-jitter} ^(2,4) | CLK↑ = 133MHz | FBIN↑ | -50 | — | 50 | — | — | — | ps |
| t _{SK(o)} ⁽³⁾ | Any Y (133MHz) | Any Y | — | — | — | — | — | 150 | ps |
| Jitter (cycle-cycle) (peak-to-peak) | CLK = 66MHz to 133MHz | Any Y or FBOU | — | — | — | — | 70 | — | ps |
| | CLK = 100MHz to 133MHz | Any Y or FBOU | — | — | — | — | 65 | — | ps |
| Duty cycle reference ⁽⁵⁾ | CLK = 133MHz | Any Y or FBOU | — | — | — | 45 | — | 55 | % |
| t _R | | Any Y or FBOU | — | 1.3 | 1.9 | 0.8 | — | 2.1 | ns |
| t _F | | Any Y or FBOU | — | 1.7 | 2.5 | 0.8 | — | 2.5 | ns |

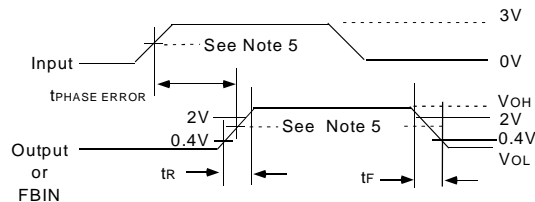
NOTES:

- The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.
- See PARAMETER MEASUREMENT INFORMATION.
- The t_{SK(o)} specification is only valid for equal loading of all outputs.
- Phase error does not include jitter.
- See TYPICAL CHARACTERISTICS.

PARAMETER MEASUREMENT INFORMATION⁽²⁾

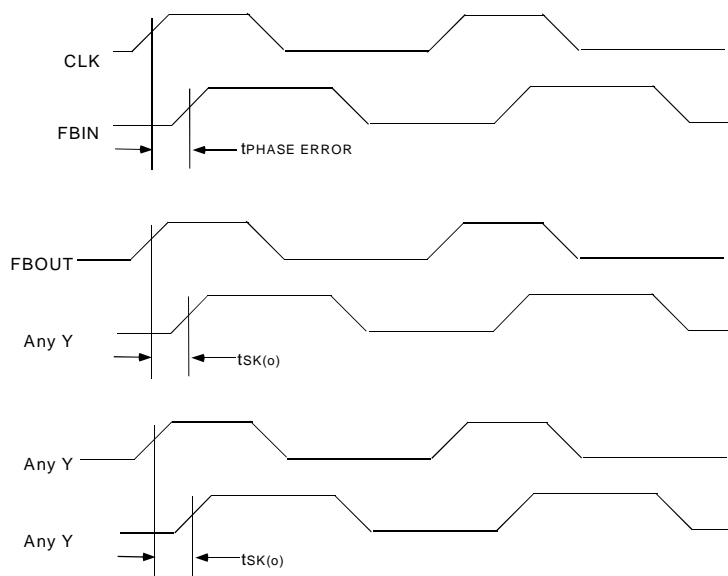
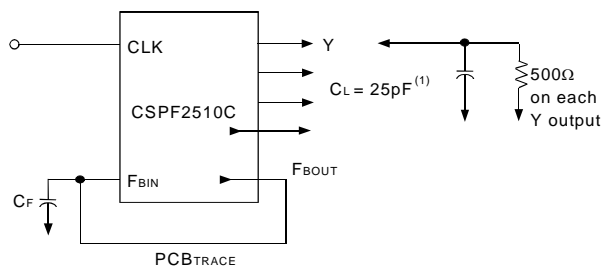


Load Circuit Waveforms



*Load Voltage Waveforms
Propagation Delay Times*

PHASE ERROR AND SKEW CALCULATIONS^(3,4,5)

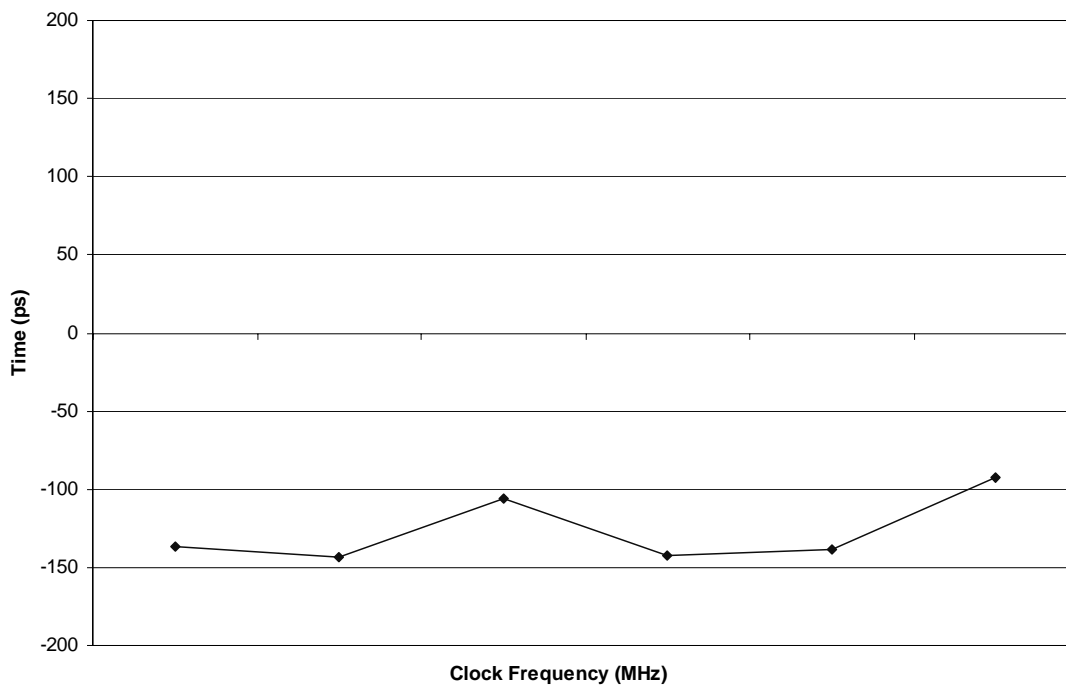


NOTES:

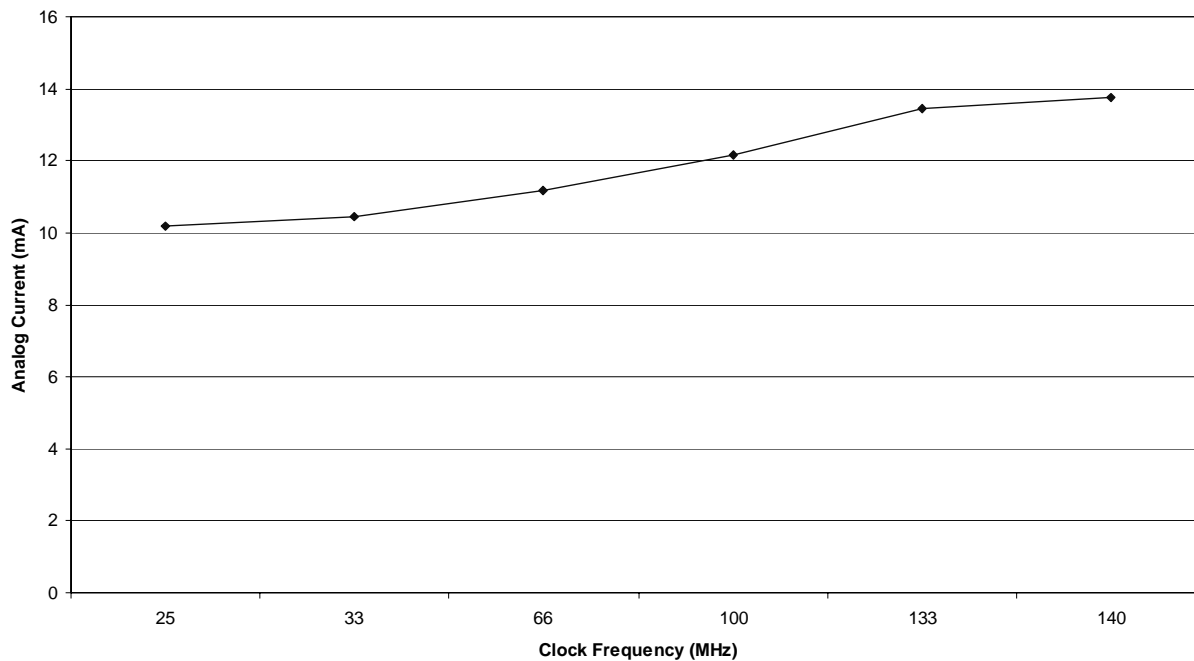
1. CL includes probe and jig capacitance.
2. All inputs pulses are supplied by generators having the following characteristics: PRR ≤ 100MHz, Zo = 50Ω, tr ≤ 1.2 ns, tf ≤ 1.2 ns.
3. The outputs are measured one at a time with one transition per measurement.
4. Phase error measurements require equal loading at outputs Y and FBOUT. CF = CL - CFBIN - CPCBTRACE; CFBIN ≅ 6pF.
5. V threshold set at 1.5V across Voltage/Temp operating range.

TYPICAL CHARACTERISTICS

Phase Error vs Clock Frequency
AV_{DD} and V_{DD} = 3.3V
T_a = 25C

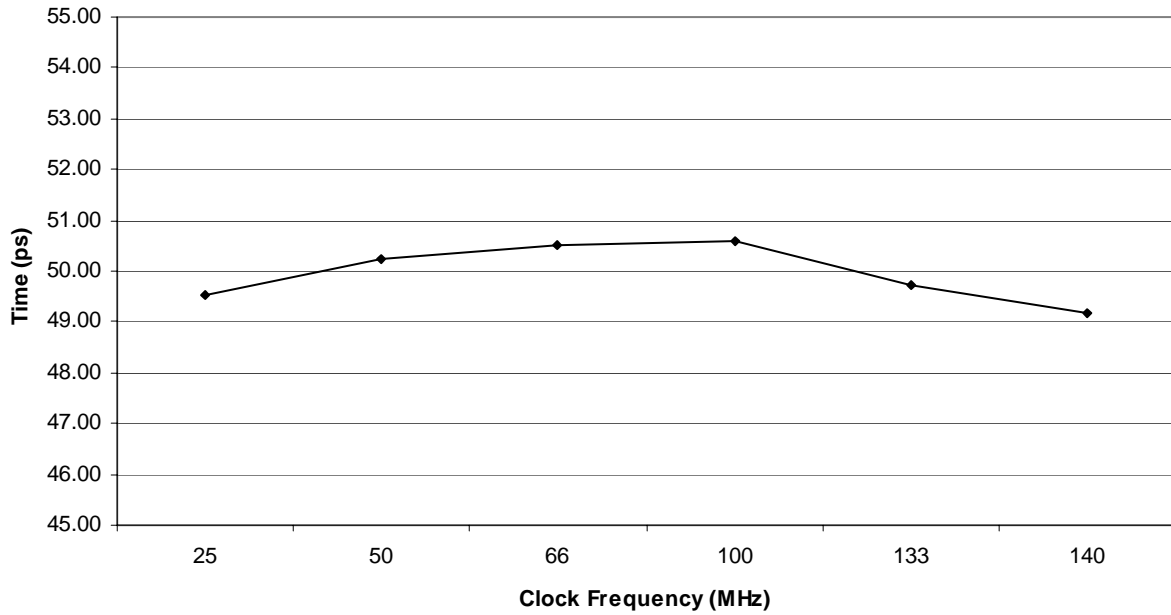


Analog Supply Current vs. Clock Frequency
AV_{DD} and V_{DD} = 3.3V
T_a = 25C

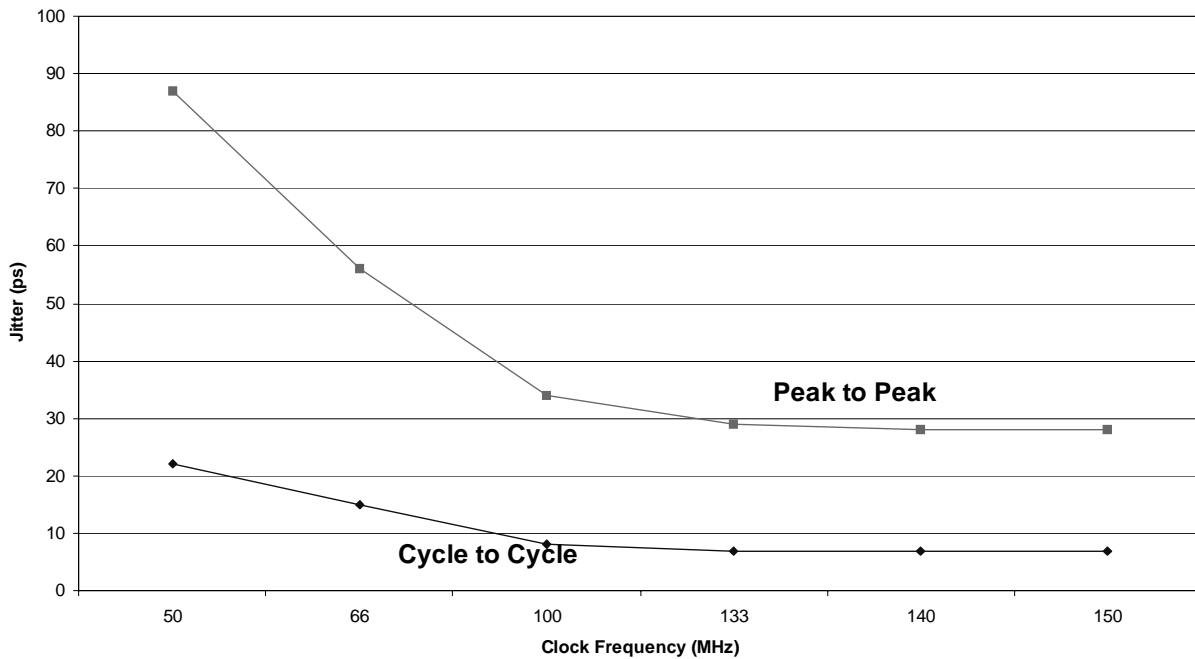


TYPICAL CHARACTERISTICS (continued)

Output Duty Cycle vs Clock Frequency
AVDD and VDD = 3.3V
Ta = 25C

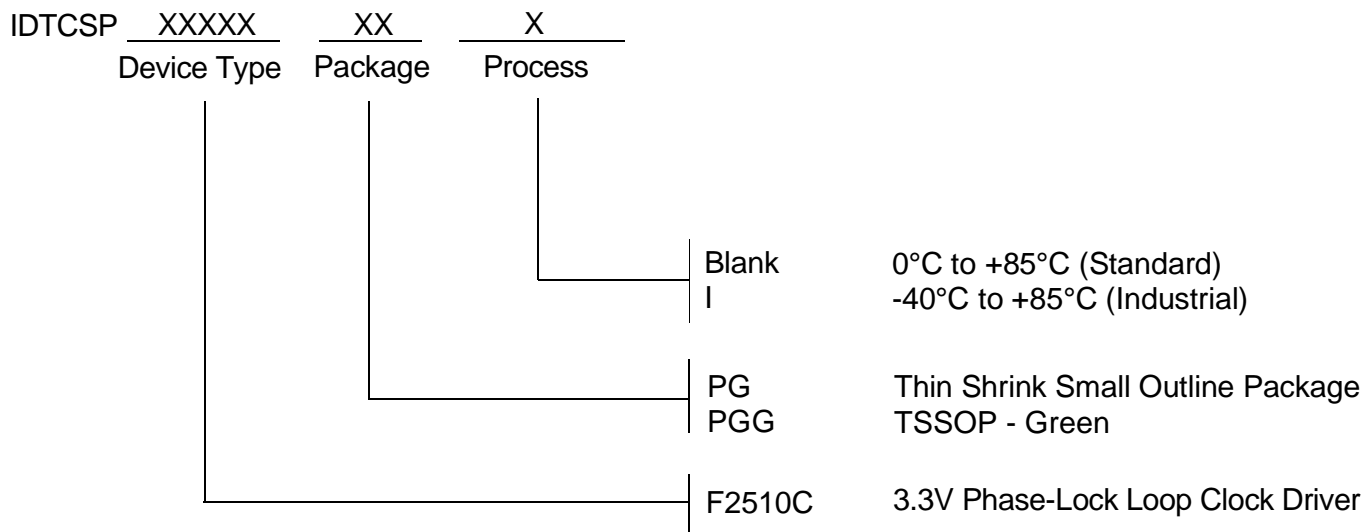


Jitter vs. Clock Frequency
Avcc and Vcc = 3.3V
Ta = 25C



NOTE:
Refer to note 5 (page 5) for test conditions.

ORDERING INFORMATION



DATA SHEET DOCUMENT HISTORY

| | |
|-----------|---|
| 4/15/2002 | Added Commercial temp. |
| 7/31/2002 | Removed Commercial Temp and put in 0C to 85C instead. |



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