ILC6382

1-Cell to 3-Cell Boost with True Load Disconnect,
3.3V, 5V or Adjustable Output

POWER
POWERED BY IMPALA
ON THE GO

General Description

The ILC6382 series of step-up DC-DC converters operate from 1-cell to 3-cell input. In shutdown mode, the device allows true load disconnect from battery input. Designed for wireless communications applications, the oscillator frequency is set at 300kHz with no harmonics at sub 20kHz audio band or at 455kHz IF band. Oscillator frequency is externally synchronizable from 200kHz to 400kHz.

Internal synchronous rectification and dual PFM/PWM mode of operation allows greater than 90% efficiency at light and full load. The ILC6382 is capable of delivering 75mA at 3.3V output from a single cell input.The ILC6382-XX offers 3.3V or 5V fixed output voltage while the ILC6382-Adj allows adjustable output voltage to 6V maximum. Output voltage accuracy is ±2% over specified temperature range.

Additional features include power good output ($\overline{POK}$) and an internal low battery detector with 100s transient rejection delay. The device will reject low battery input transients under 100msec in duration. The ILC6382 series is available in a space saving eight lead micro SOP (MSOP-8) package.

Features

- 0.9V to 6V input voltage
- Guaranteed start up at 0.9V input
- Synchronous rectification requires no external diode
- True load disconnect from battery input in shutdown
- Up to 75mA@3.3V and 40mA@5V from 1V input
- Up to 375mA@3.3V and 160mA@5V from 3V input
- Efficiency > 90% from 10mA to 150mA at V_{OUT} = 5V
- 1µA battery input current in shutdown (with V_{OUT} = 0V)
- Internal Oscillator frequency : 300kHz to ±15%
- External freq synchronization from 150kHz to 500kHz
- ILC6382 : Fixed 3.3V or 5V output
- ILC6382-Adj : Adjustable output to 6V maximum
- Low battery detector with 100ms transient rejection delay
- Powergood output flag when V_{OUT} is in regulation

Applications

- Cellular Phones, Pagers
- Palmtops, PDAs and portable electronics
- High efficiency 1V step up converters

Typical Circuit

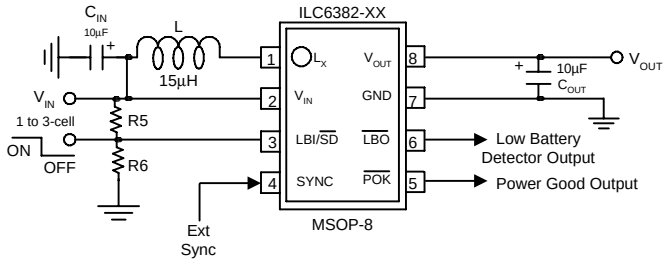


Figure 1: ILC6382

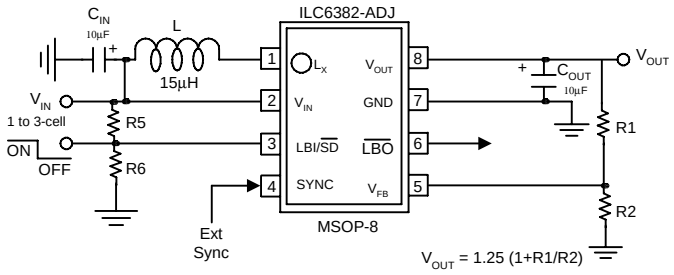
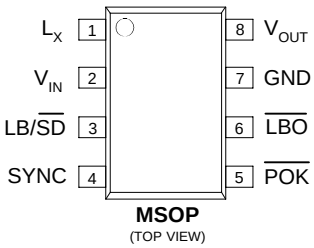


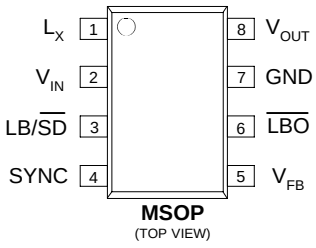
Figure 2: ILC6382-Adj

(Note: Pin 9 should be connected to ground if unused.)

Pin-Package Configurations



ILC6382CIR-XX



ILC6382CIR-ADJ

Ordering Information* (T_A = -40°C to + 85°C)	
ILC6382CIR-33	3.3V output, MSOP-8 package
ILC6382CIR-50	5V output, MSOP-8 package
ILC6382CIR-ADJ	Adjustable output, MSOP-8 package

Pin Functions ILC6382

Pin Number	Pin Name	Pin Description
1	L_x	Inductor input. Inductor L connected between this pin and the battery
2	V_{IN}	Connect directly to battery
3	LBI/$\overline{SD}$	Low battery detect input and shutdown. Low battery detect threshold is set with this pin using a potential divider. If this pin is pulled to logic low then the device will shutdown.
4	SYNC	A logic level signal referenced to V_{IN}, at a frequency between 150kHz and 500kHz on this pin will override the internal 300kHz oscillator. If the SYNC function is unused then pin 4 should be connected to ground
5	$\overline{POK}$ (ILC6382CIR-XX)	This open drain output pin will go high when output voltage is within regulation, $0.92*V_{OUT\ (NOM)} \leq V_{OUT} \leq 0.98*V_{OUT\ (NOM)}$
	V_{FB} (ILC6382CIR-ADJ)	This pin sets the adjustable output voltage via an external resistor divider network. The formula for choosing the resistors is shown in the “Applications Information“ section.
6	$\overline{LBO}$	This open drain output will go low if the battery voltage is below the low battery threshold set at pin 3
7	GND	Connect this pin to the battery and system ground
8	V_{OUT}	This is the regulated output voltage

Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Ratings	Units
Voltage on V_{OUT} pin	V_{OUT}	-0.3 to 7	V
Voltage on LBI, Sync, $\overline{LBO}$, $\overline{POK}$, V_{FB}, L_X and V_{IN} pins	-	-0.3 to 7	V
Peak switch current on L_X pin	IL_X	1	A
Current on $\overline{LBO}$ pin	$I_{sink(LBO)}$	5	mA
Continuous total power dissipation at 85 °C	P_d	400	mW
Short circuit current	I_{SC}	Internally protected (1 sec duration)	A
Operating ambient temperature	T_A	-40 to 85	°C
Maximum junction temperature	$T_{J\ (max)}$	170	°C
Storage temperature	T_{stg}	-40 to 125	°C
Lead temperature (soldering 10 sec)		300	°C
Package thermal resistance	θ_{JA}	206	°C/W

Electrical Characteristics ILC6382CIR-33

Unless otherwise specified all limits are at V_{OUT} =3.3V, V_{IRI} = 1.5V, Fosc = 300kHz and T_A = 25°C. Test circuit of figure 1. **BOLDFACE** type indicates limits that apply over the full operating temperature range. **Note 2.**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Voltage	V_{OUT}	$0.9V \le V_{IN} \le 3V$, I_{OUT}= 0mA	3.234	3.300	3.366	V
		$0.9V \le V_{IN} \le 3V$, I_{OUT}= 0mA	**3.201**		**3.399**	
Output Current	I_{OUT}	V_{IN} = 0.9V, $V_{OUT} = V_{OUT(nom)} \pm 4\%$		50		mA
		V_{IN} = 1.2V, $V_{OUT} = V_{OUT(nom)} \pm 4\%$		75		
		V_{IN} = 2.4V, $V_{OUT} = V_{OUT(nom)} \pm 4\%$		200		
		V_{IN} = 3.0V, $V_{OUT} = V_{OUT(nom)} \pm 4\%$		375		
Load Regulation	$\frac{\Delta V_{OUT}}{V_{OUT\ (no\ load)}}$	V_{IN} = 1.2V, $0mA \le I_{OUT} \le 50mA$		1.5		%
		V_{IN} = 1.2V, $0mA \le I_{OUT} \le 75mA$		2.4		
No Load Battery Input Current	$I_{IN(\ no\ load\ )}$	V_{IN} = 1.2V, I_{OUT} = 0mA		250		µA
Efficiency	η	V_{IN} = 1.2V, I_{OUT} = 3mA		82		%
		V_{IN} = 1.2V, I_{OUT}=30mA		90		

Electrical Characteristics ILC6382CIR-50

Unless otherwise specified all limits are at V_{OUT} = 5V, V_{IRI} = 1.5V, Fosc = 300kHz and T_A = 25°C. Test circuit of figure 1. **BOLDFACE** type indicates limits that apply over the full operating temperature range. **Note 2.**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Voltage	V_{OUT}	0.9V ≤ V_{IN} ≤ 3V, I_{OUT} = 0mA 0.9V ≤ V_{IN} ≤ 3V, I_{OUT} = 0mA	4.950 **4.900**	5.000	5.050 **5.100**	V
Output Current	I_{OUT}	V_{IN} = 1.2V, V_{OUT} = $V_{OUT(nom)}$ ± 4% V_{IN} = 2.4V, V_{OUT} = $V_{OUT(nom)}$ ± 4% V_{IN} = 3.0V, V_{OUT} = $V_{OUT(nom)}$ ± 4%		50 110 160		mA
Load Regulation		V_{IN} = 2.4V, 0mA ≤ I_{OUT} ≤ 60mA		3		%
No Load Battery Input Current	$I_{IN\ (\ no\ load\ )}$	V_{IN} = 2.4V, I_{OUT} = 0mA		250		µA
Efficiency	η	V_{IN} = 2.4V, I_{OUT} = 3mA V_{IN} = 2.4V, I_{OUT} =100mA		85 92		%

General Electrical Characteristics for all voltage versions.

Unless otherwise specified all limits are at V_{IN} = 2.4V, V_{IRI} = 1.5V, Fosc = 300kHz, I_{OUT} = 0mA and T_A = 25°C. Test circuits of figure 1 and figure 2 for ILC6382CIR-XX and ILC6382CIR-ADJ respectively. **BOLDFACE** type indicates limits that apply over the full operating temperature range. **Note 2.**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Minimum startup voltage	$V_{IN(start)}$	I_{OUT} = 0mA		0.9	**1**	V
Input voltage range	V_{IN}	V_{OUT} = $V_{OUT(nominal)}$ ± 4% I_{OUT} = 0mA **(Note 3)**	0.9 **1**		6 **6**	V
Battery input current in load disconnect mode	$I_{IN(SD)}$	$V_{LBI/SD}$ ≤ 0.4V, V_{OUT} = 0V (short circuit)		1	**2**	ΩA
Switch on resistance	$R_{ds(on)}$	N-Channel MOSFET P-Channel MOSFET		400 750		mΩ
Oscillator frequency	f_{osc}		**255**	300	**345**	kHz
External clock frequency range (sync)	f_{sync}		**150**		**500**	kHz
External clock pulse width	$t_{W(sync)}$	**Note 4**	**200**			ns
External clock rise/fall time	t_r / t_f	**Note 4**			**100**	ns
LBI input threshold	V_{REF}		1.175 **1.150**	1.250	1.325 **1.350**	V
Input leakage current	I_{LEAK}	Pins LBI/$\overline{SD}$, Sync and V_{FB}, **Note 4**			200	nA
LBI hold time	$t_{hold(LBI)}$	**Note 5**	**120**	100		ms

General Electrical Characteristics for all voltage versions (Continued).

Unless otherwise specified all limits are at V_{IN} = 2.4V, V_{LBI} = 1.5V, Fosc = 300kHz, I_{OUT} = 0mA and TA = 25°C. Test circuits of figure 1 and figure 2 for ILC6382-XX and ILC6382-ADJ respectively. **BOLDFACE** type indicates limits that apply over the full operating temperature range. **Note 2**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
LBO output voltage low	$V_{LBO(low)}$	I_{SINK} = 2mA, open drain output, V_{LBI} = 1V			**0.4**	V
LBO output leakage current	$I_{LBO(hi)}$	V_{LBO} = 5V		1	**2**	µA
Shutdown input voltage low	$V_{SD(low)}$				**0.4**	V
Shutdown input voltage high	$V_{SD(hi)}$		**1**		**6**	V
Sync input voltage low	$V_{sync(low)}$				**0.4**	V
Sync input voltage high	$V_{sync(hi)}$		**1**		**6**	V
POK output voltage low	$V_{\overline{POK}(low)}$	I_{SINK} = 2mA, open drain output			**0.4**	V
POK output voltage high	$V_{\overline{POK}(hi)}$				**6**	V
POK output leakage current	$I_{L(\overline{POK})}$	Force 6V at pin 5			**2**	µA
POK threshold	$V_{TH(\overline{POK})}$		0.92xV_{OUT}	0.95xV_{OUT}	0.98xV_{OUT}	V
POK hysteresis	V_{HYST}			50		mV
Feedback voltage (ILC6382 - ADJ only)	V_{FB}		1.225 **1.212**	1.250	1.275 **1.288**	V
Output voltage adjustment range (ILC6382CIR-ADJ only)	$V_{OUT(adj)\ min}$ $V_{OUT(adj)\ max}$	V_{IN} = 0.9V, I_{OUT} = 50mA V_{IN} = 3V, I_{OUT} = 50mA		2.5V 6		V

Note 1. Absolute maximum ratings indicate limits which, when exceeded, may result in damage to the component. Electrical specifications do not apply when operating the device outside its rated operating conditions.

Note 2. Specified min/max limits are production tested or guaranteed through correlation based on statistical control methods. Measurements are taken at constant junction temperature as close to ambient as possible using low duty pulse testing.

Note 3. $V_{OUT\ (NOM)}$ is the nominal output voltage at I_{OUT} = 0mA.

Note 4. Guaranteed by design.

Note 5. In order to get a valid low-battery-output (LBO) signal, the input voltage must be lower than the low-battery-input (LBI) threshold for a duration greater than the low battery hold time ($t_{hold(LBI)}$). This feature eliminates false triggering due to voltage transients at the battery terminal.

APPLICATIONS INFORMATION

The ILC6382 performs boost DC-DC conversion by controlling the switch element as shown in the simplified circuit in figure 3 below.

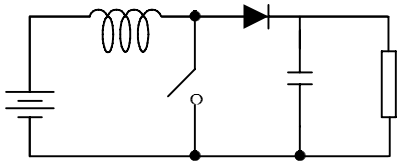


Figure 3: Basic Boost Circuit

When the switch is closed, current is built up through the inductor. When the switch opens, this current has to go somewhere and is forced through the diode to the output. As this on and off switching continues, the output capacitor voltage builds up due to the charge it is storing from the inductor current. In this way, the output voltage gets boosted relative to the input.

In general, the switching characteristic is determined by the output voltage desired and the current required by the load. Specifically the energy transfer is determined by the power stored in the coil during each switching cycle.

$P_L = f(t_{ON}, V_{IN})$

Synchronous Rectification

The ILC6382 also uses a technique called "synchronous rectification" which removes the need for the external diode used in other circuits. The diode is replaced with a second switch or in the case of the ILC6382, an FET as shown in figure 4 below.

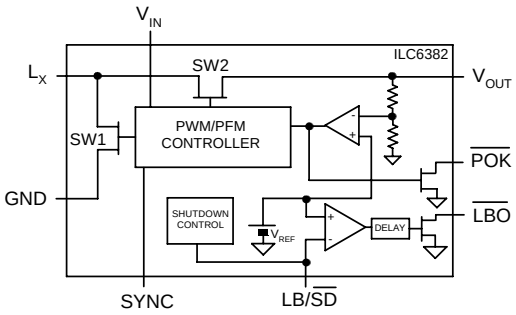


Figure 4: Simplified ILC6382 block diagram

The two switches now open and close in opposition to eachother, directing the flow of current to either charge the inductor or to feed the load. The ILC6382 monitors the voltage on the output capacitor to determine how much and how often to drive the switches.

PWM Mode Operation

The ILC6382 uses a PWM or Pulse Width Modulation technique. The switches are constantly driven at typically 300kHz. The control circuitry varies the power being delivered to the load by varying the on-time, or duty cycle, of the switch SW1 (see fig. 5). Since more on-time translates to higher current build-up in the inductor, the maximum duty cycle of the switch determines the maximum load current that the device can support.

There are two key advantages of the PWM type controllers. First, because the controller automatically varies the duty cycle of the switch's on-time in response to changing load conditions, the PWM controller will always have an optimized waveform for a steady-state load. This translates to very good efficiency at high currents and minimal ripple on the output. Ripple is due to the output cap constantly accepting and storing the charge received from the inductor, and delivering charge as required by the load. The "pumping" action of the switch produces a sawtooth-shaped voltage as seen by the output.

The other key advantage of the PWM type controllers is that the radiated noise due to the switching transients will always occur at the (fixed) switching frequency. Many applications do not care much about switching noise, but certain types of applications, especially communication equipment, need to minimize the high frequency interference within their system as much as possible. Using a boost converter requires a certain amount of higher frequency noise to be generated; using a PWM converter makes that noise highly predictable thus easier to filter out.

PFM Mode Operation

There are downsides of PWM approaches, especially at very low currents. Because the PWM technique relies on constant switching and varying duty cycle to match the load conditions, there is some point where the load current gets too small to be handled efficiently. An actual switch consumes some finite amount of current to switch on and off; at very low currents this can be of the same magnitude as the load current itself, driving switching efficiencies down to 50% and below. The ILC6382 overcomes this limitation by automatically switching over to a PFM, or Pulse Frequency Modulation, technique at low currents. This technique conserves power loss by only switching the output if the current drain requires it. As shown in the figure 5, the waveform actually skips pulses depending on the power needed by the output. This technique is also called "pulse skipping" because of this characteristic.

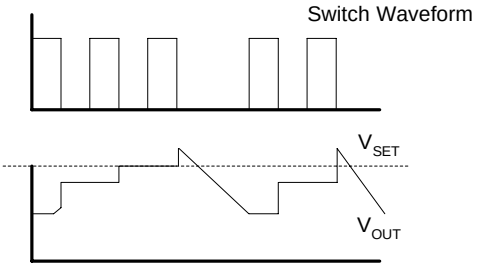


Figure 5: PFM Waveform

In the ILC6382, the switchover from PWM to PFM mode occurs when the PWM waveform drops to a low duty cycle. The low PWM duty cycle indicates to the controller that the load current is small and so it switches over to the PFM mode to improve efficiency and conserve power.

The Dual PWM/PFM mode architecture was designed specifically for applications such as wireless communications, which need the spectral predictability of a PWM-type DC-DC converter, yet also need the highest efficiencies possible, especially in Standby mode.

Other Considerations

The other limitation of PWM techniques is that, while the fundamental switching frequency is easier to filter out since it's constant, the higher order harmonics of PWM will be present and may have to be filtered out, as well. Any filtering requirements, though, will vary by application and by actual system design and layout, so generalizations in this area are difficult, at best.

However, PWM control for boost DC-DC conversion is widely used, especially in audio-noise sensitive applications or applications requiring strict filtering of the high frequency components.

External Frequency Syncronization

External frequency syncronization is allowed on the ILC6382. When an external signal between 150kHz to 500kHz is connected to pin 4, the internal oscillator will be over-ridden. This technique is useful when designers wish to synchronize two or more converters using the same external source in order to avoid unexpected harmonics. **Connect pin 4 to ground or V_{IN} if the external frequency syncronization function is not used.**

Low Battery Detector

The ILC6382's low battery detector is a based on a CMOS comparator. The negative input of the comparator is tied to an internal 1.25V (nominal) reference, V_{REF}. The positive input is the LBI/$\overline{SD}$ pin. It uses a simple potential divider arrangement with two resistors to set the LBI threshold as shown in Figure 6. The input bias current of the LBI pin is only 200nA. This means that the resistor values R1 and R2 can be set quite high. The formula for setting the LBI threshold is:

VLBI = VREF x (1+R5/R6)

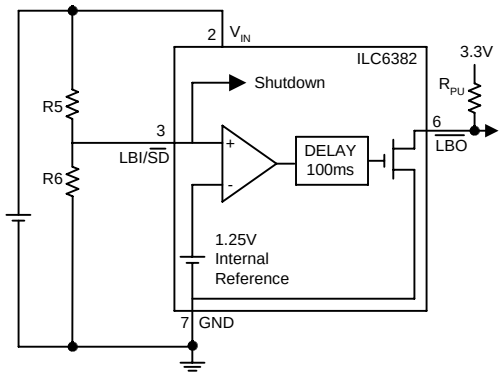


Figure 6: Low Battery Detector

Since the LBI input current is negligible (<200nA), this equation is derived by applying voltage divider formula across R6. A typical value for R6 is 100kΩ.

R5 = 100kΩ x [(V_{LBI}/V_{REF}) -1], where V_{REF}=1.25V (nom.)

The LBI detector has a built in delay of 120ms. In order to get a valid low-battery-output (LBO) signal, the input voltage must be lower than the low-battery-input (LBI) threshold for a duration greater than the low battery hold time ($t_{hold(LBI)}$) of 120msec. This feature eliminates false triggering due to voltage transients at the battery terminal caused by high frequency switching currents.

The output of the low battery detector is an open drain capable of sinking 2mA. A 10kΩ pull-up resistor is recommended on this output. **Note that when the device is not in PWM mode or is in shutdown the low battery detector does not operate.**

For VLBI < 1.25V

The low battery detector can also be configured for voltages <1.25V by bootstrapping the LBI input from V_{OUT}. The circuitry for this is shown in figure 7.

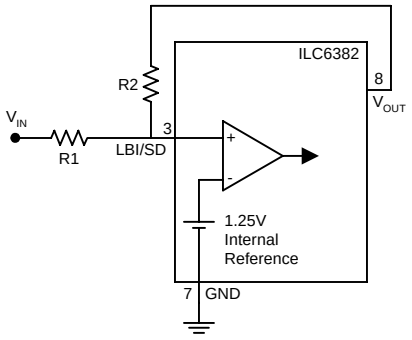


Figure 7: V_{LBI} < 1.25V

The following equation is used when V_{IN} is lower than 1.25V:

$R1 = R2 \times [(V_{REF} - V_{IN}) / (V_{OUT} - V_{REF})]$,
where V_{REF} = 1.25V (nom.)

This equation can also be derived using voltage divider formula across R2. A typical value for R2 is 100kΩ. **Note that the low battery detector does not operate when the ILC6382 is in PFM mode or in shutdown.**

Shut Down

The LBI pin is shared with the shutdown pin. A low voltage (<0.4V) will put the ILC6382 into a power down state. The simplest way to implement this is with an FET across R6 as shown in figure 8. Note that when the device is not in PWM mode or is in shutdown the low battery detector does not operate.

When the ILC6382 is shut down, the synchronous rectifier disconnects the output from the input. This ensures that there is only leakage (I_{IN} < 1µA typical) from the input to the output so that the battery is not drained when the ILC6382 is shut down.

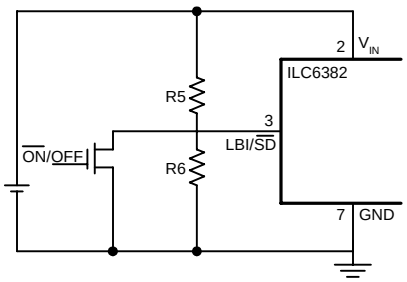


Figure 8: Shut Down Control

Power Good Output ($\overline{POK}$)

The $\overline{POK}$ output of the ILC6382 indicates when V_{OUT} is within the regulation tolerance of the set output voltage. $\overline{POK}$ output is an open drain device output capable of sinking 2mA. It will remain pulled low until the output voltage has risen to typically 95% of the specified V_{OUT}. Note that a pull-up resistor must be connected from the $\overline{POK}$ output (pin 5 of ILC6382CIR-XX) to either ILC6382's output or to some other system voltage source.

Adjustable Output Voltage Selection

The ILC6382-ADJ allows the output voltage to be set using a potential divider. The formula for setting the adjustable output voltage is;

$V_{OUT} = V_{FB} \times (1+R1/R2)$
Where V_{FB} is the threshold set which is 1.25V nominal.

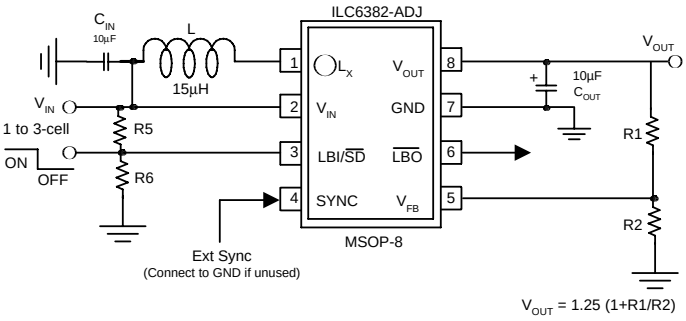


Figure 9: Adjustable Voltage Configuration

Negative Voltage Output

It is possible to generate a negative output voltage as a secondary supply using the ILC6382. This negative voltage may be useful in some applications where a negative bias voltage at low current is required.

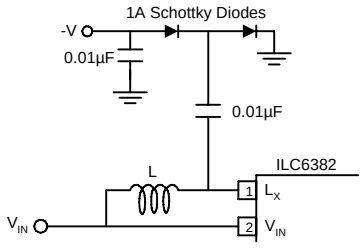


Figure 10: Negative Output Votlage

External Component Selection

Inductors

The ILC6382 is designed to work with a 15µH inductor in most applications. There are several vendors who supply standard surface mount inductors to this value. Suggested suppliers are shown in table 1. Higher values of inductance will improve efficiency, but will reduce peak inductor current and consequently ripple and noise, but will also limit output current.

Vendor	Part No	Contact
Coilcraft	DO3308P-153 D03316P-153 D01608C-153	(847) 639 6400
muRata	LQH4N150K LQH3C150K	(814) 237 1431
Sumida	CDR74B-150MC CD43-150 CD54-150	(847) 956 0666
TDK	NLC453232T-150K	(847) 390 4373

Capacitors

Input Capacitor

The input capacitor is necessary to minimize the peak current drawn from the battery. Typically a 10µF tantalum capacitor is recommended. Low equivalent series resistance (ESR) capacitors will help to minimize battery voltage ripple.

Output Capacitor

Low ESR capacitors should be used at the output of the ILC6382 to minimize output ripple. The high switching speeds and fast changes in the output capacitor current, mean that the equivalent series impedance of the capacitor can contribute greatly to the output ripple. In order to minimize these effects choose an output capacitor with less than 10nH of equivalent series inductance (ESL) and less than 100mΩ of equivalent series resistance (ESR). Typically these characteristics are met with ceramic capacitors, but may also be met with certain types of tantalum capacitors. Suitable vendors are shown in table 2.

Description	Vendor	Contact
T495 series tantalum	Kemet	(864) 963 6300
595D series tantalum	Sprague	(603) 224 1961
TAJ, TPS series tantalum	AVX	(803) 946 0690
X7R Ceramic	TDK	(847) 390 4373
	AVX	(803) 946 0690

Layout and Grounding Considerations

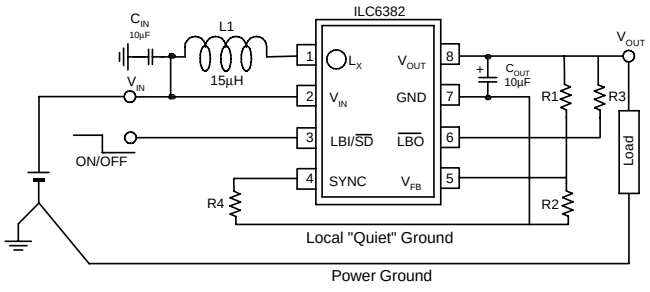
High frequency switching and large peak currents means PCB design for DC-DC converters requires careful consideration. A general rule is to place the DC-DC converter circuitry well away from any sensitive RF or analog components. The layout of the DC-DC converters and its external components are also based on some simple rules to minimise EMI and output voltage ripple.

Layout

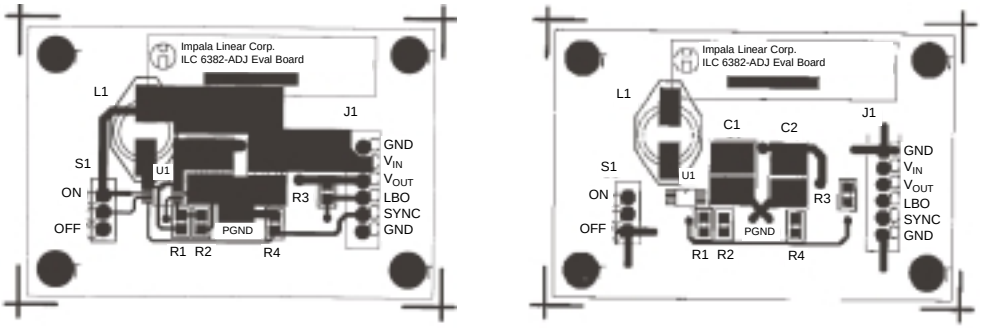
1. Place all power components, ILC6382, inductor, input capacitor and output capacitor as close together as possible.
2. Keep the output capacitor as close to the ILC6382 as possible with very short traces to the VOUT and GND pins. Typically it should be within 0.25 inches or 6mm.
3. Keep the traces for the power components wide, typically >50mil or 1.25mm.
4. Place the external networks for LBI and VFB close to the ILC6382, but away from the power components as far as possible.

Grounding

1. Use a star grounding system with separate traces for the power ground and the low power signals such as LBI/SD and VFB. The star should radiate from where the power supply enters the PCB.
2. On multilayer boards use component side copper for grounding around the ILC6382 and connect back to a quiet ground plane using vias.



Recommended application circuit schematic for ILC6382CIR-ADJ



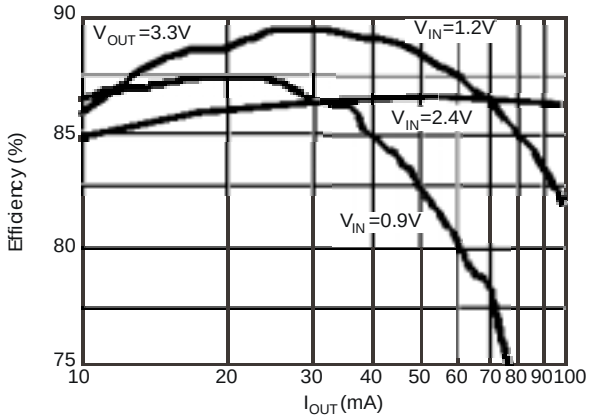
Evaluation Board Parts List For Printed Circuit Board Shown Above

Label	Part Number	Manufacturer	Description
U1	ILC6382CIR-ADJ	Impala Linear	Step-up DC-DC converter
C_{IN}, C_{OUT}	2221Y106M250NT	Novacap	10µF, ceramic capacitor
L1	DO1608C-153	Coilcraft	15µH, 0.15Ω inductor
R1 and R2	-	Dale, Panasonic	User determined values
R3	-	Dale, Panasonic	10kΩ, 1/10W, SMT
R4	-	Dale, Panasonic	1MegΩ, 1/10W, SMT

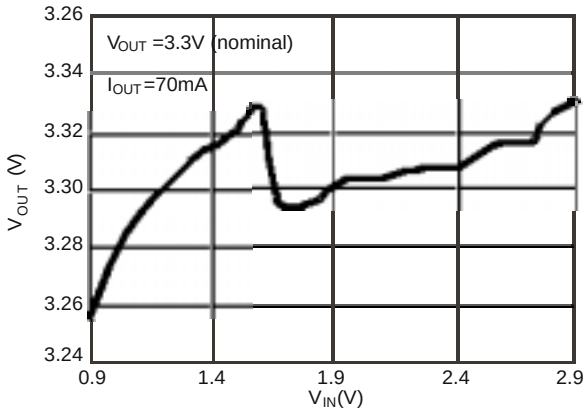
Typical Performance Characteristics ILC6382CIR-33 (V_{OUT} = 3.3 V)

Unless otherwise specified: T_A = 25°C, C_{IN} = 10µF, C_{OUT} = 10µF, L = 10µH

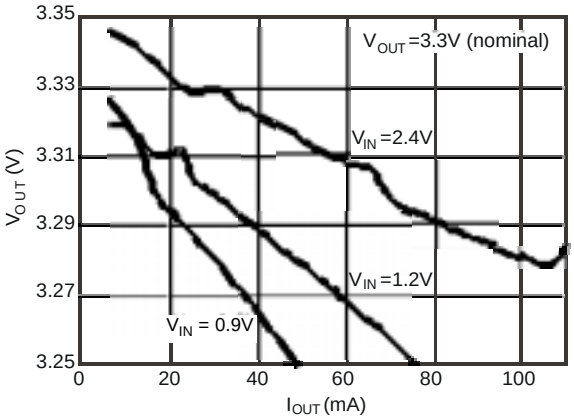
Efficiency



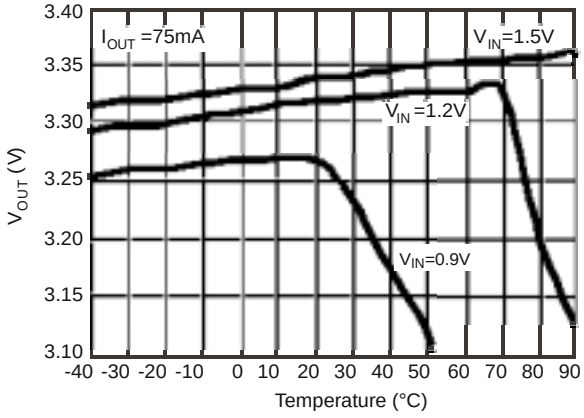
Line Regulation



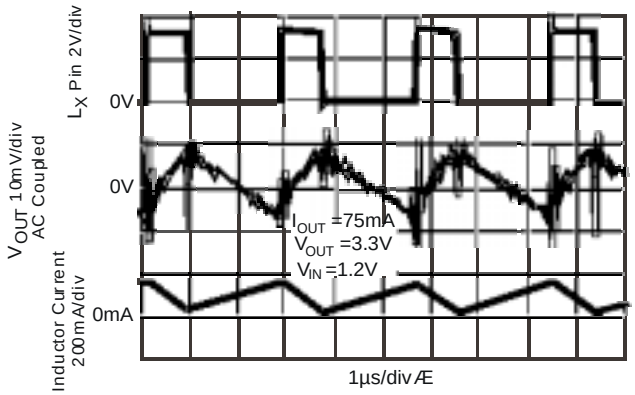
Load Regulation



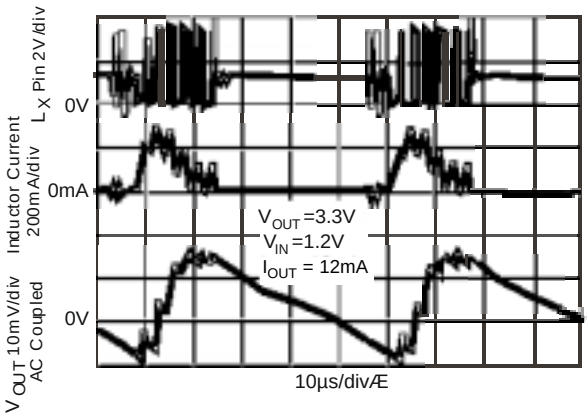
V_{OUT} vs Temperature



Load Switching Waveforms (PWM Mode)



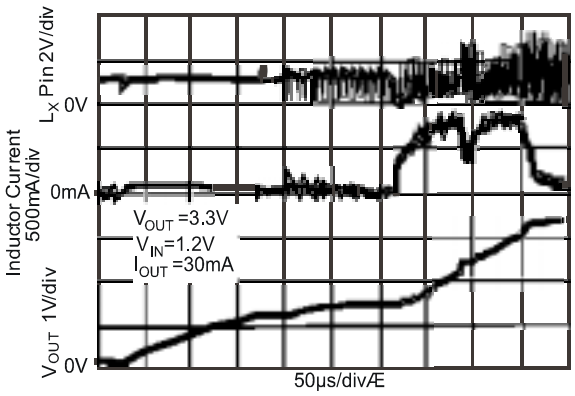
Load Switching Waveforms (PFM Mode)



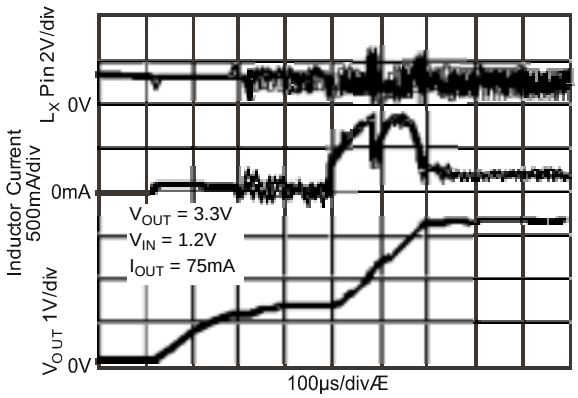
Typical Performance Characteristics ILC6382CIR-33 (V_{OUT} = 3.3V)

Unless otherwise specified: T_A = 25°C, C_{IN} = 10µF, C_{OUT} = 10µF, L = 15µH.

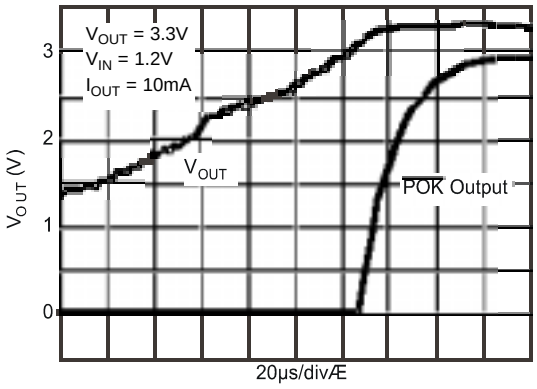
Start-up



Start-up

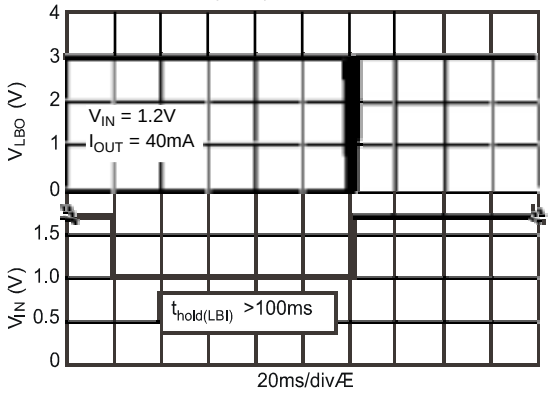


Power Good Output ($\overline{POK}$)



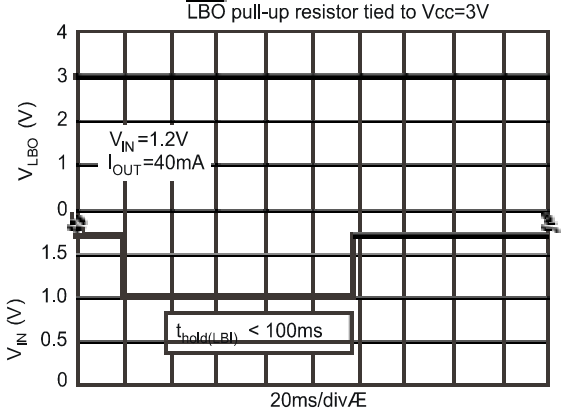
Low Battery Output (V_{IN}<V_{TH} for Greater than 100ms)

$\overline{LBO}$ pull-up resistor tied to Vcc=3V

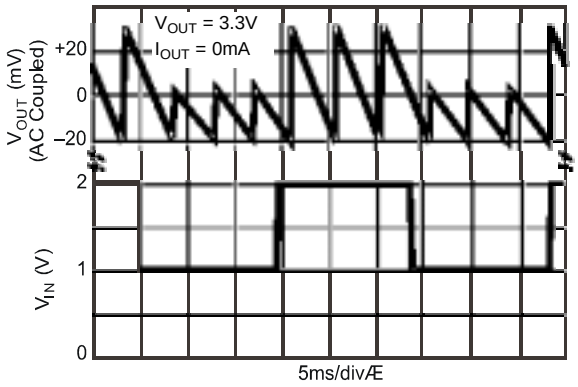


Low Battery Output (V_{IN}<V_{TH} for Less than 100ms)

$\overline{LBO}$ pull-up resistor tied to Vcc=3V



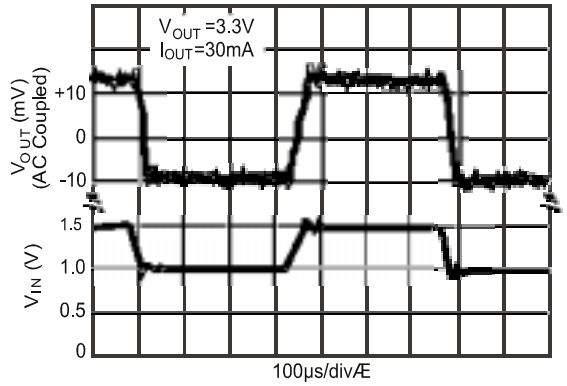
Line Transient Response (PFM mode)



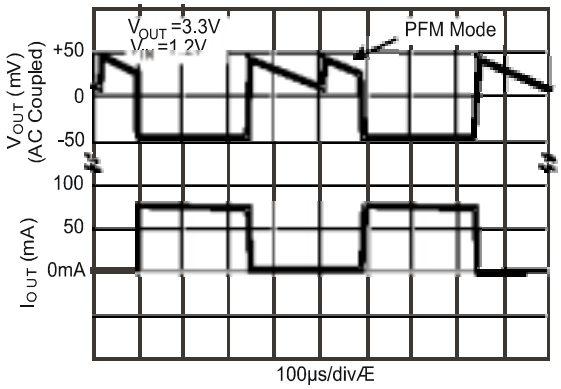
Typical Performance Characteristics ILC6382CIR-33 (V_{OUT} = 3.3V)

Unless otherwise specified: T_A = 25°C, C_{IN} = 10µF, C_{OUT} = 10µF, L = 15µH.

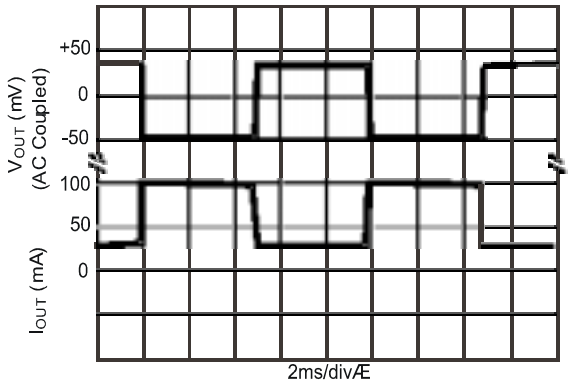
Line Transient Response (PWM mode)



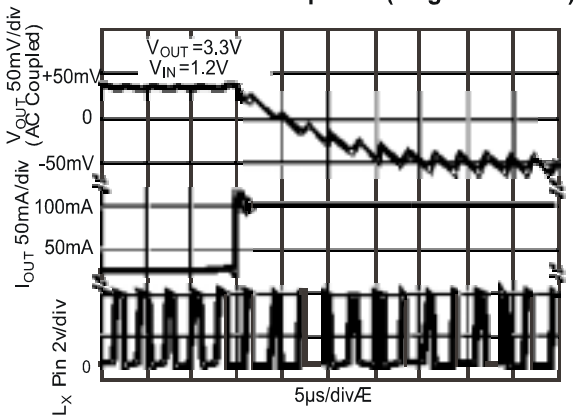
Load Transient Response (0 mA to 75 mA Load Step)



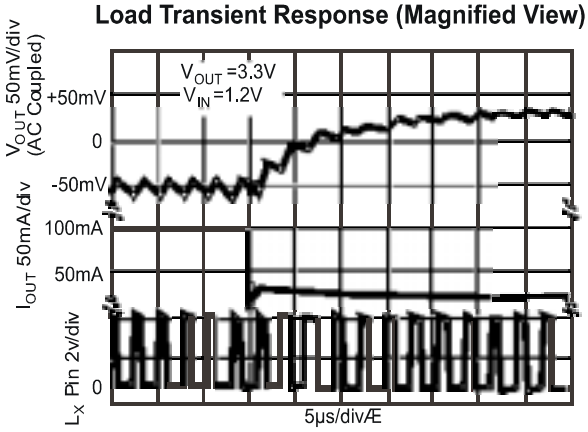
Load Transient Response (25 mA to 100 mA Load Step)



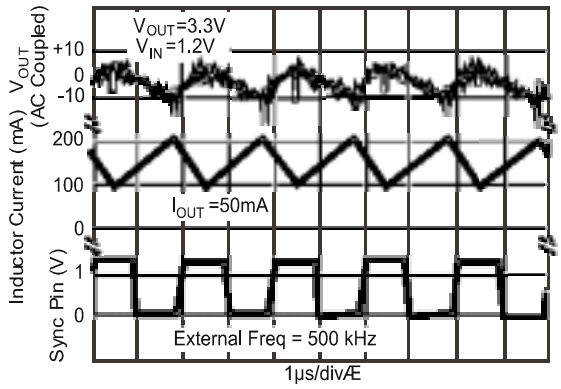
Load Transient Response (Magnified View)



Load Transient Response (Magnified View)



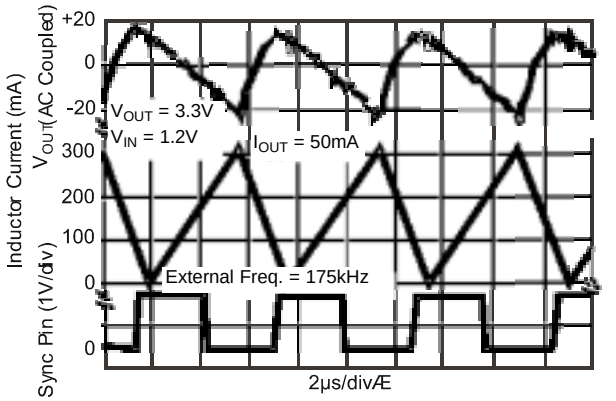
External Frequency Synchronization (Pin 4)



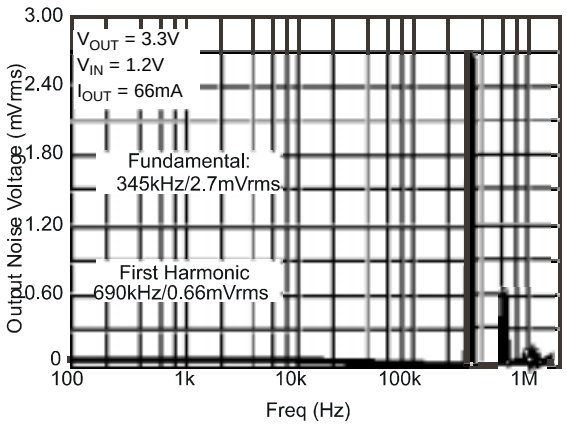
Typical Performance Characteristics ILC6382CIR-33 (V_{OUT} = 3.3V)

Unless otherwise specified: T_A = 25°C, C_{IN} = 10µF, C_{OUT} = 10µF, L = 15µH.

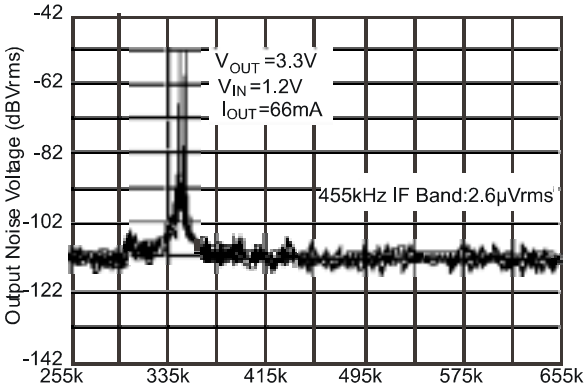
External Frequency Synchronization (Pin 4)



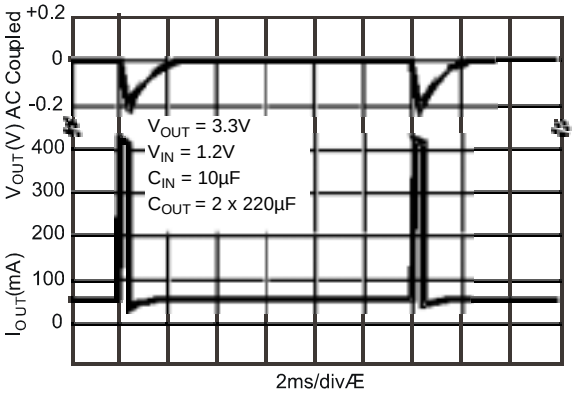
Spectral Noise Plot



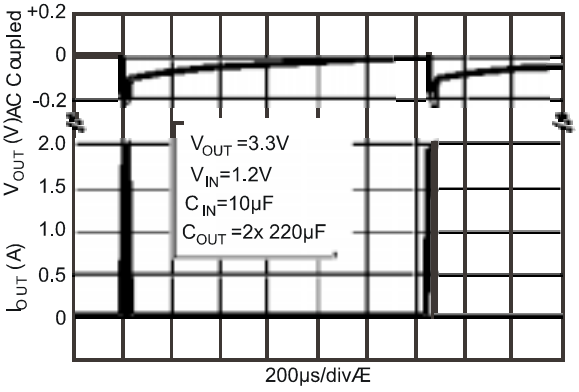
Spectral Noise Plot



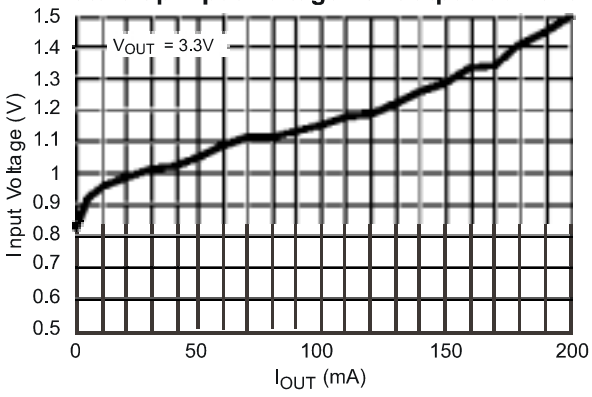
DECT Transient Response



2A, 30µs Load Transient Response



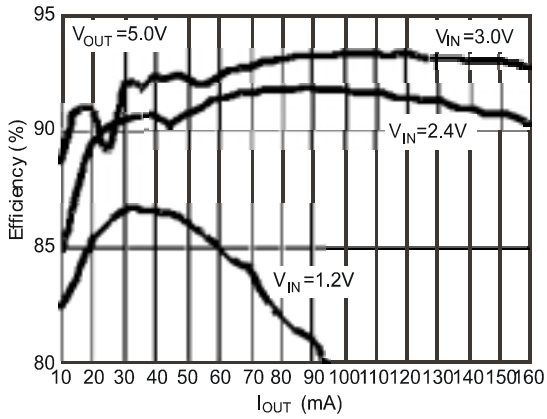
Start-Up Input Voltage vs. Output Current



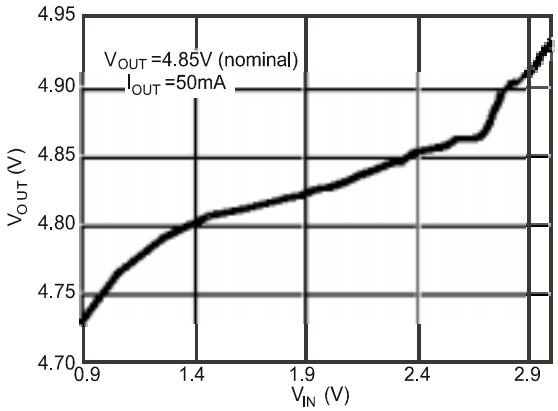
Typical Performance Characteristics ILC6382CIR-33 (V_{OUT} = 3.3V)

Unless otherwise specified: T_A = 25°C, C_{IN} = 10µF, C_{OUT} = 10µF, L = 15µH.

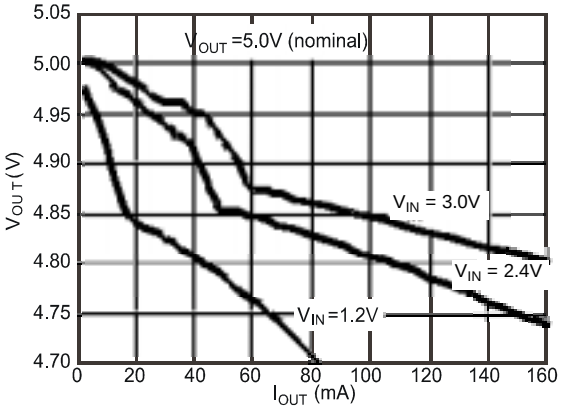
Efficiency



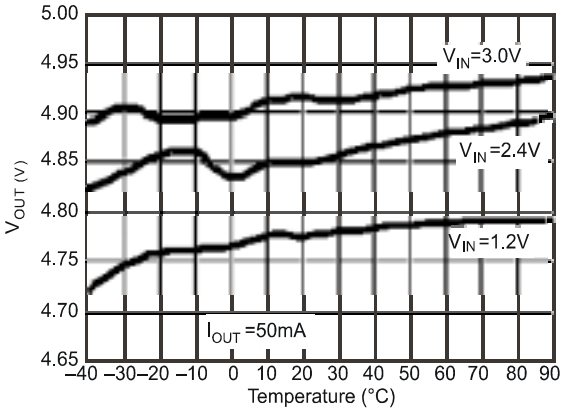
Line Regulation



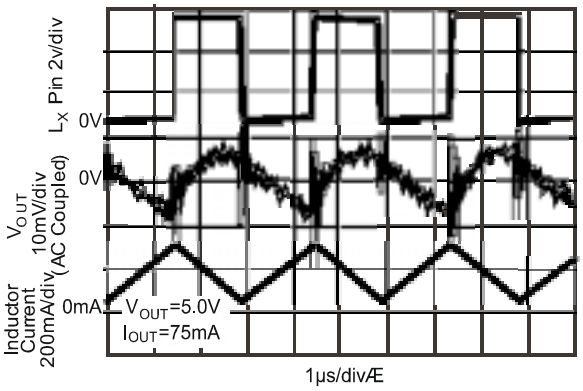
Load Regulation



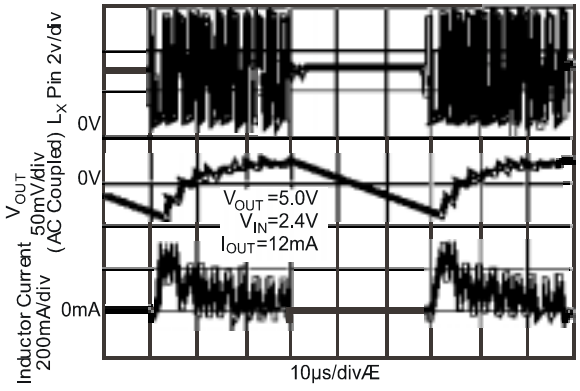
V_{OUT} vs Temperature



Load Switching Waveforms (PWM Mode)



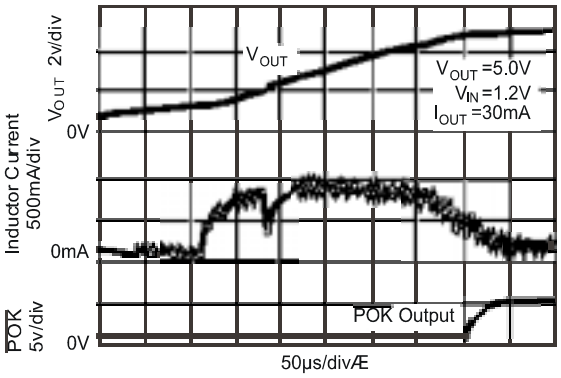
Load Switching Waveforms (PFM Mode)



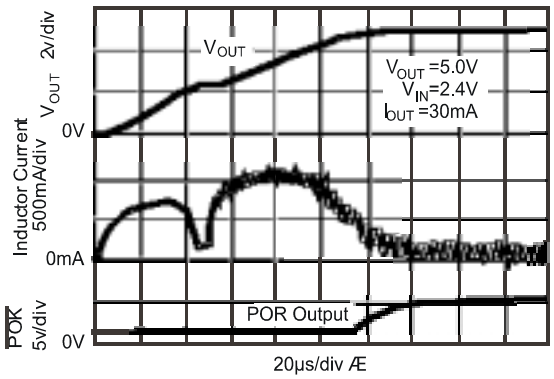
Typical Performance Characteristics ILC6382CIR-33 (V_{OUT} = 3.3V)

Unless otherwise specified: T_A = 25°C, C_{IN} = 10µF, C_{OUT} = 10µF, L = 15µH.

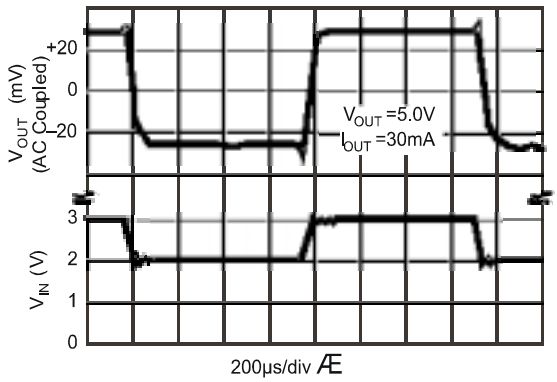
Startup and Power Good Output ($\overline{POK}$)



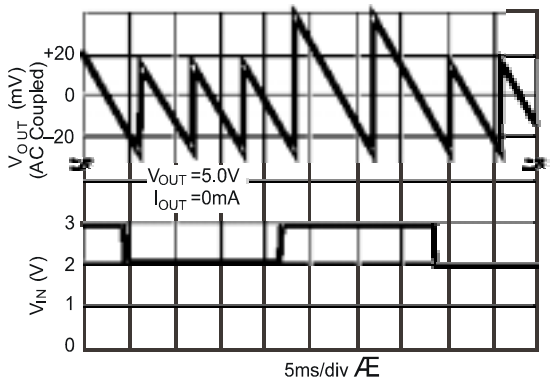
Startup and Power Good Output ($\overline{POK}$)



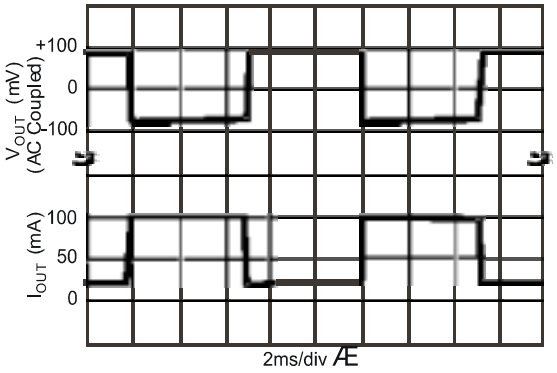
Line Transient Response (PWM Mode)



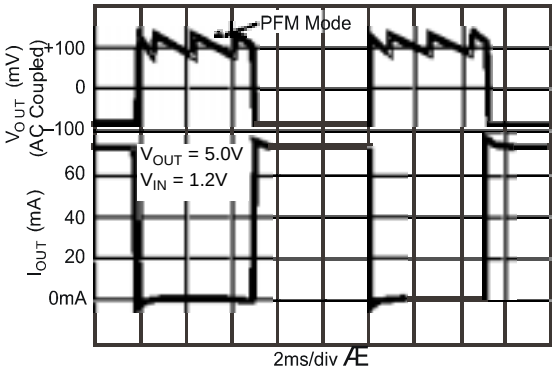
Line Transient Response (PFM Mode)



Load Transient Response (20mA to 100mA Load Step)



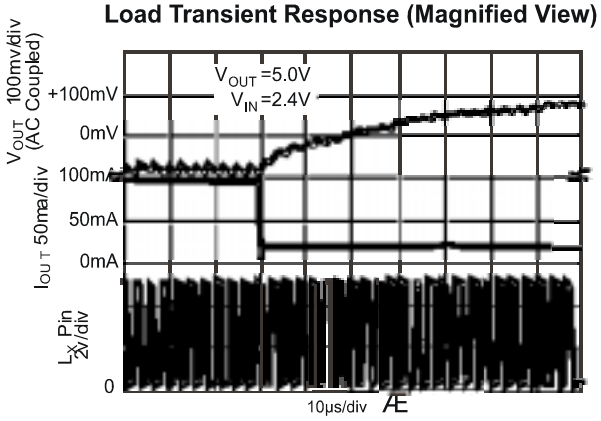
Load Transient Response (0mA to 80mA load step)



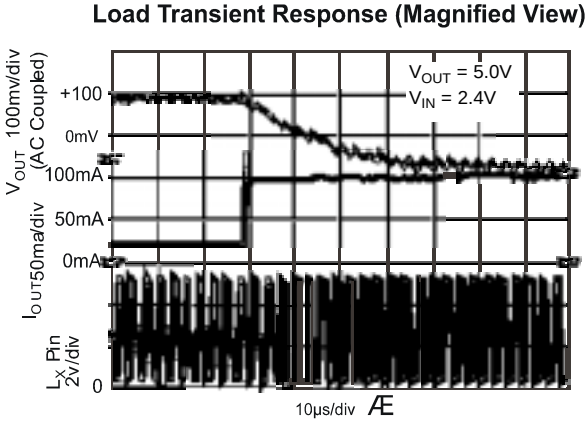
Typical Performance Characteristics ILC6382CIR-33 (V_{OUT} = 3.3V)

Unless otherwise specified: T_A = 25°C, C_{IN} = 10µF, C_{OUT} = 10µF, L = 15µH.

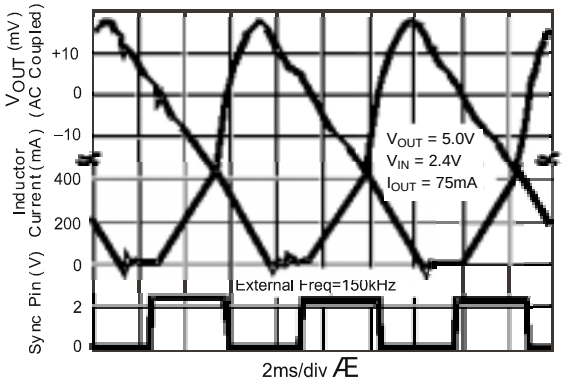
Load Transient Response (Magnified View)



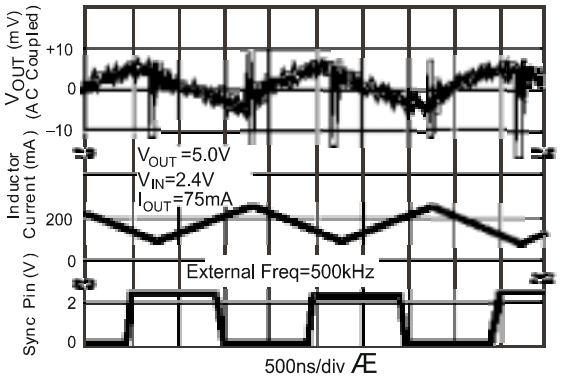
Load Transient Response (Magnified View)



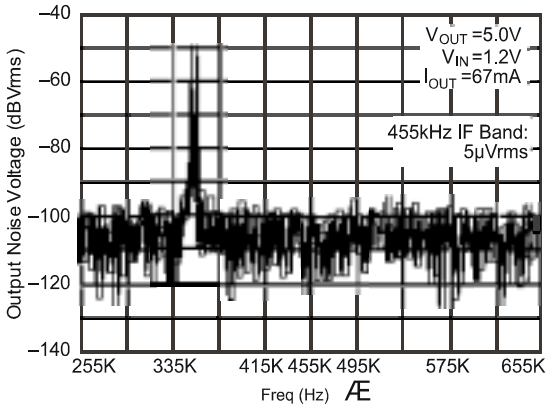
External Frequency Synchronization (Pin 4)



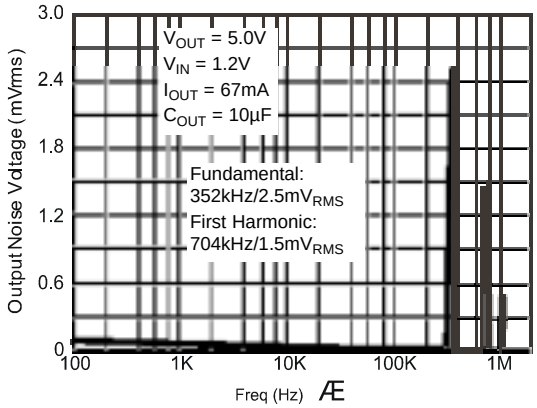
External Frequency Synchronization (Pin 4)



Spectral Noise Plot



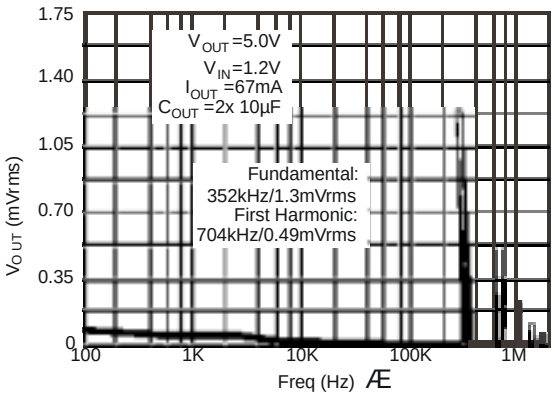
Spectral Noise Plot



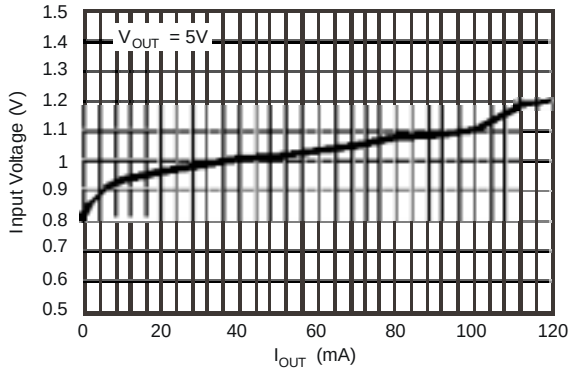
Typical Performance Characteristics ILC6382CIR-33 (V_{OUT} = 3.3V)

Unless otherwise specified: T_A = 25°C, C_{IN} = 10µF, C_{OUT} = 10µF, L = 15µH.

Spectral Noise Plot



Start-Up Input Voltage vs. Output Current



Package Dimensions

MSOP-8

All dimensions in inches