

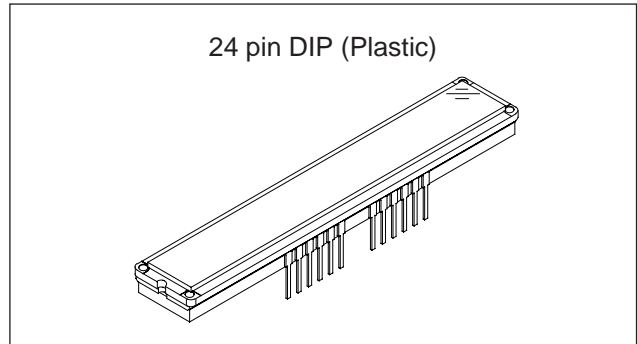
## 10680 pixel × 3 line CCD Linear Sensor (Color)

### Description

The ILX550K is a reduction type CCD linear sensor developed for color image scanner. This sensor reads A4-size documents at a density of 1200DPI.

### Features

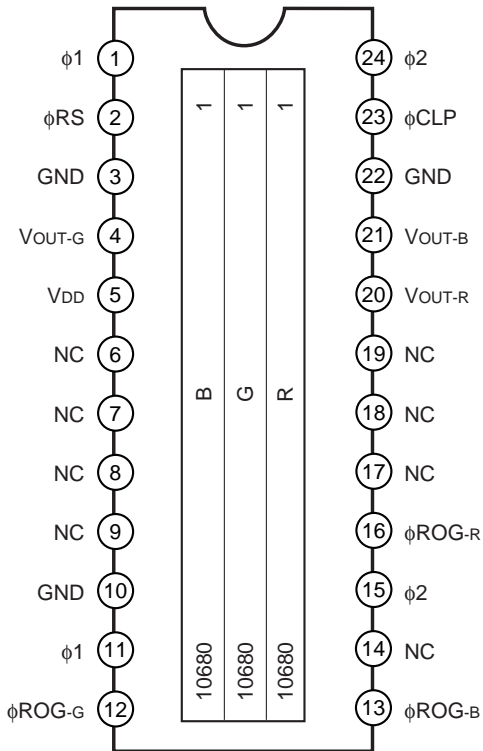
- Number of effective pixels: 32040 pixels  
(10680 pixels × 3)
- Pixel size: 4μm × 4μm (4μm pitch)
- Distance between line: 32μm (8 lines)
- Single-sided readout
- Ultra low lag/High sensitivity
- Single 12V power supply
- Maximum data rate: 5MHz/Color
- Input Clock Pulse: CMOS 5V drive
- Number of output: 3 (R, G, B)
- Package: 24 pin Plastic DIP (400mil)



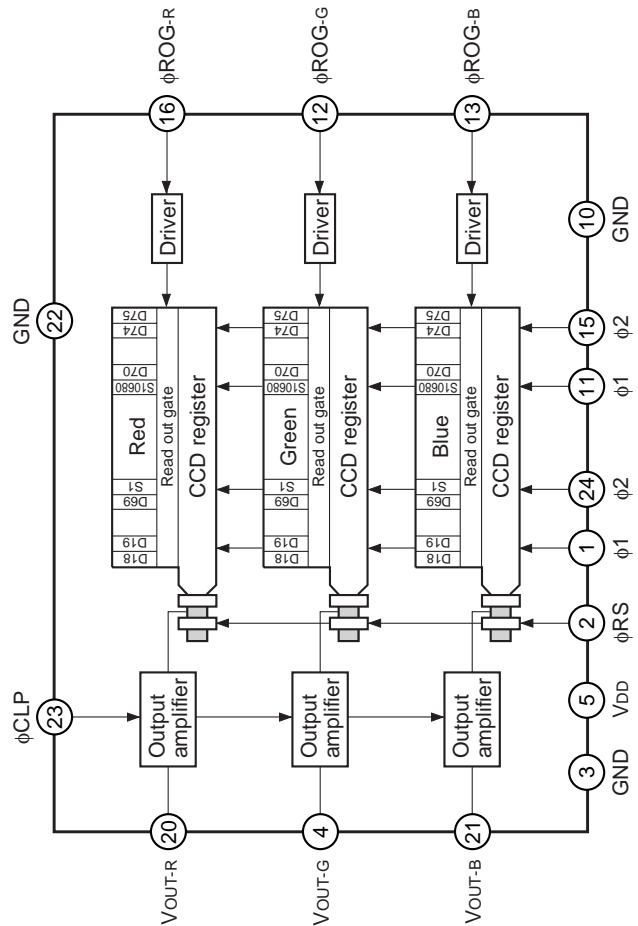
### Absolute Maximum Ratings

- Supply voltage V<sub>DD</sub> 15 V
- Operating temperature -10 to +55 °C

### Pin Configuration (Top View)



### Block Diagram



Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

## Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	$\phi 1$	Clock pulse input	13	$\phi\text{ROG-B}$	Clock pulse input
2	$\phi\text{RS}$	Clock pulse input	14	NC	NC
3	GND	GND	15	$\phi 2$	Clock pulse input
4	$V_{\text{OUT-G}}$	Signal output (green)	16	$\phi\text{ROG-R}$	Clock pulse input
5	$V_{\text{DD}}$	12V power supply	17	NC	NC
6	NC	NC	18	NC	NC
7	NC	NC	19	NC	NC
8	NC	NC	20	$V_{\text{OUT-R}}$	Signal output (red)
9	NC	NC	21	$V_{\text{OUT-B}}$	Signal output (blue)
10	GND	GND	22	GND	GND
11	$\phi 1$	Clock pulse input	23	$\phi\text{CLP}$	Clock pulse input
12	$\phi\text{ROG-G}$	Clock pulse input	24	$\phi 2$	Clock pulse input

## Recommended Supply Voltage

Item	Min.	Typ.	Max.	Unit
$V_{\text{DD}}$	11.4	12	12.6	V

## Clock Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacity of $\phi 1$ , $\phi 2$	$C_{\phi 1}$ , $C_{\phi 2}$	—	500	—	pF
Input capacity of $\phi\text{RS}$	$C_{\phi\text{RS}}$	—	10	—	pF
Input capacity of $\phi\text{CLP}$	$C_{\phi\text{CLP}}$	—	10	—	pF
Input capacity of $\phi\text{ROG}$	$C_{\phi\text{ROG}}$	—	10	—	pF

## Clock Frequency

Item	Symbol	Min.	Typ.	Max.	Unit
Frequency of $\phi 1$ , $\phi 2$ , $\phi\text{RS}$ , $\phi\text{CLP}$	$f_{\phi 1}$ , $f_{\phi 2}$ , $f_{\phi\text{RS}}$ , $f_{\phi\text{CLP}}$	—	1	5	MHz

## Input Clock Pulse Voltage Condition

Item		Min.	Typ.	Max.	Unit
$\phi 1$ , $\phi 2$ , $\phi\text{RS}$ , $\phi\text{CLP}$ , $\phi\text{ROG}$ pulse voltage	High level	4.75	5.0	5.25	V
	Low level	—	0	0.1	V

**Electrooptical Characteristics (Note 1)**

(Ta = 25°C, VDD = 12V, f<sub>PHS</sub> = 1MHz, Input clock = 5Vp-p, Light source = 3200K, IR cut filter CM-500S (t = 1.0mm))

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks	
Sensitivity	Red	R <sub>R</sub>	1.8	2.7	3.6	V/(lx · s)	Note 2
	Green	R <sub>G</sub>	2.1	3.3	4.5		
	Blue	R <sub>B</sub>	1.7	2.6	3.5		
Sensitivity nonuniformity	PRNU	—	4	20	%	Note 3	
Saturation output voltage	V <sub>SAT</sub>	2	2.5	—	V	Note 4	
Saturation exposure	Red	SE <sub>R</sub>	0.56	0.93	—	lx · s	Note 5
	Green	SE <sub>G</sub>	0.44	0.76	—		
	Blue	SE <sub>B</sub>	0.57	0.96	—		
Dark voltage average	V <sub>DRK</sub>	—	2	5	mV	Note 6	
Dark signal nonuniformity	DSNU	—	4	12	mV	Note 6	
Image lag	IL	—	0.02	—	%	Note 7	
Supply current	I <sub>VDD</sub>	—	25	50	mA		
Total transfer efficiency	TTE	92	98	—	%		
Output impedance	Z <sub>o</sub>	—	450	—	Ω		
Offset level	V <sub>OS</sub>	—	7.3	—	V	Note 8	

**Notes)**

- In accordance with the given electrooptical characteristics, the black level is defined as the average value of D18, D19 to D67.
- For the sensitivity test light is applied with a uniform intensity of illumination.
- PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 2.

$$V_{OUT-G} = 500\text{mV (Typ.)}$$

$$PRNU = \frac{(V_{MAX} - V_{MIN})/2}{V_{AVE}} \times 100 [\%]$$

Where the 5340 pixels are divided into blocks of 100, the maximum output of each block is set to V<sub>MAX</sub>, the minimum output to V<sub>MIN</sub> and the average output to V<sub>AVE</sub>.

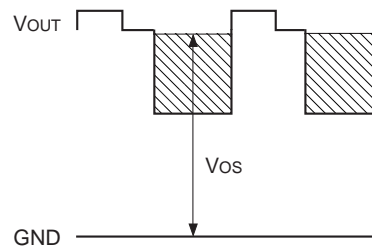
- Use below the minimum value of the saturation output voltage.
- Saturation exposure is defined as follows.

$$SE = \frac{V_{SAT}}{R}$$

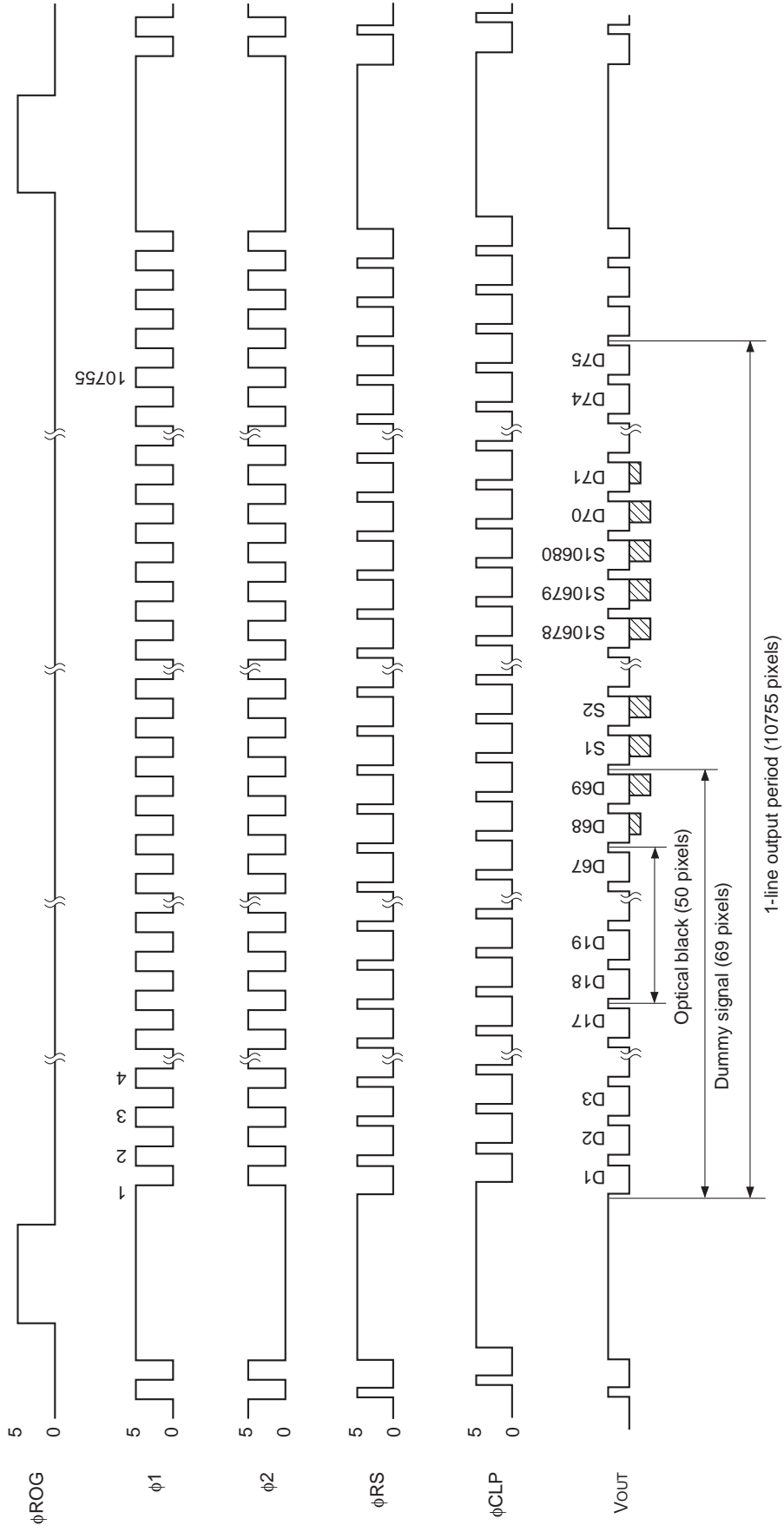
Where R indicates R<sub>R</sub>, R<sub>G</sub>, R<sub>B</sub>, and SE indicates SE<sub>R</sub>, SE<sub>G</sub>, SE<sub>B</sub>.

- Optical signal accumulated time τ<sub>int</sub> stands at 5.5ms.
- V<sub>OUT-G</sub> = 500mV (Typ.)
- V<sub>OS</sub> is defined as indicated below.

V<sub>OUT</sub> indicates V<sub>OUT-R</sub>, V<sub>OUT-G</sub> and V<sub>OUT-B</sub>.

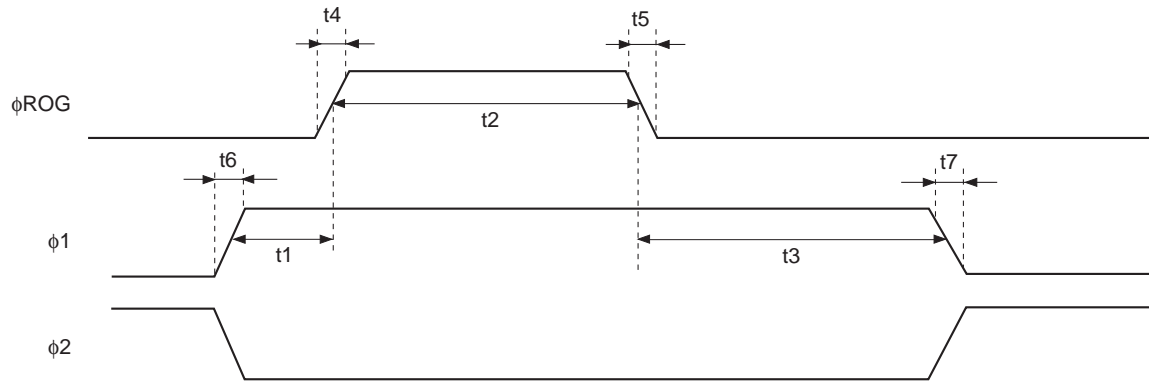


**Clock Timing Chart 1**

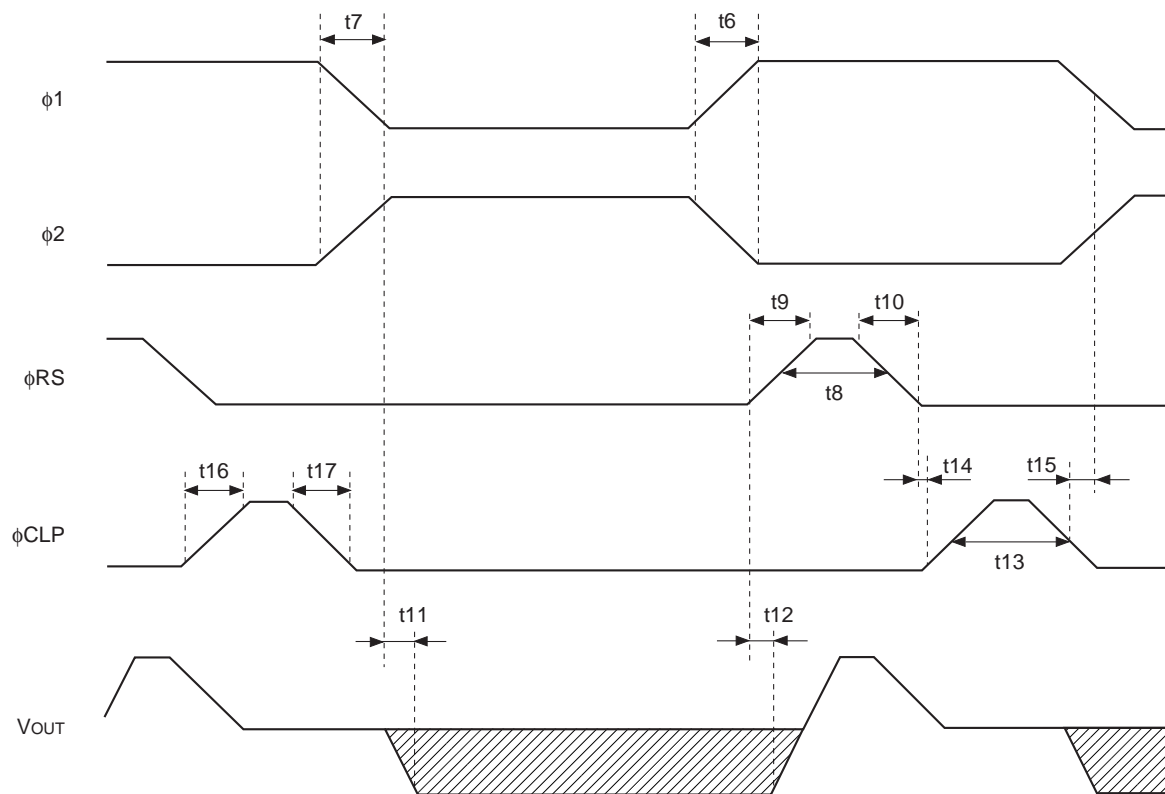


**Note)** The transfer pulses ( $\phi$ 1,  $\phi$ 2) must have more than 10755 cycles.  
 Vout indicates Vout-R, Vout-G, Vout-B.  
 $\phi$ ROG indicates  $\phi$ ROG-R,  $\phi$ ROG-G,  $\phi$ ROG-B.

**Clock Timing Chart 2**



**Clock Timing Chart 3**

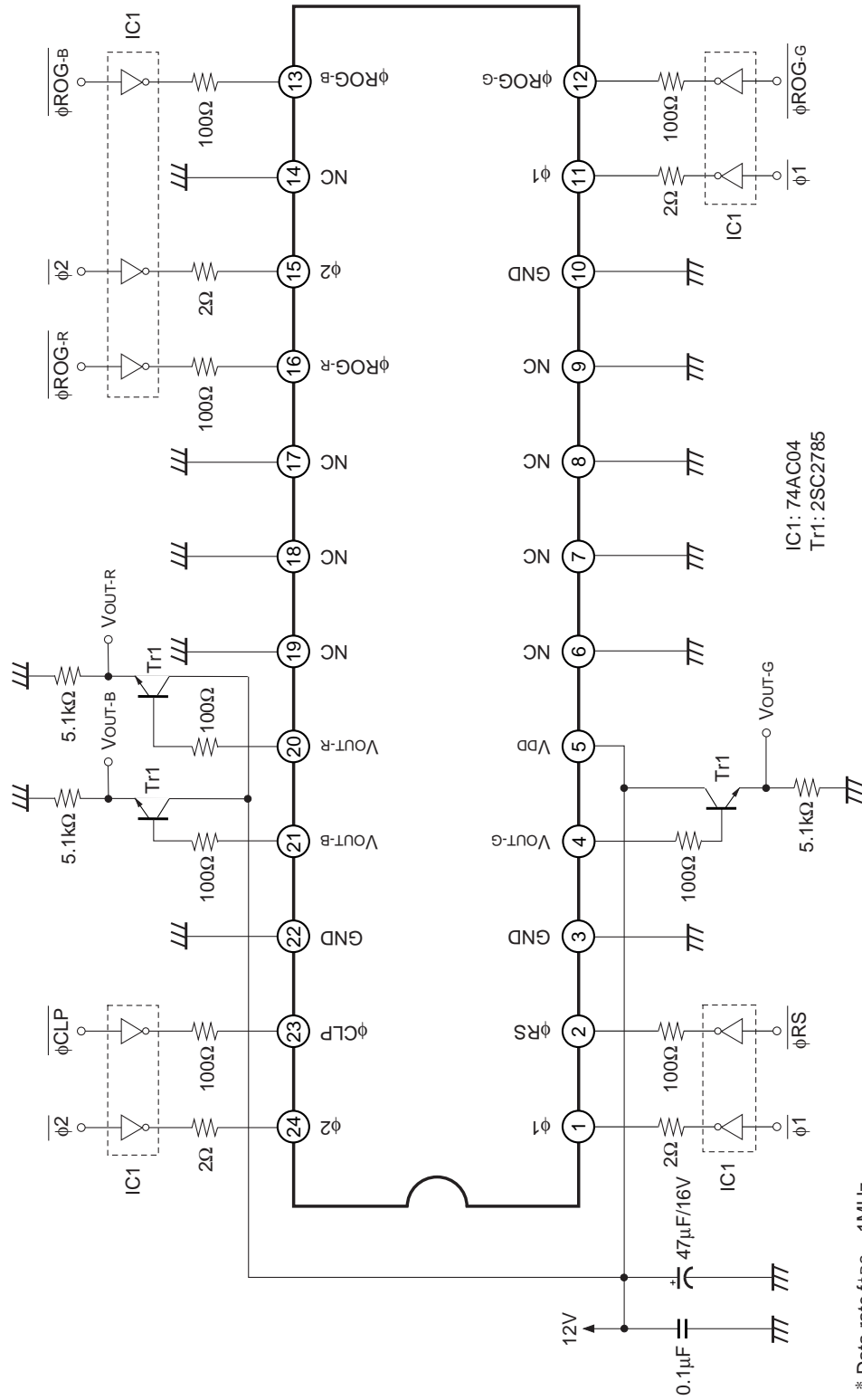


## Clock Pulse Recommended Timing

Item	Symbol	Min.	Typ.	Max.	Unit
$\phi$ ROG, $\phi$ 1 pulse timing	t1	50	100	—	ns
$\phi$ ROG pulse high level period	t2	3	5	—	$\mu$ s
$\phi$ ROG, $\phi$ 1 pulse timing	t3	1	2	—	$\mu$ s
$\phi$ ROG pulse rise time	t4	0	5	—	ns
$\phi$ ROG pulse fall time	t5	0	5	—	ns
$\phi$ 1 pulse rise time/ $\phi$ 2 pulse fall time	t6	0	20	—	ns
$\phi$ 1 pulse fall time/ $\phi$ 2 pulse rise time	t7	0	20	—	ns
$\phi$ RS pulse high level period	t8	30	50* <sup>1</sup>	—	ns
$\phi$ RS pulse rise time	t9	0	20	—	ns
$\phi$ RS pulse fall time	t10	0	20	—	ns
Signal output delay time	t11	—	50	—	ns
	t12	—	20	—	ns
$\phi$ CLP pulse high level period	t13	40	100	—	ns
$\phi$ CLP pulse timing	t14	40	100	—	ns
	t15	10	50	—	ns
$\phi$ CLP pulse rise time	t16	0	20	—	ns
$\phi$ CLP pulse fall time	t17	0	20	—	ns

\*<sup>1</sup> These timing is the recommended condition under  $f_{\phi RS} = 1\text{MHz}$ .

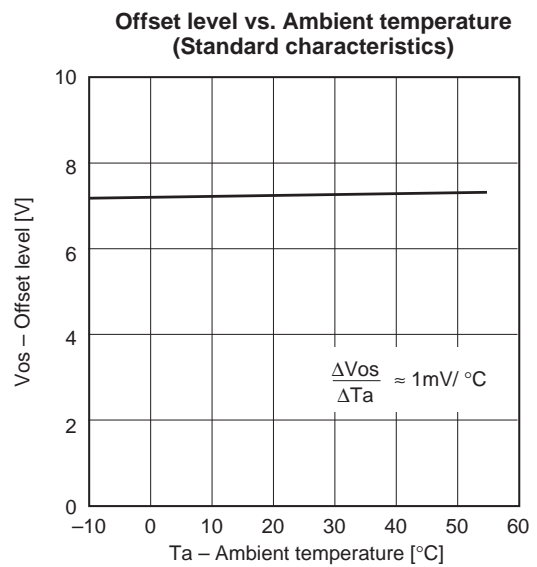
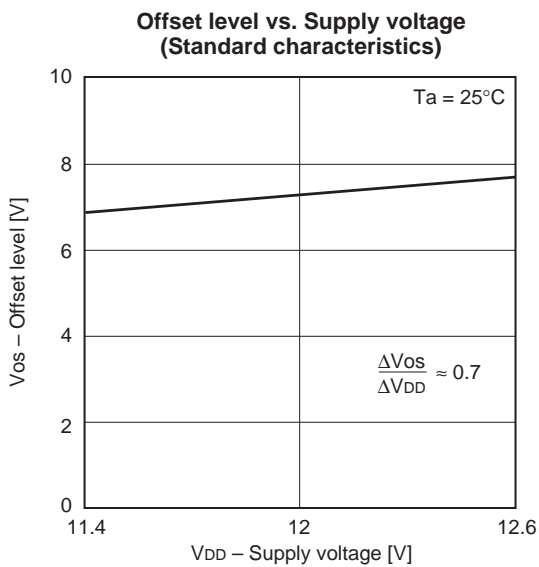
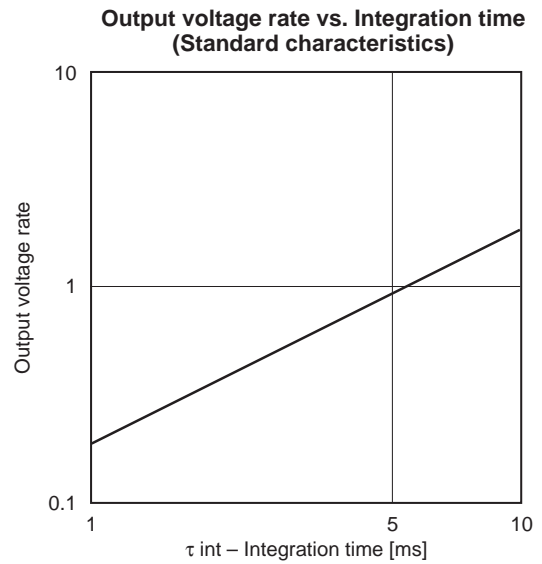
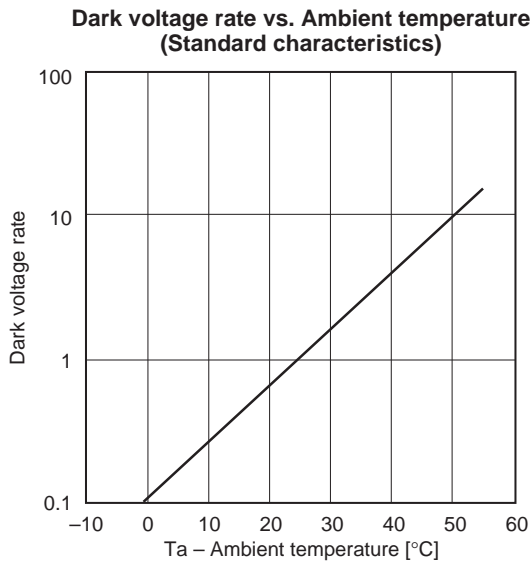
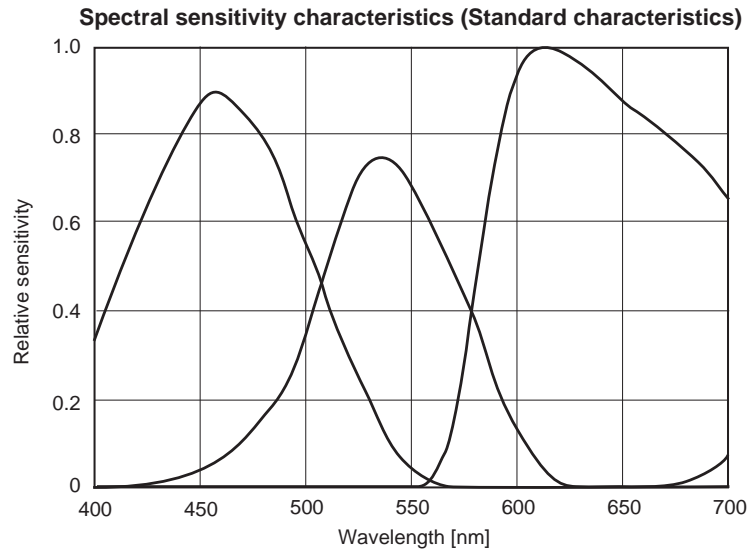
Application Circuit\*



\* Data rate  $f_{\phi RS} = 1\text{MHz}$

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics ( $V_{DD} = 12V$ ,  $T_a = 25^\circ C$ )





## Notes of Handling

### 1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

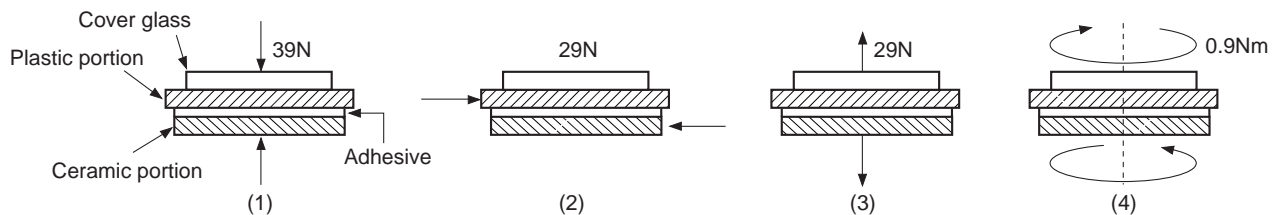
- a) Either handle bare handed or use non chargeable gloves, clothes or material.  
Also use conductive shoes.
- b) When handling directly use an earth band.
- c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
- d) Ionized air is recommended for discharge when handling CCD image sensor.
- e) For the shipment of mounted substrates, use boxes treated for prevention of static charges.

### 2) Notes on Handling CCD Packages

The following points should be observed when handling and installing packages.

a) Remain within the following limits when applying static load to the package:

- (1) Compressive strength: 39N/surface (Do not apply load more than 0.7mm inside the outer perimeter of the glass portion.)
- (2) Shearing strength: 29N/surface
- (3) Tensile strength: 29N/surface
- (4) Torsional strength: 0.9Nm



b) In addition, if a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portion. Therefore, for installation, either use an elastic load, such as a spring plate, or an adhesive.

c) Be aware that any of the following can cause the package to crack or dust to be generated.

- (1) Applying repetitive bending stress to the external leads.
- (2) Applying heat to the external leads for an extended period of time with soldering iron.
- (3) Rapid cooling or heating.
- (4) Prying the plastic portion and ceramic portion away at a support point of the adhesive layer.
- (5) Applying the metal a crash or a rub against the plastic portion.

Note that the preceding notes should also be observed when removing a component from a board after it has already been soldered.

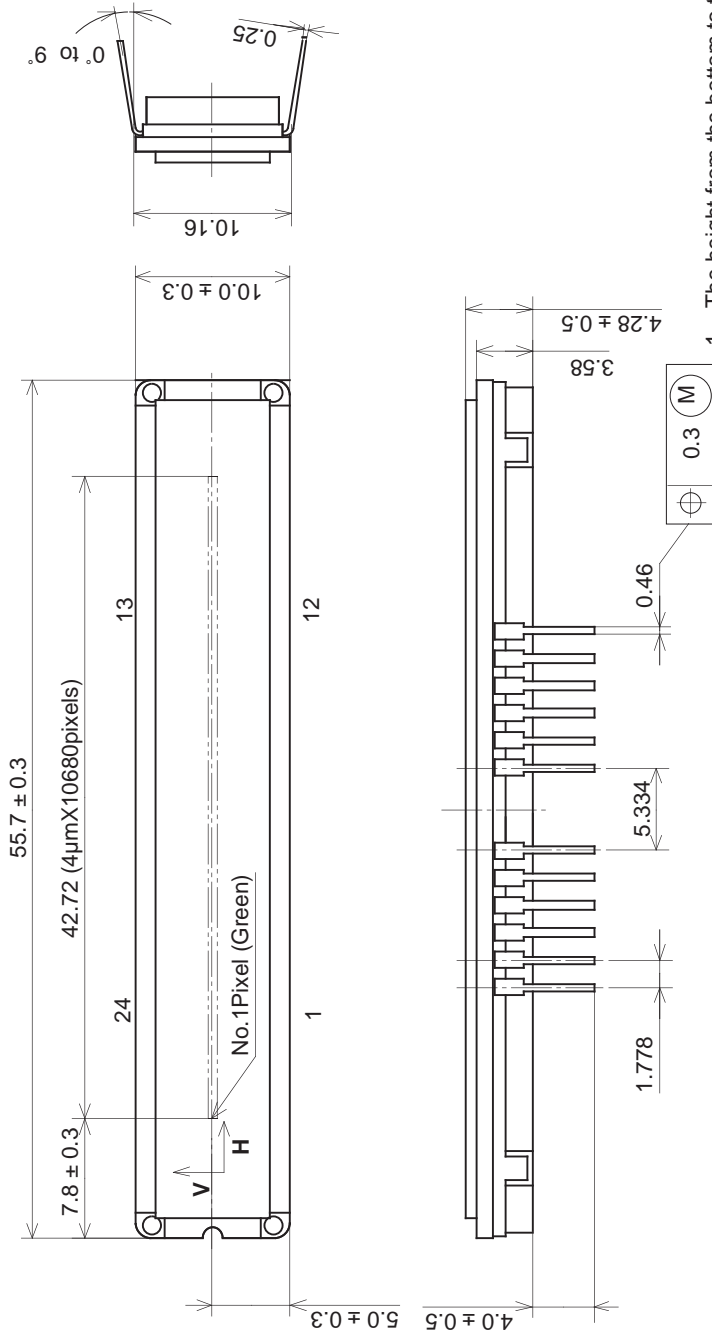
### 3) Soldering

- a) Make sure the package temperature does not exceed 80°C.
- b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
- c) To dismount an imaging device, do not use a solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

- 4) Dust and dirt protection
  - a) Operate in clean environments.
  - b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
  - c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
  - d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
- 5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.
- 6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

Package Outline Unit: mm

24pin SDIP(400mil)



1. The height from the bottom to the sensor surface is 2.38 ± 0.3mm.
2. The thickness of the cover glass is 0.7mm, and the refractive index is 1.5.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Plastic, Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42ALLOY
PACKAGE MASS	5.43g
DRAWING NUMBER	LS-B25-01(E)