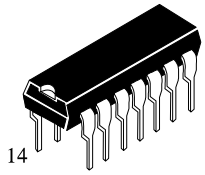
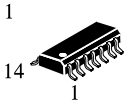
IN7472

AND-Gated J-K Master-Slave Flip-Flops with Reset and Clear



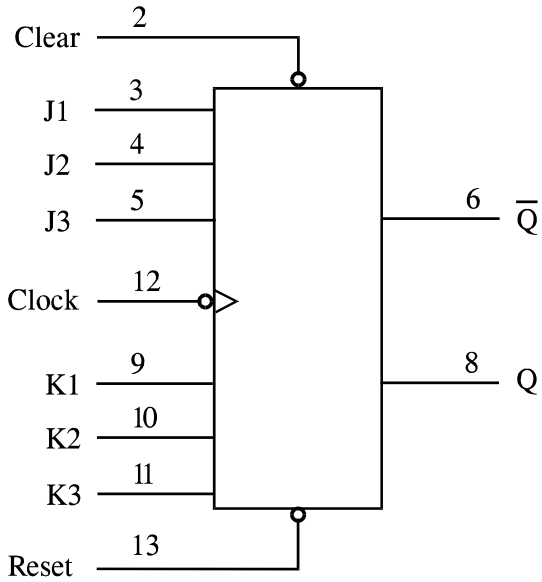
N SUFFIX
PLASTIC



D SUFFIX
SOIC

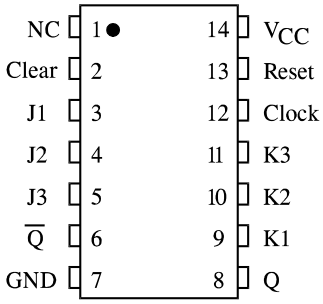
ORDERING INFORMATION
IN7472N Plastic
IN7472D SOIC
T_A = -10° to 70° C for all packages

LOGIC DIAGRAM



PIN 14 =V_{CC}
PIN 7 = GND

PIN ASSIGNMENT



NC - No internal connection

FUNCTION TABLE

Inputs					Output	
Reset	Clear	Clock	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\overline{Q_0}$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

X =don't care
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable; that is, it will not persist whenpreset and clear inputs return to their inactive (high) level.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	7.0	V
V_{IN}	Input Voltage	5.5	V
I_{OL}	Low Level Output Current	16	mA
Tstg	Storage Temperature Range	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		4.75	5.25	V
V_{IH}	High Level Input Voltage		2.0		V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			-400	μA
I_{OL}	Low Level Output Current			16	mA
t_w	Pulse Width	Clock high	20		ns
		Clock low	47		
		Reset or Clear low	25		
t_{su}	Input Setup Time		0↑		ns
t_h	InputHold Time		0↓		ns
f_{max}	Maximum Clock Frequency			15	MHz
T_A	Ambient Temperature Range		-10	+70	°C

↑↓ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

DC ELECTRICAL CHARACTERISTICS over full operating conditions

Symbol	Parameter		Test Conditions	Guaranteed Limit		Unit
				Min	Max	
V_{IK}	Input Clamp Voltage		V_{CC} = min, I_{IN} = -10 mA		-1.5	V
V_{OH}	High Level Output Voltage		V_{CC} = min, I_{OH} =max	2.4		V
V_{OL}	Low Level Output Voltage		V_{CC} = min, I_{OL} =max		0.4	V
I_I	Input Current at Maximum Input Voltage		V_{CC} = max, V_{IN}= 5.5 V		1	mA
I_{IH}	High Level Input Current	D, J, K	V_{CC} = max, V_{IN} = 2.4 V		40	μA
		Clear			80	
		Reset			80	
		Clock			80	
I_{IL}	Low Level Input Current	D, J, K	V_{CC} = max, V_{IN} = 0.4 V		-1.6	mA
		Clear			-3.2	
		Reset			-3.2	
		Clock			-3.2	
I_{OS}*	Short-Circuit Output Current		V_{CC} = max	-18	-55	mA
I_{CC}	Supply Current		V_{CC} = max, See Note 1		20	mA

*Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Note 1: With outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

AC ELECTRICAL CHARACTERISTICS ($T = 25°C$, $V_{CC} = 5.0$ V, $C_L = 15$ pF, $R_L = 390\ \Omega$, Input $t_r = t_f = 10$ ns)

Symbol	Parameter	Min	Max	Unit
t_{PLH}	Propagation Delay Time, Low to High Level Output (from Reset to Q)		25	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output (from Reset to Q)		40	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output (from Clear to Q)		25	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output (from Clear to Q)		40	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output (from Clock to Q or Q)		25	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output (from Clock to Q or Q)		40	ns

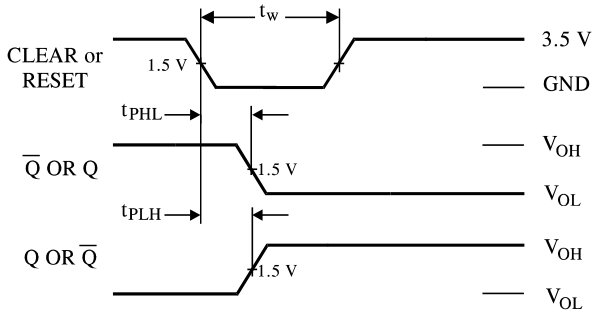


Figure 1. Switching Waveforms

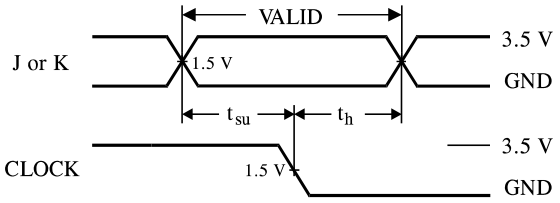
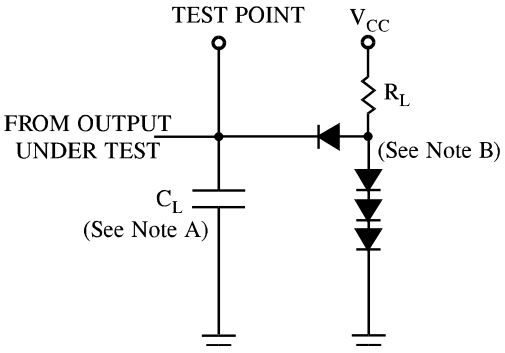


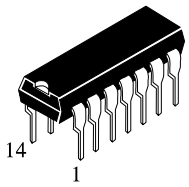
Figure 2. Switching Waveforms

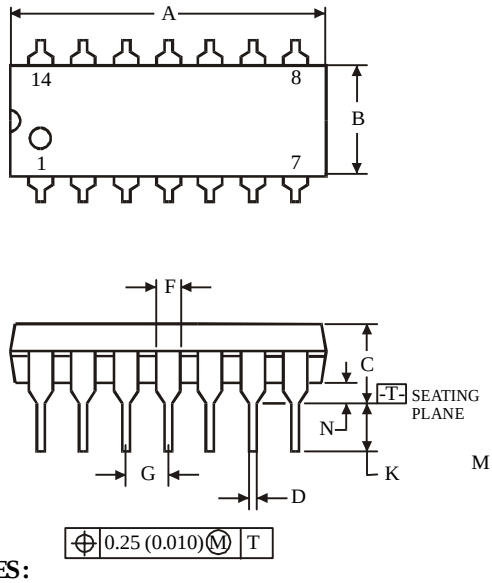


NOTES A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.

Figure 3. Test Circuit

N SUFFIX PLASTIC DIP
(MS - 001AA)



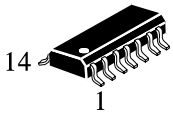


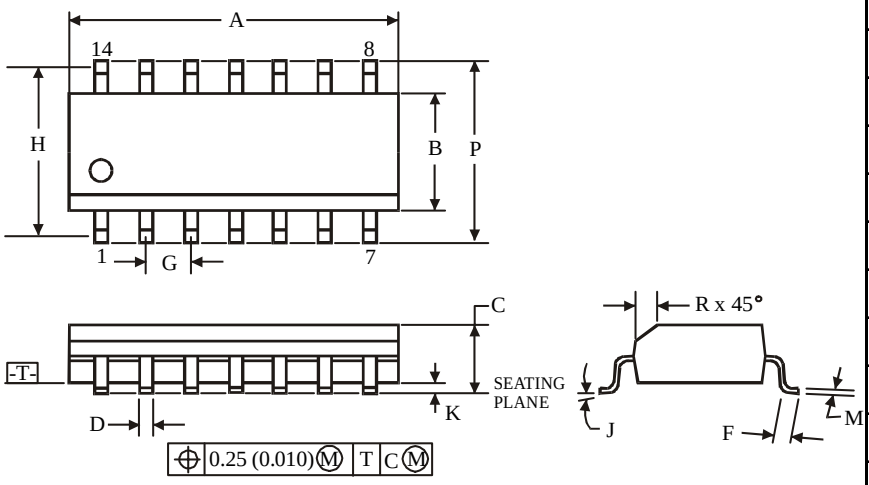
	Dimension, mm	
Symbol	**MIN**	**MAX**
A	18.67	19.69
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

NOTES:

1. Dimensions “A”, “B” do not include mold flash or protrusions.
   Maximum mold flash or protrusions 0.25 mm (0.010) per side.

D SUFFIX SOIC
(MS - 012AB)





	Dimension, mm	
Symbol	**MIN**	**MAX**
A	8.55	8.75
B	3.8	4
C	1.35	1.75
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	5.27	
J	0°	8°
K	0.1	0.25
M	0.19	0.25
P	5.8	6.2
R	0.25	0.5

NOTES:

1. Dimensions A and B do not include mold flash or protrusion.
2. Maximum mold flash or protrusion 0.15 mm (0.006) per side
   for A; for B – 0.25 mm (0.010) per side.