

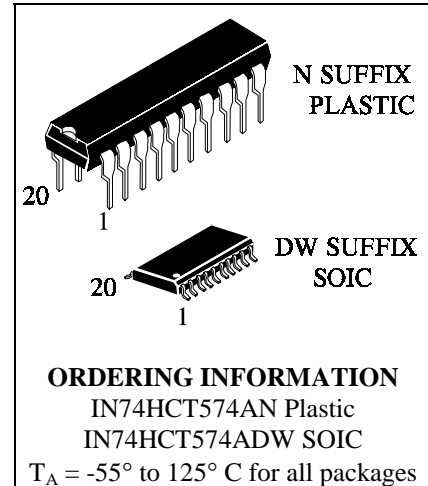
IN74HCT574A

**Octal 3-State
Noninverting D Flip-Flop
High-Performance Silicon-Gate CMOS**

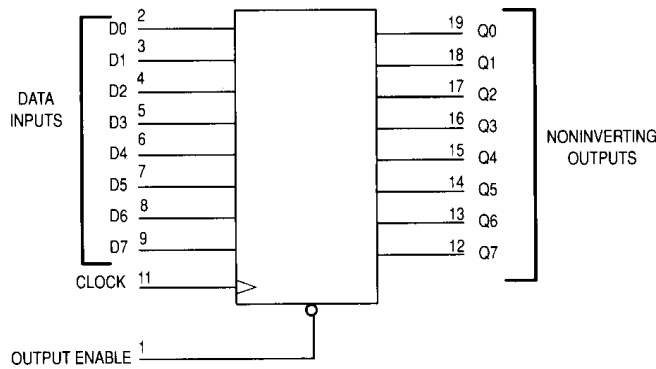
The IN74HCT574A is identical in pinout to the LS/ALS574. This device may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

Data meeting the setup time is clocked to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip-flops, but when Output Enable is high, all device outputs are forced to the high-impedance state; thus, data may be stored even when the outputs are not enabled.

- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μ A



LOGIC DIAGRAM



PIN 20 = V_{CC}
 PIN 10 = GND

PIN ASSIGNMENT

| | | | |
|---------------|----|----|----------|
| OUTPUT ENABLE | 1 | 20 | V_{CC} |
| D0 | 2 | 19 | Q0 |
| D1 | 3 | 18 | Q1 |
| D2 | 4 | 17 | Q2 |
| D3 | 5 | 16 | Q3 |
| D4 | 6 | 15 | Q4 |
| D5 | 7 | 14 | Q5 |
| D6 | 8 | 13 | Q6 |
| D7 | 9 | 12 | Q7 |
| GND | 10 | 11 | CLOCK |

FUNCTION TABLE

| Inputs | | Output | |
|---------------|-------|--------|-----------|
| Output Enable | Clock | D | Q |
| L | | H | H |
| L | | L | L |
| L | L,H, | X | no change |
| H | X | X | Z |

X = don't care
 Z = high impedance

MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|------------------|--|------------------------------|------|
| V _{CC} | DC Supply Voltage (Referenced to GND) | -0.5 to +7.0 | V |
| V _{IN} | DC Input Voltage (Referenced to GND) | -1.5 to V _{CC} +1.5 | V |
| V _{OUT} | DC Output Voltage (Referenced to GND) | -0.5 to V _{CC} +0.5 | V |
| I _{IN} | DC Input Current, per Pin | ±20 | mA |
| I _{OUT} | DC Output Current, per Pin | ±35 | mA |
| I _{CC} | DC Supply Current, V _{CC} and GND Pins | ±75 | mA |
| P _D | Power Dissipation in Still Air, Plastic DIP+ SOIC Package+ | 750 500 | mW |
| T _{stg} | Storage Temperature | -65 to +150 | °C |
| T _L | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) | 260 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|------------------------------------|--|-----|-----------------|------|
| V _{CC} | DC Supply Voltage (Referenced to GND) | 4.5 | 5.5 | V |
| V _{IN} , V _{OUT} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V _{CC} | V |
| T _A | Operating Temperature, All Package Types | -55 | +125 | °C |
| t _r , t _f | Input Rise and Fall Time (Figure 1) | 0 | 500 | ns |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limit | | | Unit |
|------------------|--|--|----------------------|----------------------|---------------|------------|------|
| | | | | 25 °C to -55°C | ≤85 °C | ≤125 °C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA | 4.5 | 2.0 | 2.0 | 2.0 | V |
| | | | 5.5 | 2.0 | 2.0 | 2.0 | |
| V _{IL} | Maximum Low - Level Input Voltage | V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA | 4.5 | 0.8 | 0.8 | 0.8 | V |
| | | | 5.5 | 0.8 | 0.8 | 0.8 | |
| V _{OH} | Minimum High-Level Output Voltage | V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA | 4.5 | 4.4 | 4.4 | 4.4 | V |
| | | V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 6.0 mA | 5.5 | 5.4 | 5.4 | 5.4 | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{IN} = V _{IL} or V _{IH} I _{OUT} ≤ 20 μA | 4.5 | 0.1 | 0.1 | 0.1 | V |
| | | V _{IN} = V _{IL} or V _{IH} I _{OUT} ≤ 6.0 mA | 5.5 | 0.1 | 0.1 | 0.1 | |
| I _{IN} | Maximum Input Leakage Current | V _{IN} =V _{CC} or GND | 4.5 | ±0.1 | ±1.0 | ±1.0 | μA |
| | | | 5.5 | ±0.1 | ±1.0 | ±1.0 | |
| I _{OZ} | Maximum Three State Leakage Current | Output in High-Impedance State V _{IN} =V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND | 5.5 | ±0.5 | ±5.0 | ±10 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{IN} =V _{CC} or GND I _{OUT} =0μA | 5.5 | 4.0 | 40 | 160 | μA |
| ΔI _{CC} | Additional Quiescent Supply Current | V _{IN} =2.4 V, Any One Input V _{IN} =V _{CC} or GND, Other Inputs I _{OUT} =0μA | | ≥-55°C | 25°C to 125°C | | mA |
| | | | 5.5 | 2.9 | 2.4 | | |

AC ELECTRICAL CHARACTERISTICS($V_{CC}=5.0\text{ V} \pm 10\%$, $C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

| Symbol | Parameter | Guaranteed Limit | | | Unit |
|-----------------------|---|------------------|-------|--------|------|
| | | 25 °C to -55°C | ≤85°C | ≤125°C | |
| f_{max} | Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4) | 30 | 24 | 20 | MHz |
| t_{PLH} , t_{PHL} | Maximum Propagation Delay, Clock to Q (Figures 1 and 4) | 30 | 38 | 45 | ns |
| t_{PLZ} , t_{PHZ} | Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5) | 28 | 35 | 42 | ns |
| t_{PZH} , t_{PZL} | Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5) | 28 | 35 | 42 | ns |
| t_{TLH} , t_{THL} | Maximum Output Transition Time, Any Output (Figures 1 and 4) | 12 | 15 | 18 | ns |
| C_{IN} | Maximum Input Capacitance | 10 | 10 | 10 | pF |
| C_{OUT} | Maximum Three-State Output Capacitance (Output in High-Impedance State) | 15 | 15 | 15 | pF |

| | | | | | |
|----------|--|--------------------------------------|--|--|----|
| C_{PD} | Power Dissipation Capacitance (Per Flip-Flop) | Typical @25°C, $V_{CC}=5.0\text{ V}$ | | | pF |
| | Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$ | 58 | | | |

TIMING REQUIREMENTS ($V_{CC}=5.0\text{ V} \pm 10\%$, $C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

| Symbol | Parameter | Guaranteed Limit | | | Unit |
|---------------|--|------------------|-------|--------|------|
| | | 25 °C to -55°C | ≤85°C | ≤125°C | |
| t_{SU} | Minimum Setup Time, Data to Clock (Figure 3) | 10 | 13 | 15 | ns |
| t_h | Minimum Hold Time, Clock to Data (Figure 3) | 5 | 5 | 5 | ns |
| t_w | Minimum Pulse Width, Clock (Figure 1) | 15 | 19 | 22 | ns |
| t_r , t_f | Maximum Input Rise and Fall Times (Figure 1) | 500 | 500 | 500 | ns |

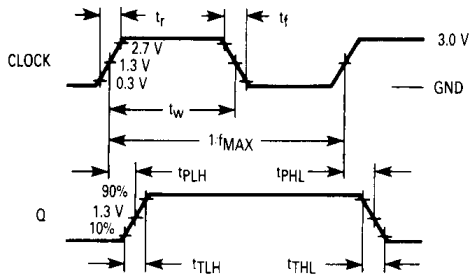


Figure 1. Switching Waveforms

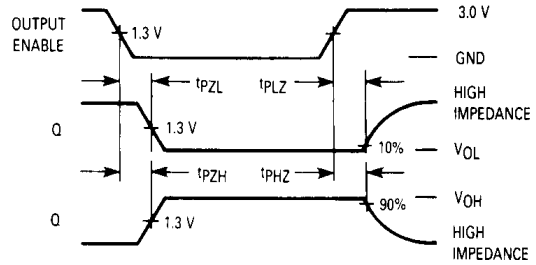


Figure 2. Switching Waveforms

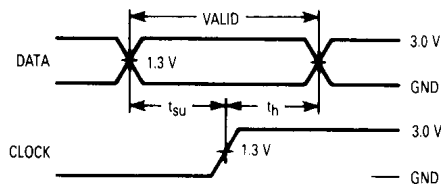
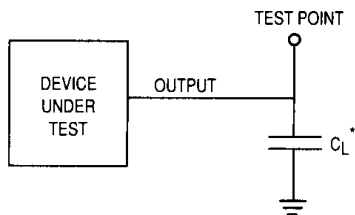
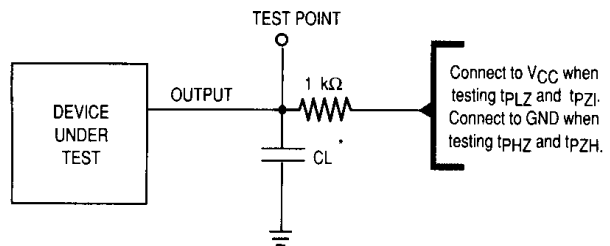


Figure 3. Switching Waveforms



* Includes all probe and jig capacitance

Figure 4. Test Circuit



*Includes all probe and jig capacitance

Figure 5. Test Circuit

EXPANDED LOGIC DIAGRAM

