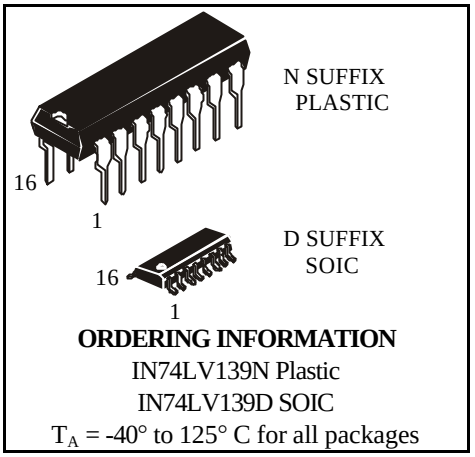
IN74LV139

Dual 2-to-4 line decoder/demultiplexer; inverting



ORDERING INFORMATION

IN74LV139N Plastic

IN74LV139D SOIC

T_A = -40° to 125° C for all packages

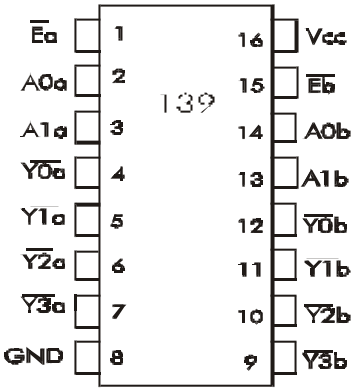
The IN74LV139 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HCT139.

The74LV139 is dual 2-to-4 line decoder/demultiplexer . This device has two independent decoders, each accepting two binary weighted inputs (A0a,A0b and A1a,A1b) and providing four mutually exclusive active LOW outputs (nY0 to nY3). Each decoder has an active LOW enable input (nE)

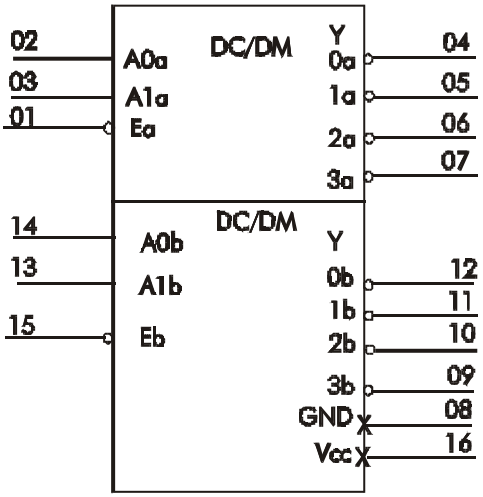
When $n\overline{E}$ is HIGH, every output is forced HIGH. The enable can be used as the data input for a 1-to-4 demultiplexer application.

- Optimized for Low Voltage applications:1.2 to 3.6 V
- Demultiplexing capability
- Two independent 2-to-4 decoders
- Multifunction capability
- Active LOW mutually exclusive outputs
- Output capability: standard

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 16 =V_{CC}

PIN 8 = GND

FUNCTION TABLE

Inputs			Outputs
$\overline{E}$	A1	A0	Y0 Y1 Y2 Y3
H	X	X	H H H H
L	L	L	L H H H
L	L	H	H L H H
L	H	L	H H L H
L	H	H	H H H L

H = high level (steady state)

L = low level (steady state)

X = don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Conditions	Unit
V_{CC}	DC supply voltage	-0.5 to +7.0		V
I_{IK}	DC input diode current	±20	V_I< - 0.5 or V_I> Vcc+0.5V	mA
I_{OK}	DC output diode current	±50	V_O< - 0.5 or V_O> Vcc+0.5V	mA
I_O	DC output source or sink current	±25	-0.5Â<Vo<Vcc+0.5B	mA
I_{CC}	DC V_{CC} or GND current for types with standard outputs	±50		mA
Tstg	Storage Temperature	-65 to +150		°C
P_D	Power Dissipation per package Plastic DIP+ SOIC Package+	 750 500		mW
T_L	Lead temperature, 1.5 mm from Case for 4 seconds (Plastic DIP), 0.3 mm (SOIC Package)	260		°C

*
Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C
SOIC Package: : - 8 mW/°C from 70° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC supply voltage		1.2	5.5	V
V_I	DC input voltage,		0	V_{CC}	V
V_O	DC output voltage		0	V_{CC}	V
T_A	Operating ambient temperature range in free air		-40	+125	°C
t_r, t_f	Input rise and fall times except for Schmitt-trigger inputs	Vcc= 1.0 ? 2.0Â Vcc= 2.0 ? 2.7Â Vcc= 2.7 ? 3.6Â Vcc= 3.6 ? 5.5Â	0 0 0	500 200 100 50	ns/B

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC}, Â	Guaranteed Limit						Unit
				25°C		î ò -40°C to 85°C		î ò -40°C to 125°C		
				min	max	min	max	min	max	
V_{IH}	High-level input voltage		1.2 2.0 2.7 to 3.6 4.5 to 5.5	0.9 1.4 2.0 0.7 Vcc	- - - -	0.9 1.4 2.0 0.7 Vcc	- - - -	0.9 1.4 2.0 0.7 Vcc	- - - -	Â
V_{IL}	Low -level input voltage		1.2 2.0 2.7 to 3.6 4.5 to 5.5	- - - -	0.3 0.6 0.8 0.3 Vcc	- - - -	0.3 0.6 0.8 0.3 Vcc	- - - -	0.3 0.6 0.8 0.3 Vcc	Â
V_{OH}	High-level output voltage	$-I_0$=100µA V_{IH} or V_{IL}	1.2 2.0 2.7 3.0 3.6 4.5 5.5	- 1.85 2.55 2.85 3.45 4.35 5.35	- - - - - - -	- 1.8 2.5 2.8 3.4 4.3 5.3	- - - - - - -	- 1.8 2.5 2.8 3.4 4.3 5.3	- - - - - - -	Â
		V_{IH} or V_{IL} $-I_{O=}$6.0 mA $-I_{O=}$12.0 mA	3.0 4.5	2.48 3.70	-	2.40 3.60	-	2.20 3.50	-	B
V_{OL}	Low-level output voltage	V_{IH} or V_{IL} I_0=100µA	1.2 2.0 3.0	- - - -	0.15 0.15 0.15	- - - -	0.2 0.2 0.2	- - - -	0.2 0.2 0.2	B
		V_{IH} or V_{IL} $I_{O=}$6.0 mA $I_{O=}$12.0 mA	3.0 4.5	-	0.33 0.40	-	0.40 0.55	-	0.50 0.65	B
I_I	Input leakage current	V_{CC} or GND	5.5	-	±0.1	-	±1.0	-	±1.0	ì êÀ
I_{CC}	Quiescent supply current	V_{CC} or GND I_O=0	5.5	-	8.0	-	80	-	160	ì êÀ

AC ELECTRICAL CHARACTERISTICS (C_L=50 pF, $t_{LH} = t_{HL}$ = 2.5 nc, V_{IL}=0B, $V_{IH}=V_{CC}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit						Unit
			25°C		î ò -40°C to 85°C		î ò -40°C to 125°C		
			min	max	min	max	min	max	
t_{PLH}, t_{PHL}	Propagation delay, input A to output Y (Figures 1)	1.2 2.0 2.7 3.0 4.5	-	140 27 20 16 13	-	140 31 23 18 15	-	140 39 29 23 19	ns
t_{PLH}, t_{PHL}	Propagation delay , E to output Y (Figures 2)	1.2 2.0 2.7 3.0 4.5	-	120 22 16 13 10	-	120 27 20 16 13	-	120 34 25 20 16	ns
C_I	Input capacitance	5.0 Ò=+25 î Ñ		7.0					pF

C_{PD}	Power dissipation capacitance (per enabled output) Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	Typical @25°C,V_{CC}=5.5 V 84*	pF

* - Power dissipation capacitance per multiplexer

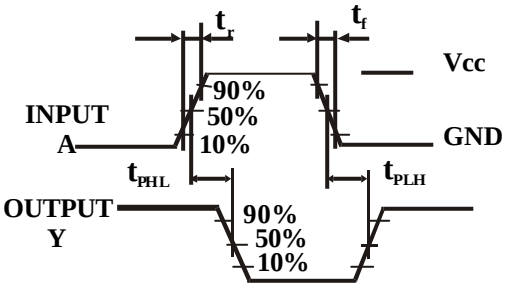


Figure 1. Switching Waveforms

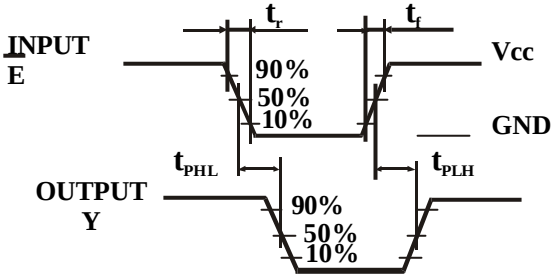
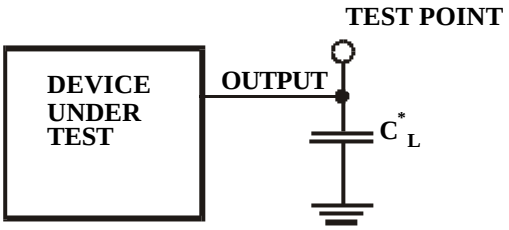


Figure 2. Switching Waveforms

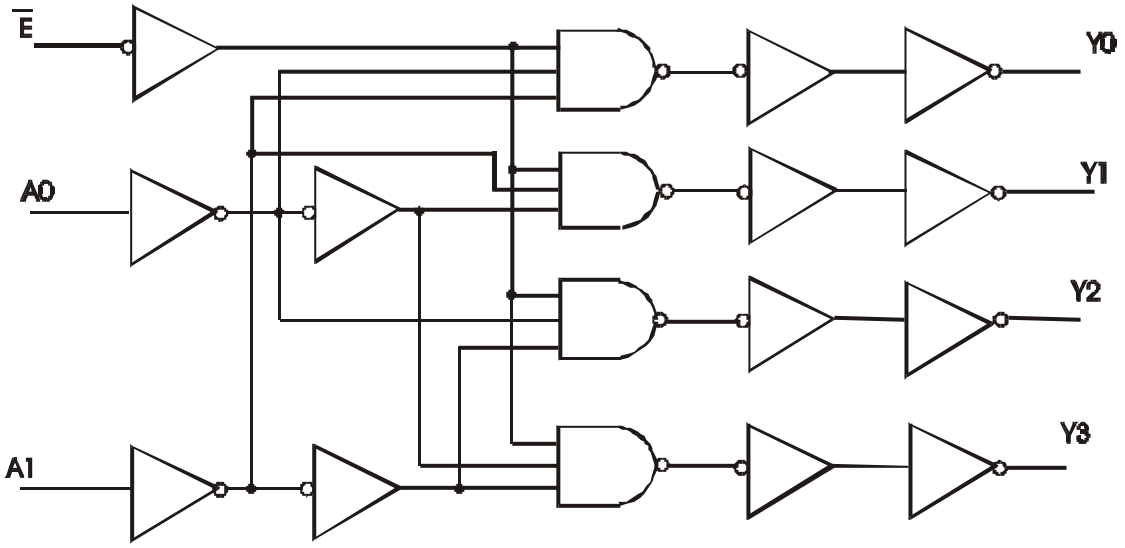


*** Includes all prode and jig capacitance**

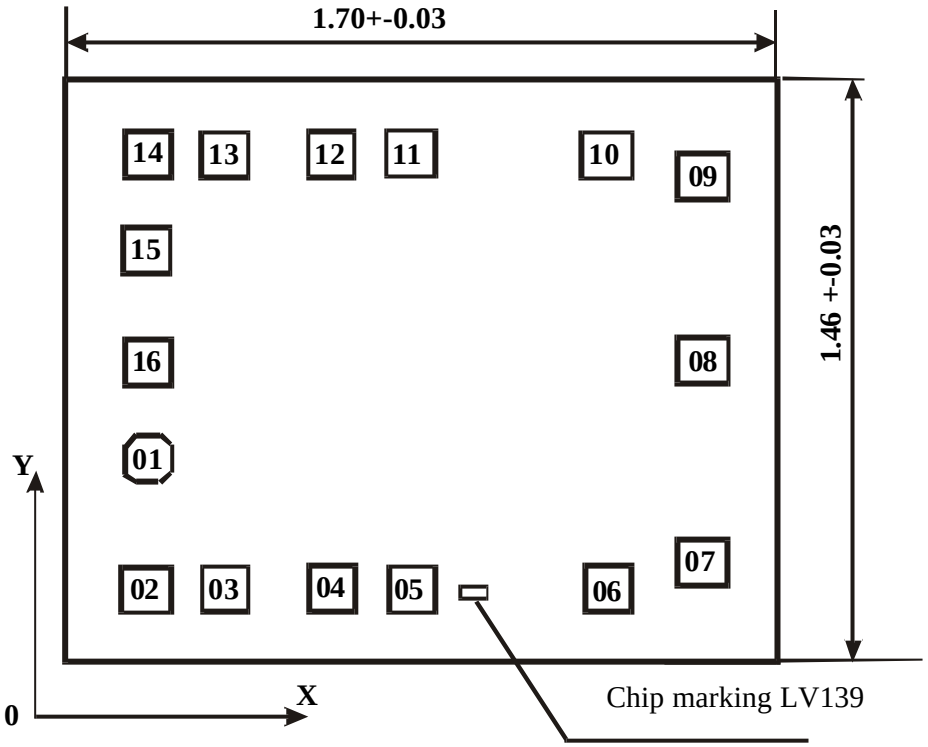
Figure 3. Test Circuit

EXPANDED LOGIC DIAGRAM

(1/2 of Device)



CHIP PAD DIAGRAM



Location of marking (mm): left lower corner x = 0.950, y = 0.130;
Thickness of chip: 0.46 ± 0.02 mm

PAD LOCATION

Pad No.	Pad Name	X	Y	Pad size (mm)
01	$\overline{E}$a	0.1245	0.4625	0.100 x 0.100
02	A0a	0.1245	0.1290	0.100 x 0.100
03	A1a	0.2920	0.1290	0.100 x 0.100
04	$\overline{Y0}$a	0.5480	0.1290	0.100 x 0.100
05	$\overline{Y1}$a	0.7520	0.1290	0.100 x 0.100
06	$\overline{Y2}$a	1.2830	0.1290	0.100 x 0.100
07	Y3a	1.4845	0.1845	0.100 x 0.100
08	GND	1.4840	0.6770	0.100 x 0.100
09	Y3b	1.4845	1.1720	0.100 x 0.100
10	Y2b	1.2830	1.2265	0.100 x 0.100
11	Y1b	0.7520	1.2265	0.100 x 0.100
12	Y0b	0.5480	1.2265	0.100 x 0.100
13	A1b	0.2920	1.2265	0.100 x 0.100
14	A0b	0.1245	1.2265	0.100 x 0.100
15	Eb	0.1245	0.8930	0.100 x 0.100
16	Vcc	0.1245	0.6650	0.100 x 0.100

∗ Note: Pad location is given as per passivation layer