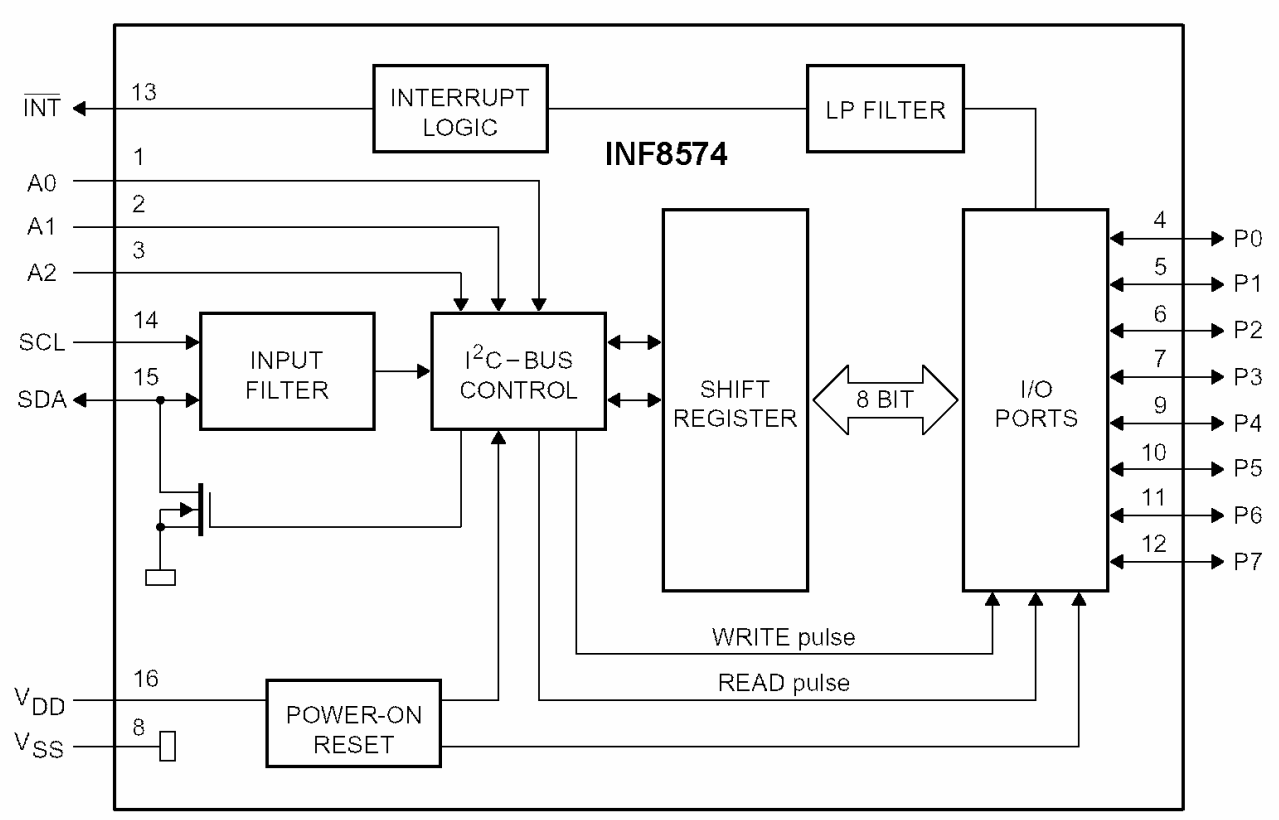
GENERAL DESCRIPTION

The INF8574 is a silicon CMOS circuit. It provides general purpose remote I/O expansion for most microcontroller families via the two-line bidirectional bus (I^2C).
The device consists of an 8-bit quasi-bidirectional Port and an I^2C interface. The INF8574 has a low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^2C-bus. This means that the INF8574 can remain a simple slave device.

FEATURES

- Operating supply voltage 2.5 to 6 V
- Low standby current consumption of 10 A maximum
- I^2C to parallel port expander
- Open-drain interrupt output
- 8-bit remote I/O Port for the I^2C-bus
- Compatible with most microcontrollers
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with INF8574A)
- DIP16, space-saving SO16 or SSOP20 package.

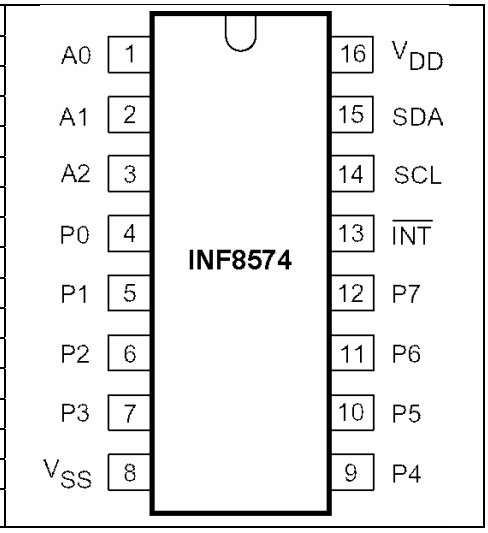
BLOCK DIAGRAM



INTEGRAL

PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	address input 0
A1	2	address input 1
A2	3	address input 2
P0	4	quasi-bidirectional I/O Port 0
P1	5	quasi-bidirectional I/O Port 1
P2	6	quasi-bidirectional I/O Port 2
P3	7	quasi-bidirectional I/O Port 3
V_{SS}	8	supply ground
P4	9	quasi-bidirectional I/O Port 4
P5	10	quasi-bidirectional I/O Port 5
P6	11	quasi-bidirectional I/O Port 6
P7	12	quasi-bidirectional I/O Port 7
INT	13	interrupt output (active LOW)
SCL	14	serial clock line
SDA	15	serial data line
V_{DD}	16	supply voltage

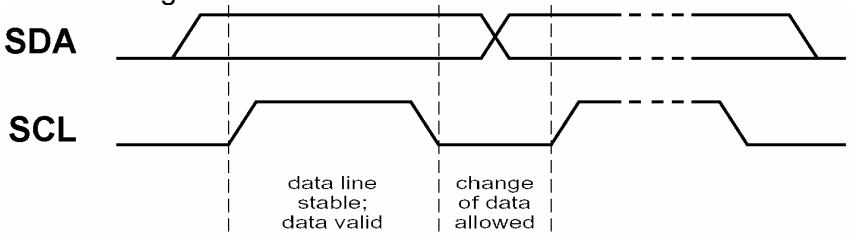


CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

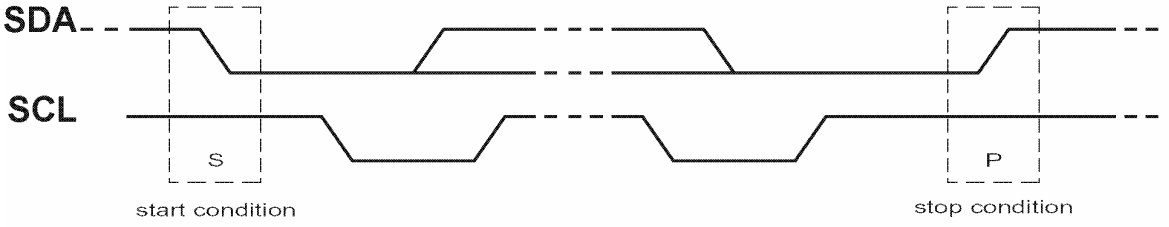
Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals



Bit transfer.

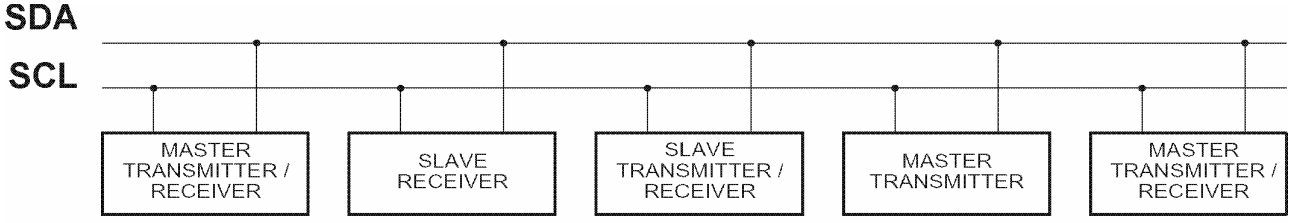
Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).



Definition of start and stop conditions.

System configuration

A device generating a message is a ‘transmitter’, a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’.



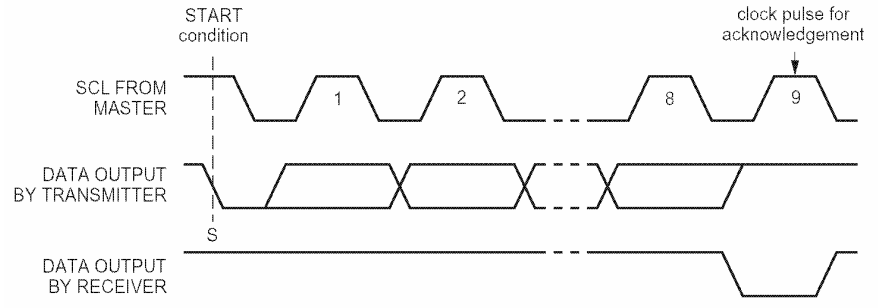
System configuration.

Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

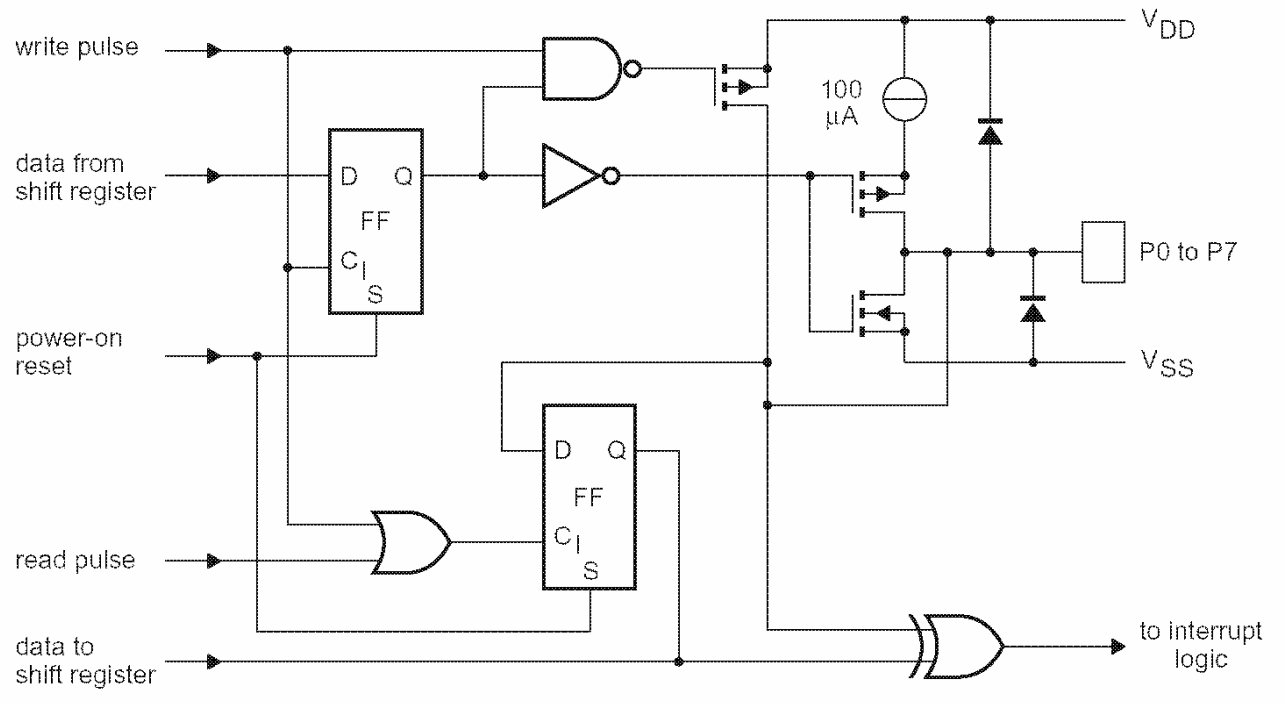
A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.



Acknowledgement on the I^2C-bus.

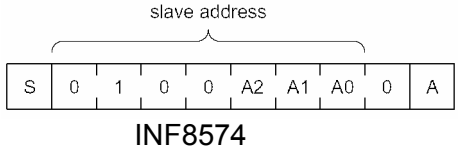
FUNCTIONAL DESCRIPTION



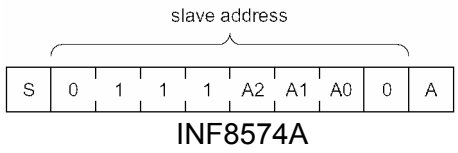
Simplified schematic diagram of each Port.

Addressing

For addressing.



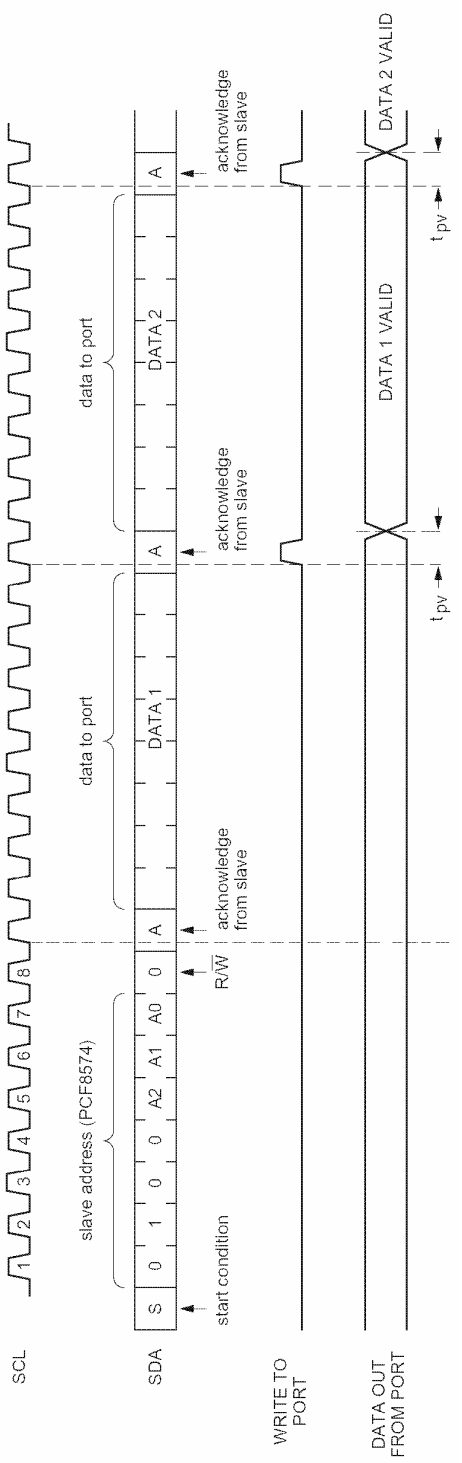
INF8574



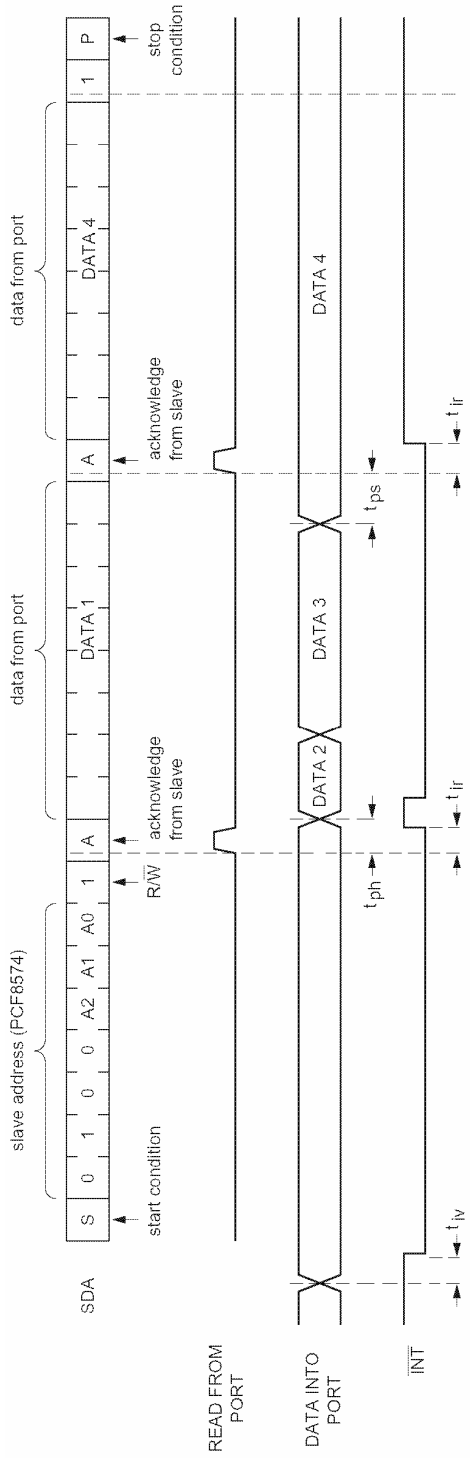
INF8574A

Slave addresses.

Each bit of the INF8574 I/O Port can be independently used as an input or output. Input data is transferred from the Port to the microcontroller by the READ mode (see Fig.11). Output data is transmitted to the Port by the WRITE mode (see Fig.10).



WRITE mode (output Port).



A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

READ mode (input Port).

Interrupt

The INF8574 provides an open drain output (INT) which can be fed to a corresponding input of the microcontroller. This gives these chips a type of master function which can initiate an action elsewhere in the system.

An interrupt is generated by any rising or falling edge of the Port inputs in the input mode. After time t_{iv} the signal INT is valid.

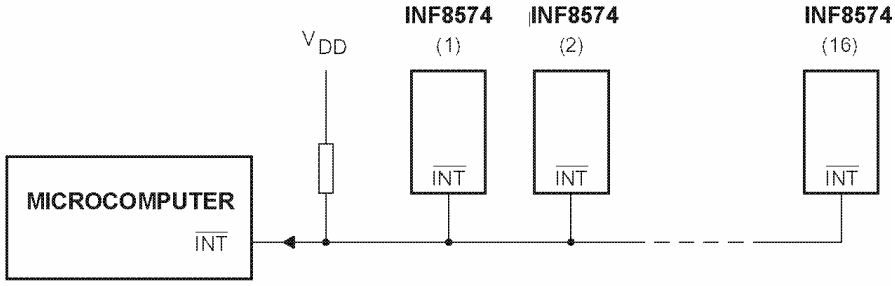
Resetting and reactivating the interrupt circuit is achieved when data on the Port is changed to the original setting or data is read from or written to the Port which has generated the interrupt.

Resetting occurs as follows:
- In the READ mode at the acknowledge bit after the rising edge of the SCL signal.
- In the WRITE mode at the acknowledge bit after the HIGH-to-LOW transition of the SCL signal.
- Interrupts which occur during the acknowledge clock pulse may be lost (or very short) due to the resetting of the interrupt during this pulse.

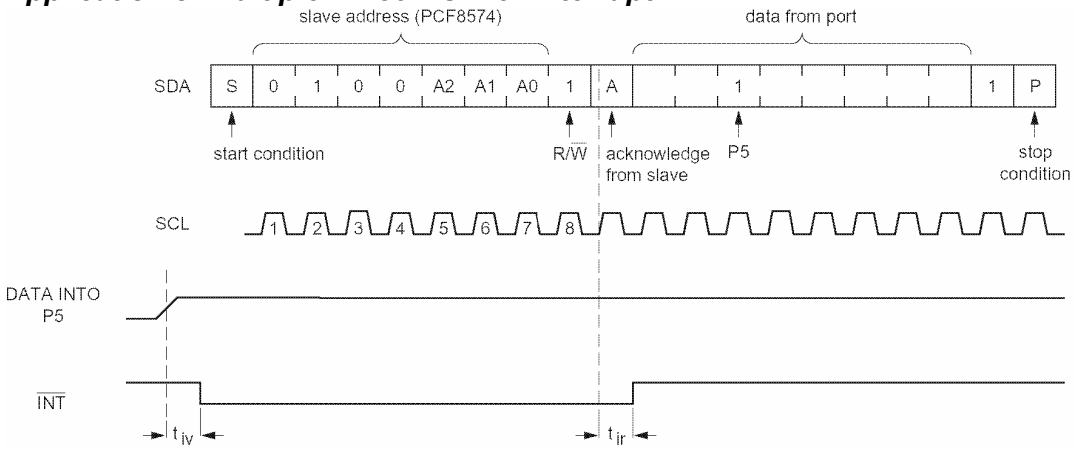
Each change of the Ports after the resettings will be detected and after the next rising clock edge, will be transmitted as INT. Reading from or writing to another device does not affect the interrupt circuit.

Quasi-bidirectional I/O Ports

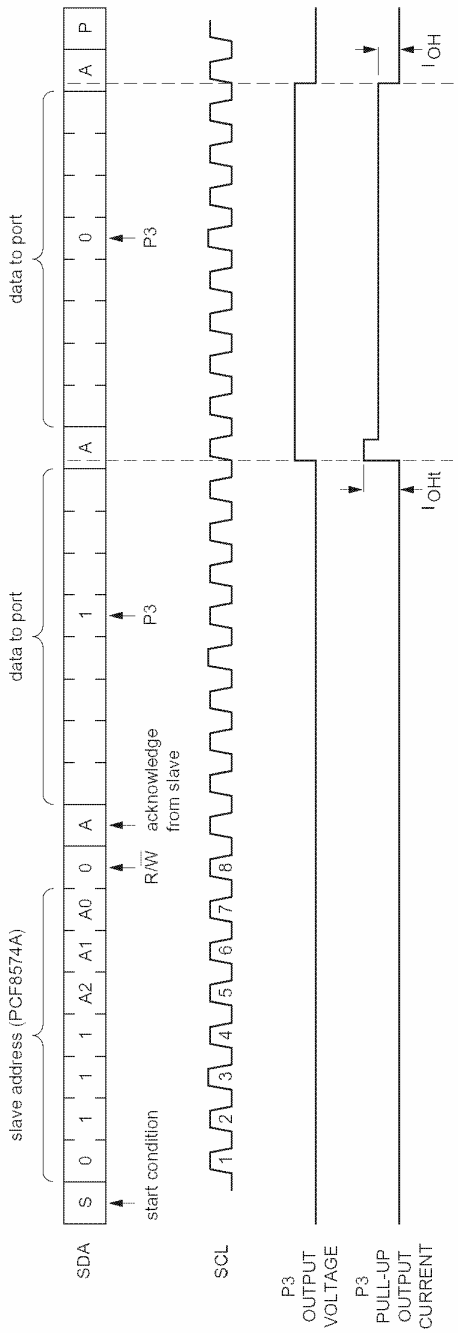
A quasi-bidirectional Port can be used as an input or output without the use of a control signal for data direction. At power-on the Ports are HIGH. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The Ports should be HIGH before being used as inputs.



Application of multiple INF8574s with interrupt.



Interrupt generated by a change of input to Port P5.



Transient pull-up current I_{OHt} while P3 changes from LOW-to-HIGH and back to LOW.

LIMITING VALUES

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	-0.5	+7.0	V
V_I	input voltage	V_{SS} - 0.5	V_{DD} + 0.5	V
I_I	DC input current	-	±20	mA
I_O	DC output current	-	±25	mA
I_{DD}	supply current	-	±100	mA
I_{SS}	supply current	-	±100	mA
P_{tot}	total power dissipation	-	400	mW
P_O	power dissipation per output	-	100	mW
T_{stg}	storage temperature	-65	+150	°C
T_{amb}	operating ambient temperature	-40	+85	°C

DC CHARACTERISTICS V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} =40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.5		6.0	V
I_{DD}	supply current	operating mode; V_{DD} = 6 V; no load; V_I = V_{DD} or V_{SS}; f_{SCL} = 100 kHz		40	100	µA
I_{stb}	standby current	standby mode; V_{DD} = 6 V; no load; V_I = V_{DD} or V_{SS}		2.5	10	µA
V_{POR}	power-on reset voltage	V_{DD} = 6 V; no load; V_I = V_{DD} or V_{SS}; note 1		1.3	2.4	V
Input SCL; input/output SDA						
V_{IL}	LOW level input voltage		-0.5		+0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}		V_{DD} + 0.5	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3			mA
$\|I_L\|$	leakage current	V_I = V_{DD} or V_{SS}			1	µA
C_I	input capacitance	V_I = V_{SS}			7	pF
I/O Ports						
V_{IL}	LOW level input voltage		-0.5		+0.3V_{DD}	V
V_{IH}	HIGH level input voltage		-0.7V_{DD}		V_{DD} + 0.5	V
$I_{IHL(max)}$	maximum allowed input current through protection diode	$V_I \geq V_{DD}$ or $V_I \leq V_{SS}$			±400	µA
I_{OL}	LOW level output current	V_{OL} = 1 V; V_{DD} = 5 V	10	25		mA
I_{OH}	HIGH level output current	V_{OH} = V_{SS}	30		300	µA
I_{OHt}	transient pull-up current	HIGH during acknowledge (see Fig.14); V_{OH} = V_{SS}; V_{DD} = 2.5 V		1		mA
C_I	input capacitance				10	pF
C_O	output capacitance				10	pF
Port timing C_L ≤100 pF						
t_{pv}	output data valid				4	µs
t_{su}	input data set-up time		0			µs
t_h	input data hold time		4			µs
Interrupt INT						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	1.6			mA
$\|I_L\|$	leakage current	V_I = V_{DD} or V_{SS}			1	µA
Timing; C_L ≤100 pF						
t_{iv}	input data valid time				4	µs
t_{ir}	reset delay time				4	µs
Select inputs A0 to A2						
V_{IL}	LOW level input voltage		-0.5		+0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}		V_{DD} + 0.5	V
$\|I_{LI}\|$	input leakage current	pin at V_{DD} or V_{SS}			250	nA

Note

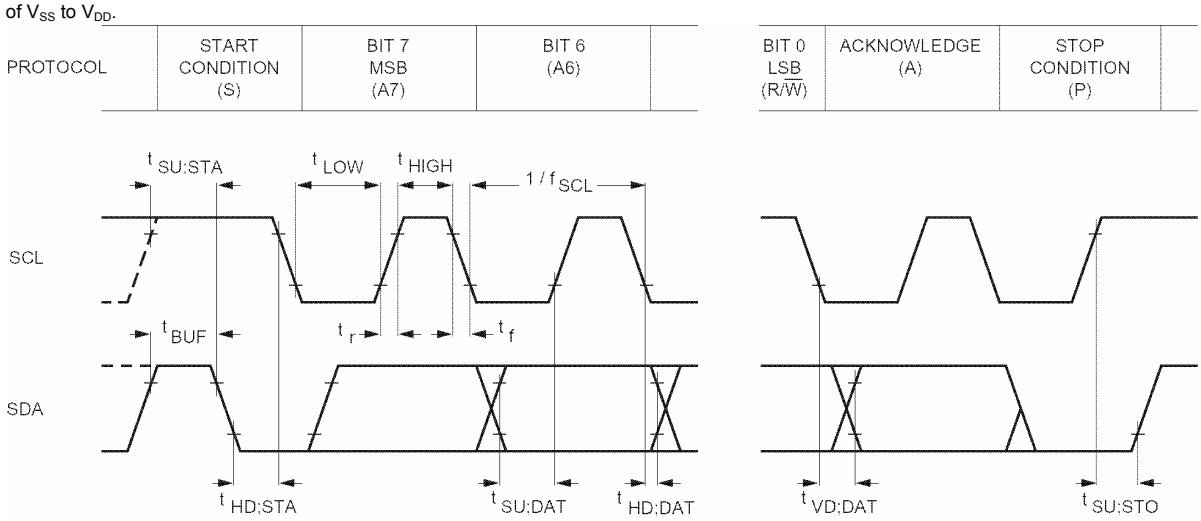
1. The power-on reset circuit resets the I^2C-bus logic with V_{DD} < V_{POR} and sets all Ports to logic 1 (with current source to V_{DD}).

I²C-BUS TIMING CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
I²C-BUS TIMING					
f_{SCL}	SCL clock frequency			100	kHz
t_{SW}	tolerable spike width on bus			100	ns
t_{BUF}	bus free time	4.7			µs
$t_{SU;STA}$	start condition set-up time	4.7			µs
$t_{HD;STA}$	start condition hold time	4.0			µs
t_{LOW}	SCL LOW time	4.7			µs
t_{HIGH}	SCL HIGH time	4.0			µs
t_r	SCL and SDA rise time			1.0	µs
t_f	SCL and SDA fall time			0.3	µs
$t_{SU;DAT}$	data set-up time	250			ns
$t_{HD;DAT}$	data hold time	0			ns
$t_{VD;DAT}$	SCL LOW to data out valid			3.4	µs
$t_{SU;STO}$	stop condition set-up time	4.0			µs

Note

1. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.



I²C-bus timing diagram.

INTEGRAL