International
IOR Rectifier

Preliminary Data Sheet No. PD60162J

IR2106/IR21064
IR2107/IR21074

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 5V Schmitt triggered input logic
- Matched propagation delay for both channels
- Logic and power ground +/- 5V offset.
- Lower di/dt gate driver for better noise immunity
- Outputs in phase with inputs (IR2106/IR21064)
- Outputs out of phase with inputs (IR2107/IR21074)

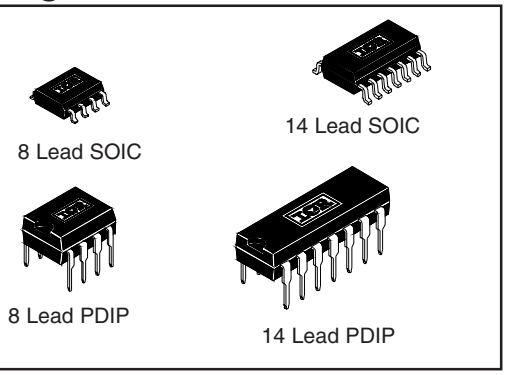
Product Summary

V_{OFFSET}	600V max.
I_{O}+/-	120 mA / 250 mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	180 ns
Delay matching	50 ns

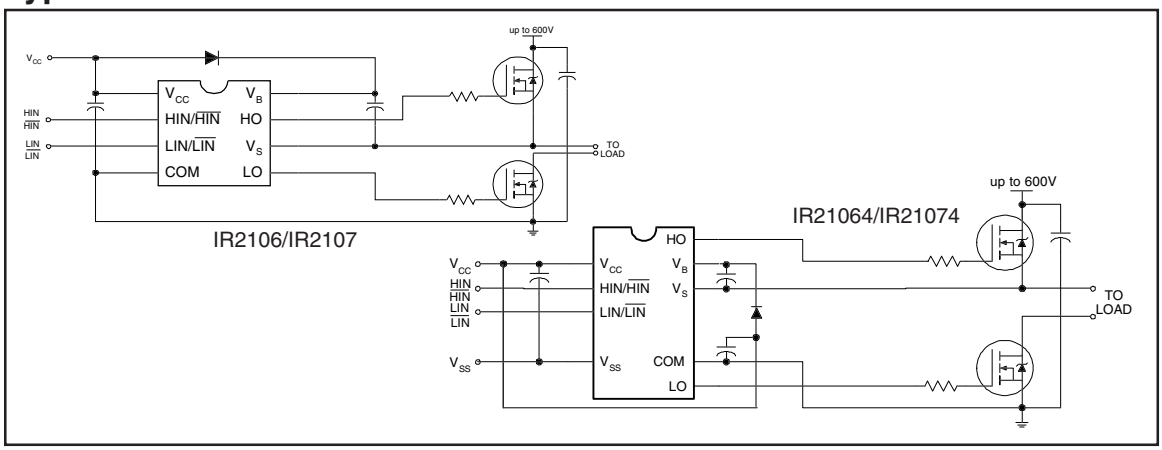
Description

The IR2106/IR21064/IR2107/IR21074 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Packages



Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating absolute voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & LIN - IR2106/IR21064) ($\overline{HIN}$ & $\overline{LIN}$ - IR2107/IR21074)		V_{SS} - 0.3	V_{CC} + 0.3	
V_{SS}	Logic ground (IR21064/IR21074 only)		V_{CC} - 25	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
		(14 lead PDIP)	—	1.6	
		(14 lead SOIC)	—	1.0	
Rth_{JA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
		(14 lead PDIP)	—	75	
		(14 lead SOIC)	—	120	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
VB	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN & LIN - IR2106/IR21064) ($\overline{HIN}$ & $\overline{LIN}$ - IR2107/IR21074)	V_{SS}	V_{CC}	
V_{SS}	Logic ground (IR21064/IR21074 only)	-5	5	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 pF, T_A = 25°C.

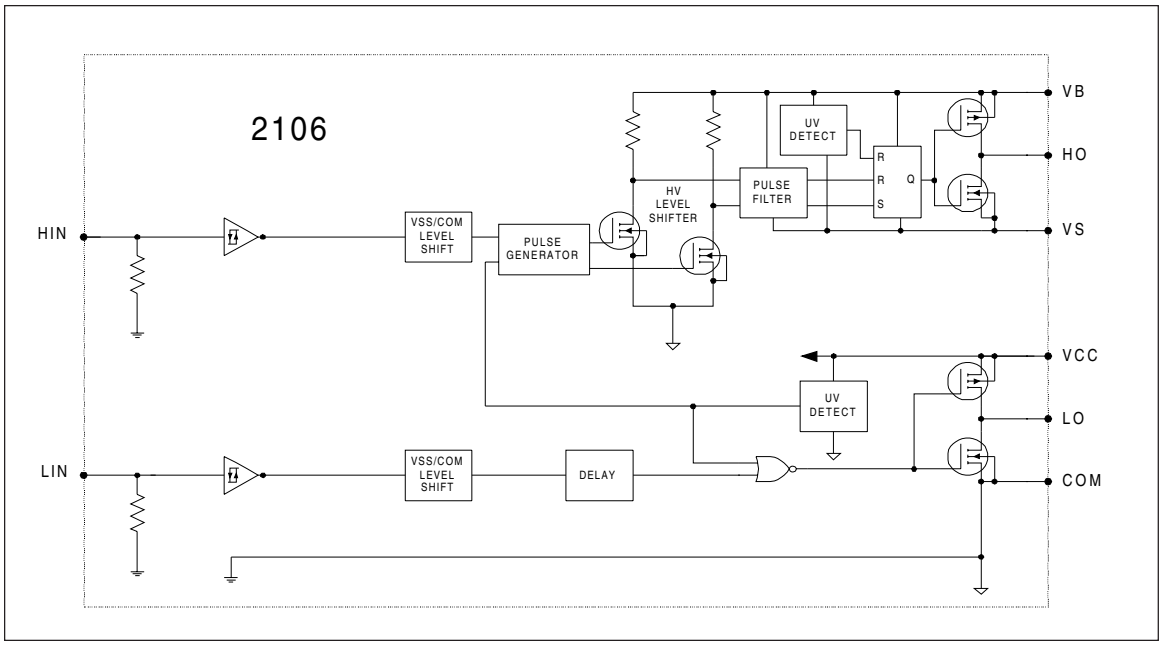
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	180	270	nsec	V_S = 0V
t_{off}	Turn-off propagation delay	—	170	250		V_S = 0V or 600V
MT	Delay matching, HS & LS turn-on/off	—	0	50		
t_r	Turn-on rise time	—	150	220		V_S = 0V
t_f	Turn-off fall time	—	50	80		V_S = 0V

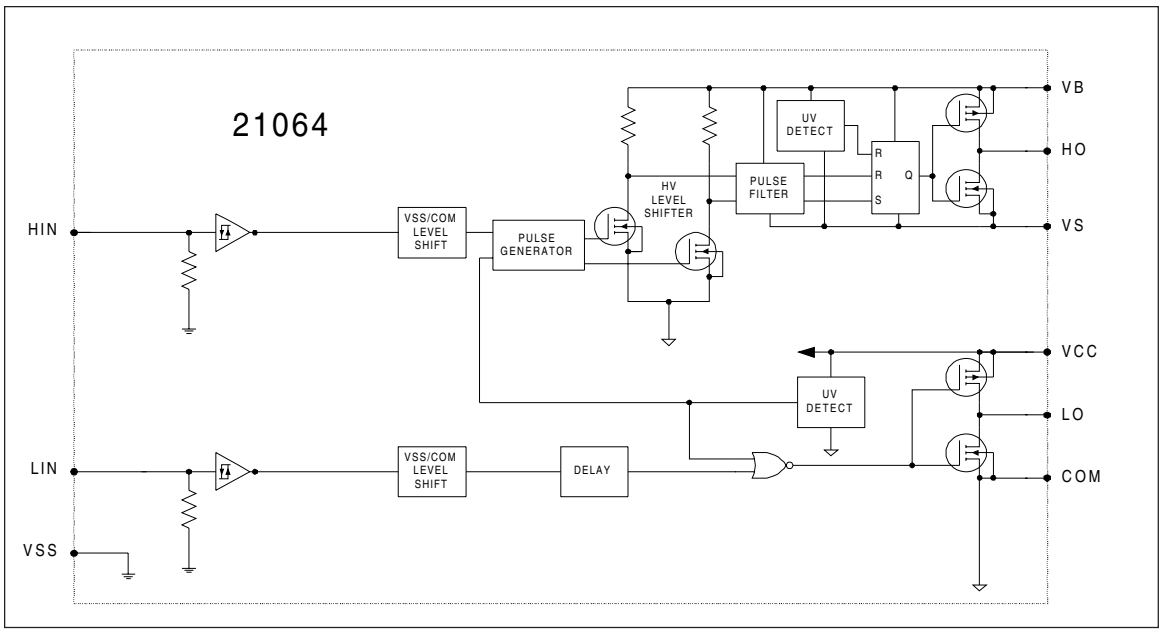
Static Electrical Characteristics

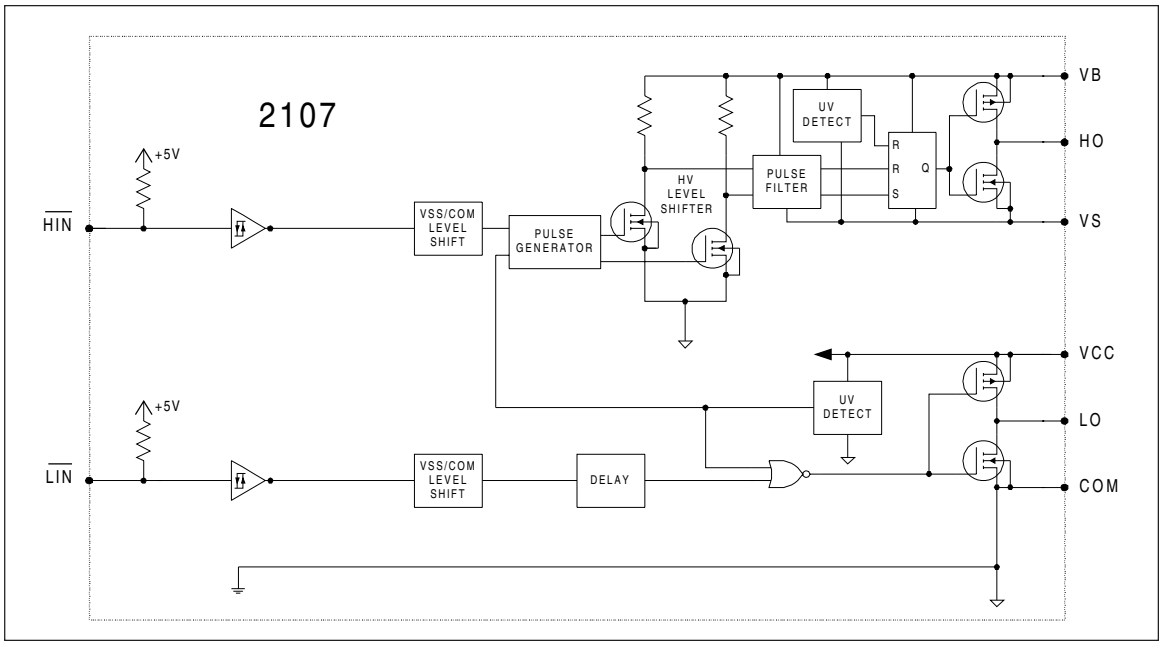
V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM and T_A = 25°C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input leads: HIN and LIN (IR2106/IR21064) and $\overline{HIN}$ and $\overline{LIN}$ (IR2107/IR21074). The V_O, I_O and Ron parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

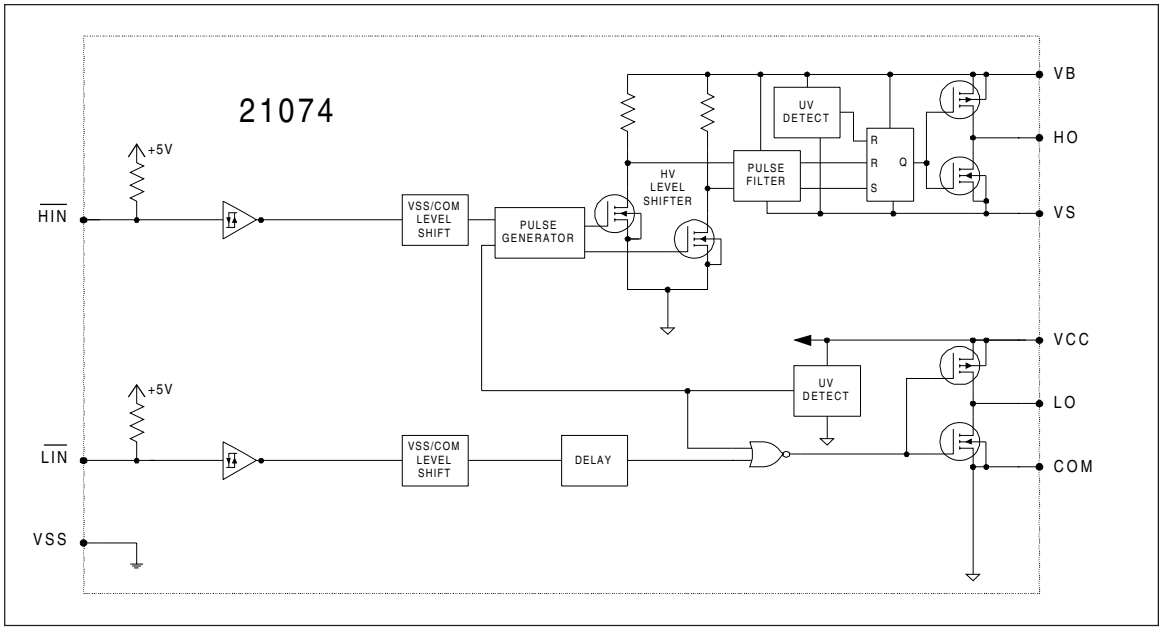
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “1” input voltage (IR2106/IR21064) Logic “0” input voltage (IR2107/IR21074)	2.7	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic “0” input voltage (IR2106/IR21064) Logic “1”input voltage (IR2107/IR21074)	—	—	0.8		V_{CC} = 10V to 20V
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	0.8	1.4		I_O = 20 mA
V_{OL}	Low level output voltage, V_O	—	0.3	0.6		I_O = 20 mA
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	20	60	150		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	50	120	240		V_{IN} = 0V or 5V
I_{IN+}	Logic “1” input bias current	—	5	20		V_{IN} = 5V (IR2106(4)) V_{IN} = 0V (IR2107(4))
I_{IN-}	Logic “0” input bias current	—	1	2		V_{IN} = 0V (IR2106(4)) V_{IN} = 5V (IR2107(4))
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O+}	Output high short circuit pulsed current	120	200	—	mA	V_O = 0V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	250	350	—		V_O = 15V, PW ≤ 10 µs

Functional Block Diagram





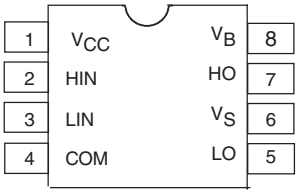

2107
+5V
HIN
VSS/COM LEVEL SHIFT
PULSE GENERATOR
HV LEVEL SHIFTER
PULSE FILTER
UV DETECT
R
R
Q
S
VB
HO
VS
VCC
LO
COM
+5V
LIN
VSS/COM LEVEL SHIFT
DELAY
UV DETECT


21074
+5V
HIN
VSS/COM LEVEL SHIFT
PULSE GENERATOR
HV LEVEL SHIFTER
PULSE FILTER
UV DETECT
R
R
Q
S
VB
HO
VS
VCC
LO
COM
+5V
LIN
VSS/COM LEVEL SHIFT
DELAY
UV DETECT
VSS

Lead Definitions

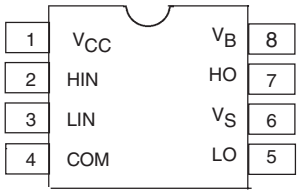
Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase (IR2106/IR21064)
$\overline{\text{HIN}}$	Logic input for high side gate driver output (HO), out of phase (IR2107/IR21074)
LIN	Logic input for low side gate driver output (LO), in phase (IR2106/IR21064)
$\overline{\text{LIN}}$	Logic input for low side gate driver output (LO), out of phase (IR2107/IR21074)
VSS	Logic Ground (IR21064 and IR21074 only)
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



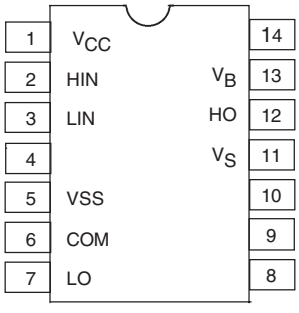
8 Lead PDIP

IR2106



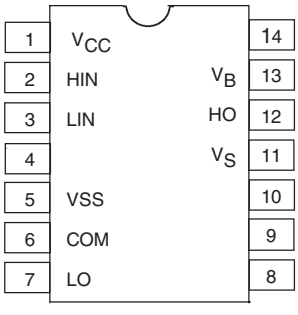
8 Lead SOIC

IR2106S



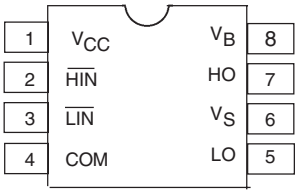
14 Lead PDIP

IR21064



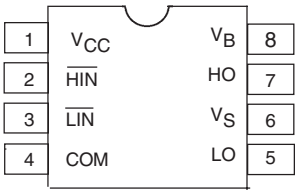
14 Lead SOIC

IR21064S



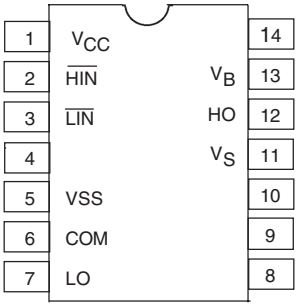
8 Lead PDIP

IR2107



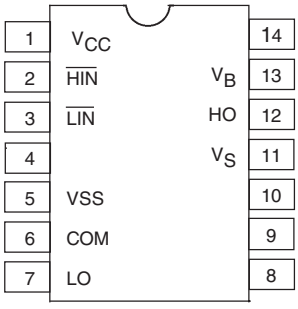
8 Lead SOIC

IR2107S



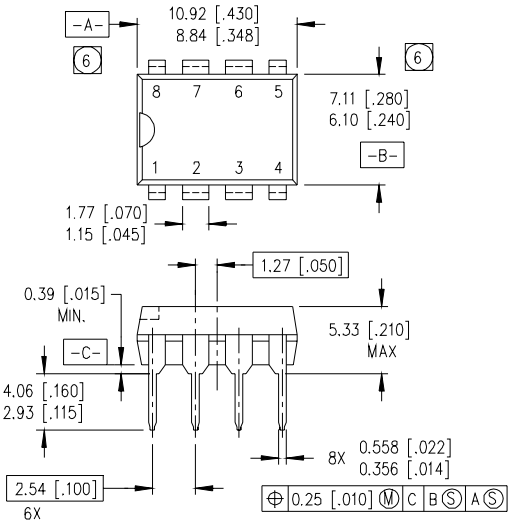
14 Lead PDIP

IR21074



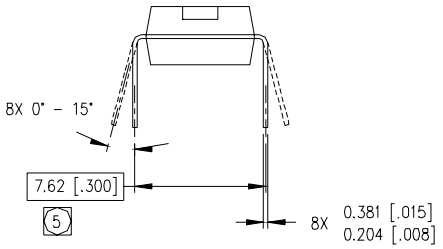
14 Lead SOIC

IR21074S



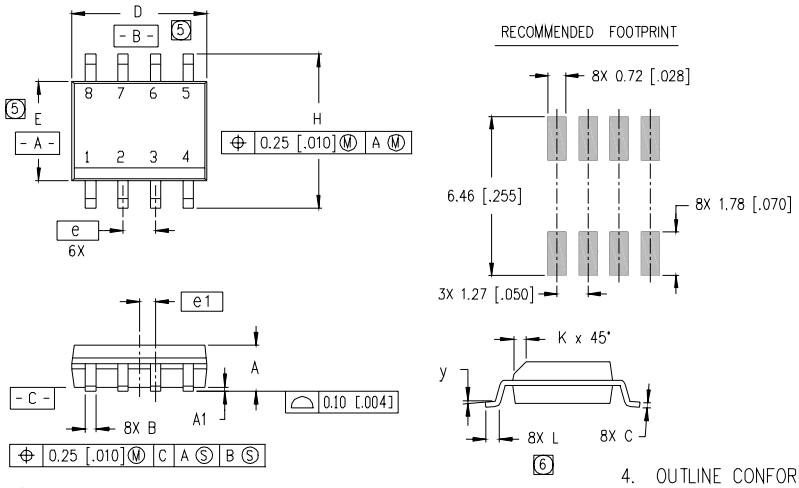
NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



8 Lead PDIP

01-3003 01



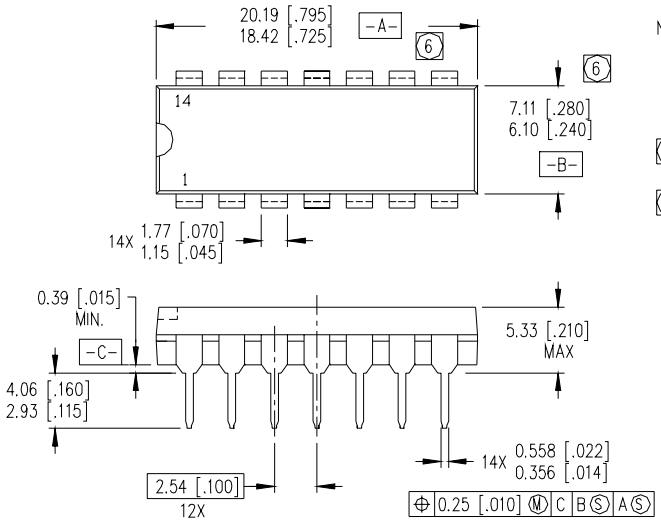
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

NOTES:

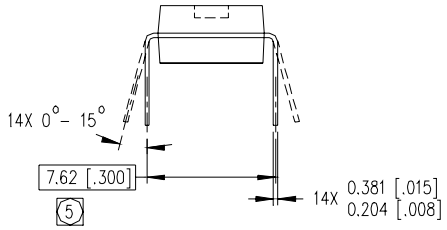
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].
6. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8 Lead SOIC

01-0021 08

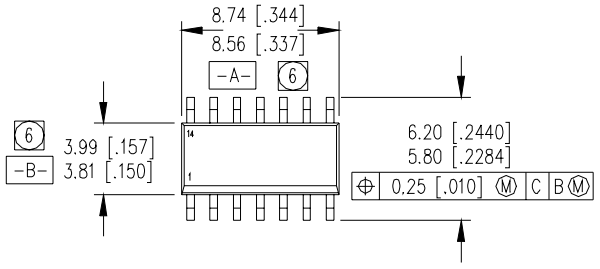


NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AC.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

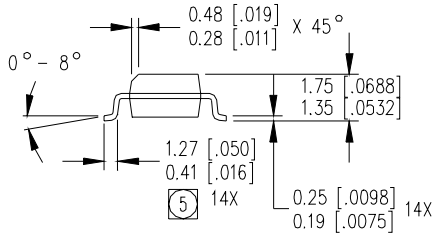


14 Lead PDIP

01-3002 03



NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2 CONTROLLING DIMENSION: MILLIMETER
3 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4 OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AB.
5 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].



14 Lead SOIC (narrow body)

01-3063 00

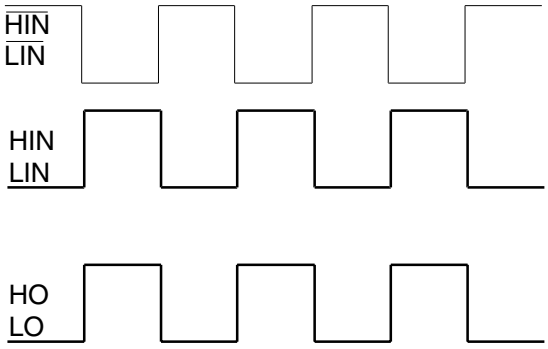


Figure 1. Input/Output Timing Diagram

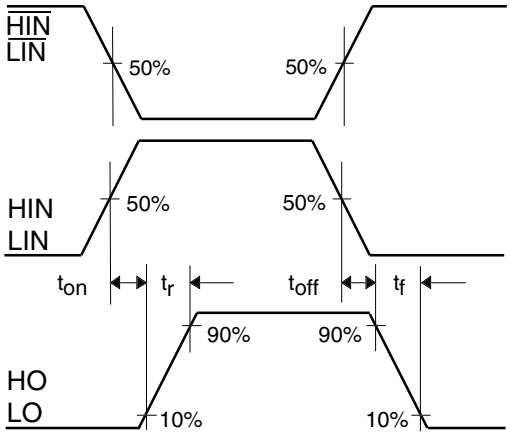


Figure 2. Switching Time Waveform Definitions

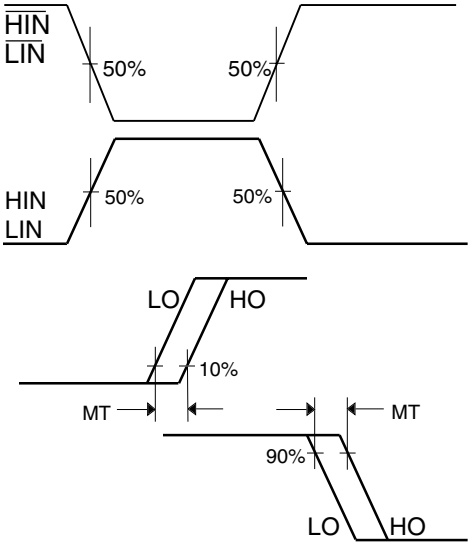


Figure 3. Delay Matching Waveform Definitions