

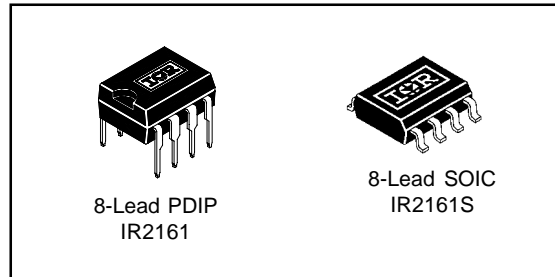
IR2161(S)

HALOGEN CONVERTOR CONTROL IC

Features

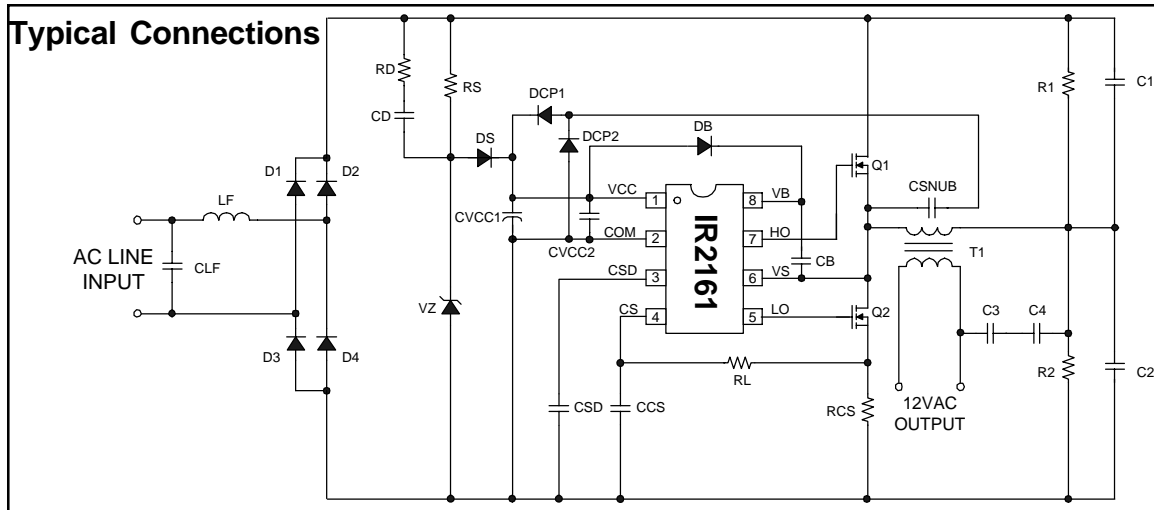
- Intelligent half-bridge driver
- Auto Resetting Short Circuit Protection
- Auto Resetting Overload Protection
- Externally Triggerable Latching Shutdown
- Latching Overtemperature Protection
- Frequency Modulation "dither" (for lower EMI)
- Micropower Startup (<300 μ A)
- Phase Cut dimmable for leading / trailing edge
- Output Voltage Shift Compensation.
- Real Softstart
- Adaptive Dead Time
- Small 8 Pin DIP/SOIC Package

Packages



Description

The IR2161 is a dedicated Intelligent Half bridge Driver IC for a Halogen convertor (electronic transformer). It includes all necessary protection features and also allows the Convertor to be dimmed externally with a standard phase cut dimmer with both leading or trailing edge types. This IC provides the advantage of reduced thermal stress in the lamp due to softstart. There is also compensation of the output voltage for load regulation. It enables the convertor to operate with extremely low harmonic distortion over the full range of loads. The IR2161 includes adaptive deadtime to allow cool running MOSFETs and improves the EMI behaviour due to frequency modulation (dither). All the features are integrated in a small 8 pin DIP/SOIC package to allow for a size reduction in the next generation of convertors.



Note: Throughout this data sheet "convertor" is spelled in accordance with standard IEC 61047 "DC or AC supplied convertors for filament lamps – Performance requirements".

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V _B	High side floating supply voltage	-0.3	625	V	
V _S	High side floating supply offset voltage	V _B - 25	V _B + 0.3		
V _{HO}	High side floating output voltage	V _S - 0.3	V _B + 0.3		
V _{LO}	Low side output voltage	-0.3	V _{CC} + 0.3		
I _O MAX	Maximum allowable output current (HO,LO) due to external power transistor miller effect	-500	500	mA	
V _{CSD} MAX	CSD pin voltage	-0.3	V _{CC} + 0.3	V	
V _{CS}	Current sense pin voltage	-0.3	V _{CC} + 0.3		
I _{CS}	Current sense pin current	-5	5	mA	
I _{CC}	Supply current (Note 1)	-20	20		
dV/dt	Allowable offset voltage slew rate	-50	50	V/ns	
P _D	Maximum power dissipation @ T _A ≤ +25°C (8 Lead DIP)	—	1	W	
	PD = (T _J MAX-T _A)/RthJA (8 Lead SOIC)	—	0.625		
RthJA	Thermal resistance, junction to ambient	(8 Lead DIP)	—	125	°C/W
		(8 Lead SOIC)	—	200	
T _J	Junction temperature	-55	150	°C	
T _S	Storage temperature	-55	150		
T _L	Lead temperature (soldering, 10 seconds)	—	300		

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V _{BS}	High side floating supply voltage	V _{CC} - 0.7	V _{CLAMP}	V
V _B MIN	Minimum required VBS voltage for proper HO functionality	—	4	
V _S	Steady state high-side floating supply offset voltage	-1	600	
V _{CC}	Supply voltage	V _{CC} UV+	V _{CLAMP}	
I _{CC}	Supply current	(Note 2)	10	mA
C _S D	CSD pin external capacitor	47	—	nF
I _{CS}	Current sense pin current	-1	1	mA
T _J	Junction temperature	-25	125	°C

Note 1: This IC contains a zener clamp structure between the chip V_{CC} and COM which has a nominal breakdown voltage of 15.6V. Please note that this supply pin should not be driven by a DC, low impedance power source greater than the V_{CLAMP} specified in the Electrical Characteristics section.

Note 2: Enough current should be supplied into the V_{CC} pin to keep the internal 15.6V zener clamp diode on this pin regulating its voltage, V_{CLAMP}.

Electrical Characteristics

$V_{CC} = V_{BS} = V_{BIAS} = 14V$, $\pm 0.25V$, $V_{CSD} = 5.0V$, $C_{LO} = C_{HO} = 1000 \text{ pF}$, and $T_A = 25^\circ\text{C}$ unless otherwise specified.

Supply Characteristics						
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	10.8	11.8	12.8	V	V_{CC} rising from 0V
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	9.2	10.2	11.2		V_{CC} falling from 14V
V_{CCUVL-}	V_{CC} supply softstart reset negative going threshold	—	—	5.5		$V_{CC} - V_{CCUV-} (-2V)$
I_{QCCUV}	UVLO mode quiescent current	—	—	300	μA	$V_{CC} = 11V$
I_{CCFLT}	Fault-mode quiescent current	—	—	2	mA	$CS=8V, V_{CSD}=0V$
I_{CCLF}	V_{CC} current (low frequency)	—	2	—		$V_{CC}=14V, V_{CSD}=5.2V$
I_{CCHF}	V_{CC} current (high frequency)	—	4.1	—		$V_{CC}=14V, V_{CSD}=0V$
V_{CLAMP}	V_{CC} zener clamp voltage	14.5	15.5	16.5	V	$I_{CC} = 5mA$
Floating Supply Characteristics						
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
I_{BSHF}	V_{BS} high frequency supply current	—	—	3.4	mA	$V_{CC}=14V, V_{BS}=14V, V_{CSD}=0V$
I_{BSLF}	V_{BS} low frequency supply current	—	—	1		$V_{CC}=14V, V_{BS}=14V, V_{CSD}=5.2V$
I_{LEAK}	Offset supply leakage current	—	—	50	μA	$V_B = V_S = 600V$
Voltage Compensation Characteristics (Run Mode)						
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{CSD (min)}$	Min CSD voltage (in Run Mode)	—	0	—	V	$V_{CS} = 0V$
$V_{CSD (max)}$	Max CSD voltage (in Run Mode)	—	5.5	—	V	$V_{CS} = 0.4V$

Electrical Characteristics (cont'd)

$V_{CC} = V_{BS} = V_{BIAS} = 14V$, $\pm 0.25V$, $V_{CSD} = 5.0V$, $C_{LO} = C_{HO} = 1000 \text{ pF}$, and $T_A = 25^\circ\text{C}$ unless otherwise specified.

Shutdown Circuit Characteristics						
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
VCSOL	Overload threshold (CS PID)	0.46	0.54	0.63	V	
VCSSC	CSD short circuit threshold (CS PID)	1	1.2	1.4		
IOL	CSD overload charging current	—	9.7	12.0	uA	VCS=0.8V, VCSD=7V
ISC	CSD short circuit charging current	84	104	125		VCS=1.5V, VCSD=7V
IRESET	CSD shutdown reset current	0.3	0.65	1		VCSD=14V, Note 3
VCSLATCH	Latched shutdown threshold	—	9	—	V	
TCSLATCH	Latched shutdown delay	—	1	—	μsec	VCS>VCSLATCH
VCSDOL	Begin fault timing	—	4.5	—	V	VCS>VCSOL
VCSDSD	Positive going threshold for oscillator shutdown	—	12	—		VCS > VCSOL
VCSDRS	Negative going threshold for oscillator restart	—	2.7	—		
Thermal Shutdown Characteristics						
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
T _{SD}	Latched over temperature limit	—	135	—	°C	
Oscillator Characteristics						
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
f _(min)	Minimum oscillator frequency	—	33	—	kHz	VCS = 5.3V
f _(max)	Maximum oscillator frequency in RUN mode	—	62	—		VCS = 0V
D	Oscillator duty cycle	—	50	—	%	
DT _{LO(max)}	Maximum LO output deadtime (run mode default)	—	1.2	—	μsec	no reset from ADT
DT _{HO(max)}	Maximum HO output deadtime (run mode default)	—	1.5	—		
Adaptive Dead-Time System Characteristics						
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
DT _{LO(min)}	Minimum LO output deadtime	—	—	300	μsec	Minimum propagation delay from ADT to output drivers
DT _{HO(min)}	Minimum HO output deadtime	—	—	500		

Electrical Characteristics (cont.)

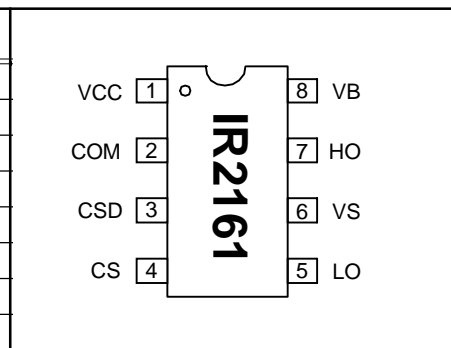
$V_{CC} = V_{BS} = V_{BIAS} = 14V$, $\pm 0.25V$, $V_{CSD} = 5.0V$, $C_{LO} = C_{HO} = 1000\text{ pF}$, and $T_A = 25^\circ\text{C}$ unless otherwise specified.

Soft Start Characteristics						
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
I_{SS}	Soft start CSD charge current	—	0.6	—	mA	
f_{SS}	Soft start frequency	—	130	—	kHz	$V_{CC} > V_{CCUV+}$
Gate Driver Output Characteristics						
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{LO=LOW}$	$V_{LO} - V_{COM}$ difference between LO output voltage and COM when LO is low	—	100	—	mV	$V_{CSD} = 0V$
$V_{HO=LOW}$	$V_{HO} - V_S$ difference between HO output voltage and V_S when HO is low	—	100	—		$V_{CSD} = 0V$
$V_{LO=HIGH}$	$V_{CC} - V_{LO}$ difference between V_{CC} and LO output voltage when LO is high	—	100	—		$V_{CSD} = 0V$
$V_{HO=HIGH}$	$V_B - V_{HO}$ difference between V_B and HO output voltage when HO is high	—	100	—		$V_{CSD} = 0V$
t_{RISE}	Turn-on rise time	—	110	200	ns	$C_{HO} = C_{LO} = 1nF$
t_{FALL}	Turn-off fall time	—	55	150		
IO+	HO, LO source current	—	300	—	mA	
IO-	HO, LO sink current	—	400	—		

Lead Definitions

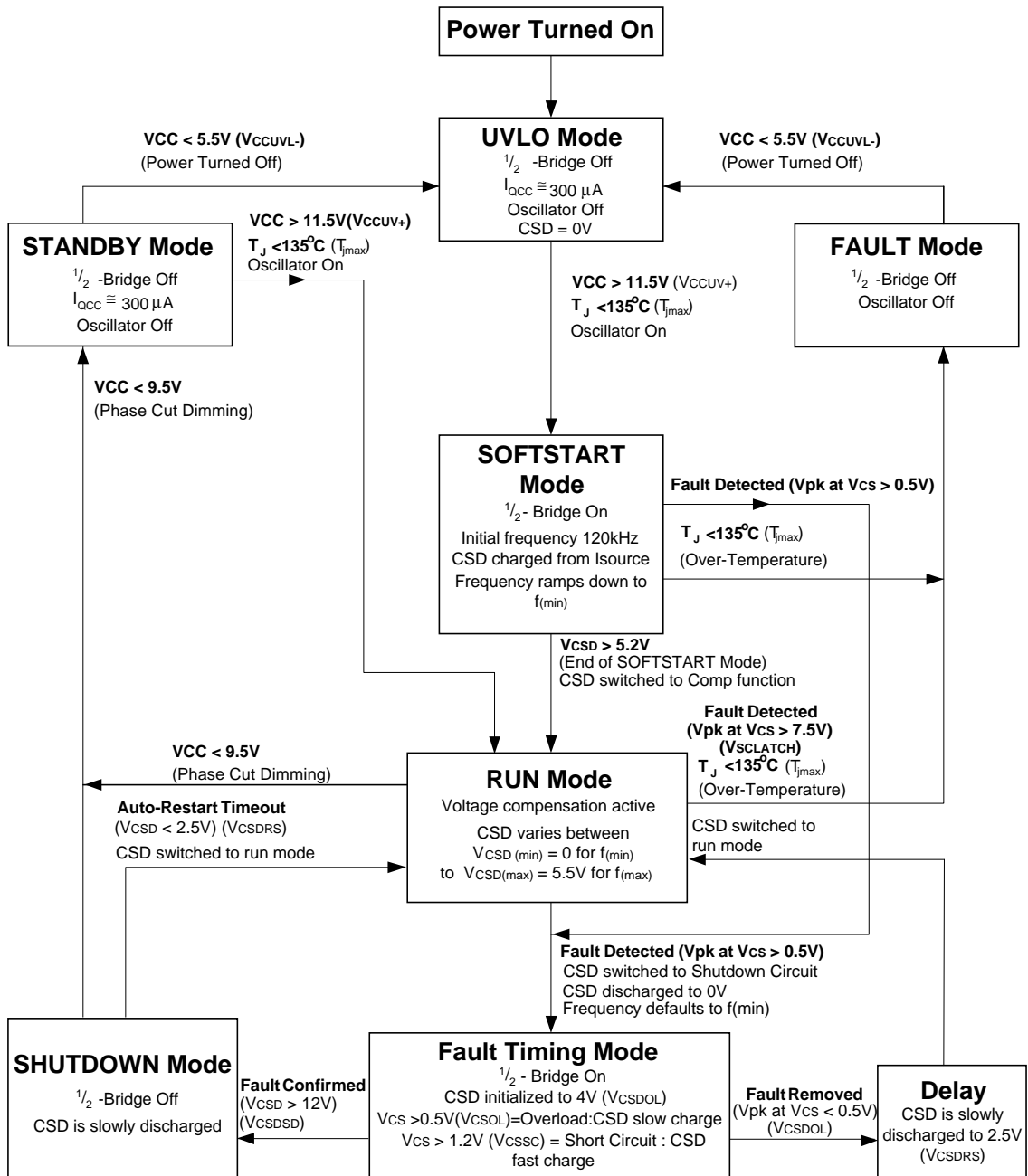
Symbol	Description
V_{CC}	Supply voltage
COM	IC power and signal ground
CSD	Shutdown timing and compensation capacitor
CS	Current sensing input
LO	Low-side gate driver output
V_S	High-side floating return
HO	High side gate driver output
V_B	High side gate driver floating supply

Lead Assignments



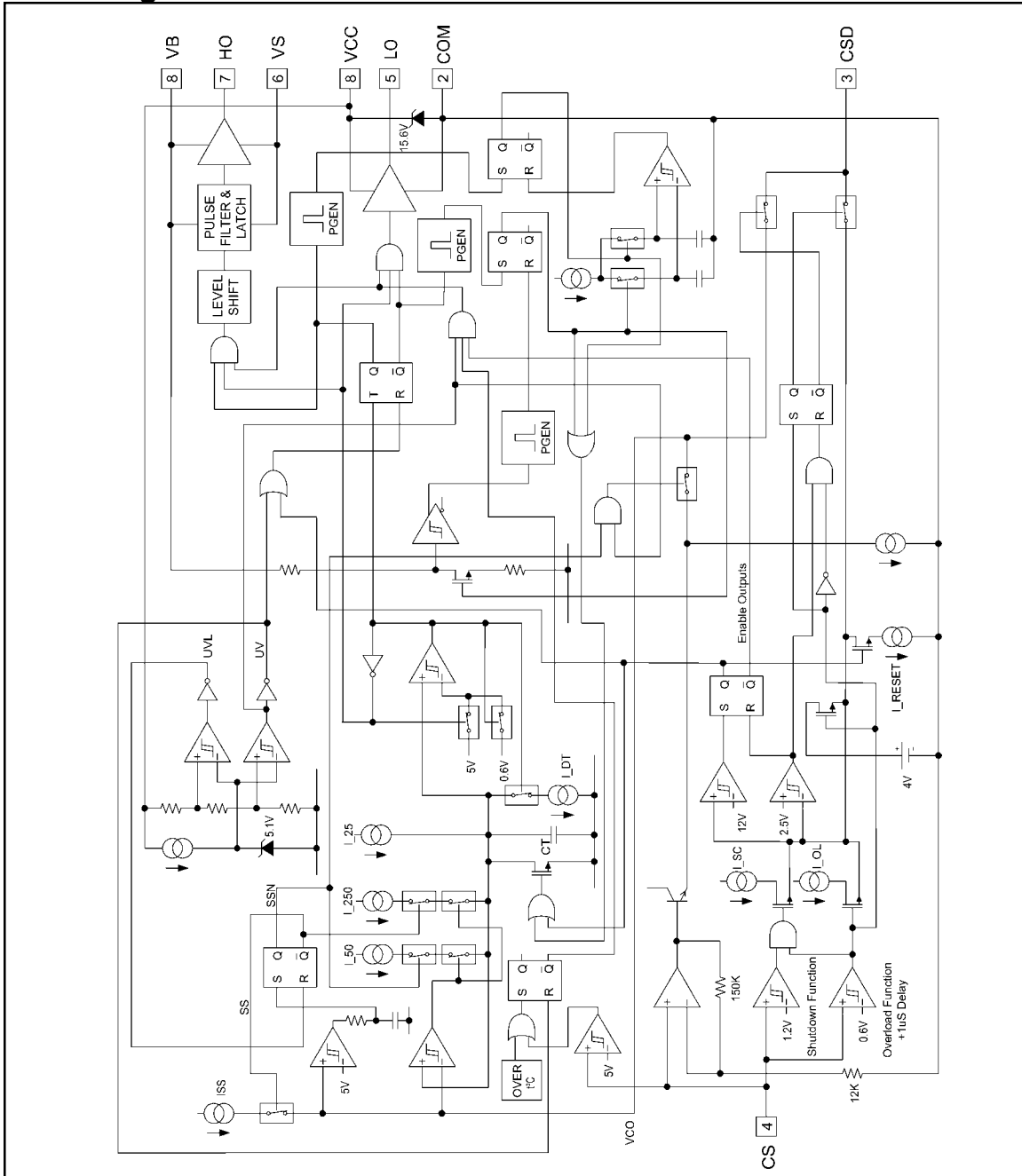
* Recommended value for CSD is 100nF (all performance data relates to this value)

NOTE: The recommended value for RL is 1K Ohm and CCS is 1nF.



NOTE: If the IR2161 die temperature exceeds 130C at any time the system will enter FAULT Mode. At a typical frequency of 40kHz, the die temperature is approximately 12°C above the ambient air temperature

Block Diagram



minimum frequency over a period of around 1s (assuming CSD=100nF). During this time the external capacitor at the CSD pin charges from 0V to 5V, controlling the oscillator frequency through the internal voltage controlled oscillator (VCO). The value of CSD will determine the duration of the soft start sweep. However, since it also governs the shut down circuit delays, the value should be kept at 100nF to achieve the datasheet operation

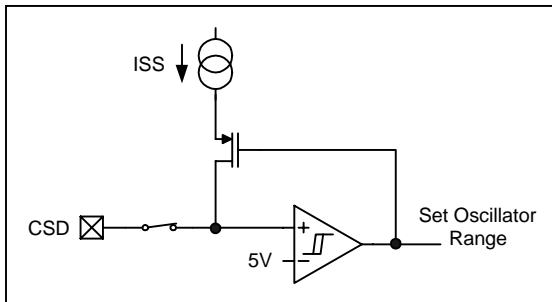


Figure 2, Halogen Converter.

It can be seen from Figure 2, that at switch on, the CSD capacitor is internally switched to the soft start circuit input. A current source charges CSD linearly to 5V over a period of 0.5s at which time the comparator output goes high. The PMOS switch opens and the ISS current source is disconnected from CSD. The comparator latches high at this point and this causes the oscillator range to change and the CSD capacitor to be disconnected from the soft start circuit and connected to the voltage compensation circuit. The latching comparator has a built in delay of at least 20uS in order to prevent false triggering caused by transients.

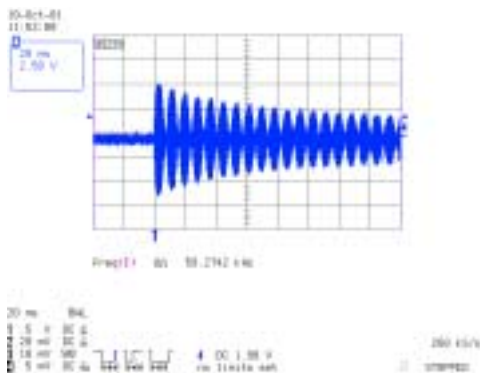


Figure 3, Typical Cold Lamp Inrush Current.

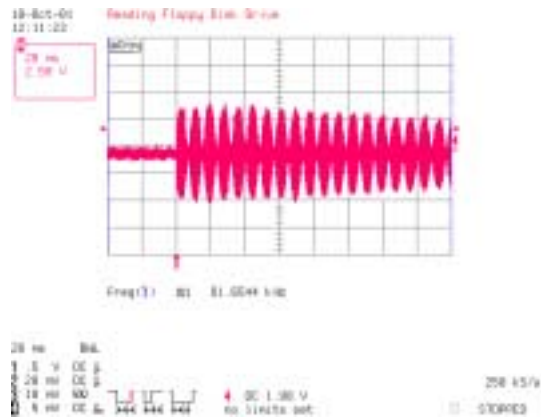


Figure 4, Cold Lamp Inrush Current with Soft Start.

Run Mode (Voltage Compensation)

When soft start is completed the system switches over to compensation mode. This function provides some regulation of the output voltage of the converter from minimum to maximum load. In this type of system it is desirable that the voltage supplied to the lamp does not exceed a particular limit. If the lamp voltage becomes too high the temperature of the filament runs too high and the life of the lamp is significantly reduced. The problem is that the output transformer is never perfectly coupled so there will always be a degree of load regulation.

The transformer has to be designed such that the lamp voltage at maximum load is sufficiently high to ensure adequate light output.

At minimum load the voltage will consequently be higher and is likely to exceed the maximum desired lamp voltage.

In the widely used self-oscillating system based around bipolar power transistors, there is some frequency change (increasing the frequency reduces the output voltage) depending on the load that helps to compensate for this, although this is non-linear and depends on many parameters in the circuit and so is not easy to predict.

The IR2161 based system includes a function that monitors the load current through the current sense resistor (RCS). The peak current is detected and amplified within the IC then appears at the CSD pin during run mode. The voltage

across the CSD capacitor will vary from 0V if there is no load to approximately 5V at maximum load.

This is provided that the correct value of current sense resistor has been selected for the maximum rated load and line voltage supply of the converter. This should be 0.33 Ohm (0.5W) for a 100W system running from a 220-240V AC line. (It should be noted that the RCS resistor value is also critical for setting the limits for the shut down circuit)

In RUN mode the oscillator frequency will vary from approximately 30kHz when VCSD is 5V (maximum load) to 55kHz when VCSD is 0V (no load). The result of this is that if a lighter load, such as a single 35W lamp, is connected to a 100W converter, the frequency will shift upwards so that the output voltage falls below the maximum that is desirable for the lamp. This provides sufficient compensation for the load to ensure that the lamp voltage will always be within acceptable limits but does not require a complicated regulation scheme involving feedback from the output.

An additional internal current source has been included to discharge the external capacitor. This will provide approximately 10% ripple at twice the line frequency if CSD is 100nF.

The advantage of this is that during the line voltage half cycle the oscillator frequency will vary by several kHz thus spreading the EMI conducted and radiated emissions over a range of frequencies and avoiding high amplitude peaks at particular frequencies. In this way the filter components used may be similar to those used in a common bipolar self-oscillating system.

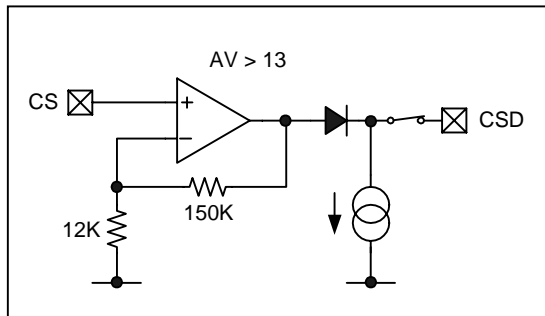


Figure 5, Voltage Compensation Circuit

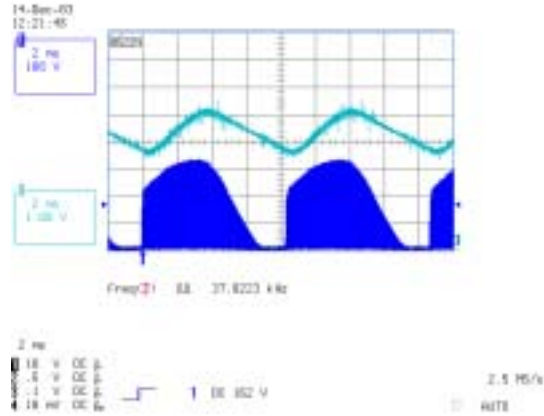


Figure 6, VS voltage and CSD voltage.

In the above trace it can be seen that a leading edge phase cut (triac) dimmer is connected at close to maximum brightness. There is a short delay at the beginning of each half cycle before the AC line voltage is switched to the converter. Dimming increases the ripple in the CSD voltage and gives more modulation. This is an inherent effect that causes no system problems.

The startup sequence of the CSD pin can be seen from the point where VCC increases above the UVLO+ threshold.

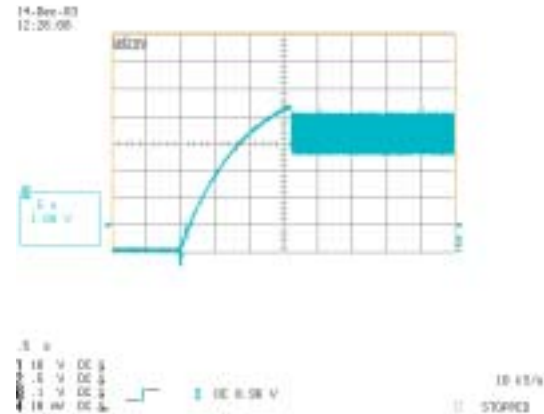


Figure 7, Startup sequence of CSD.

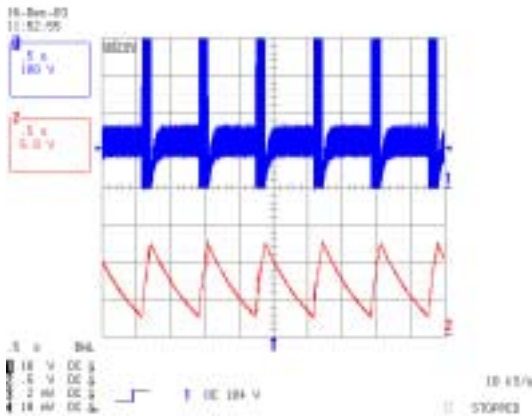


Figure 9, Short Circuit Output Current.

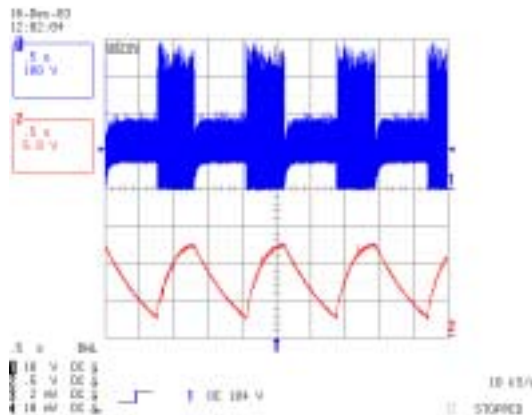


Figure 10, Overload Output Current.

In figures 9 and 10, trace (1) shows the half bridge oscillations during both types of fault mode and trace (2) shows the charging and discharging of the CSD capacitor.

The IR2161 can also be externally shut off by applying a voltage above $0.5 \cdot V_{CC}$ to the CS pin. This will cause the system to go directly to a latched fault mode, after a delay of approximately 1 μ s to avoid the possibility of false tripping caused by transients. To restart the system, it is necessary to cycle Vcc off and on.

In addition, any time Vcs exceeds VCSLATCH (approximately half Vcc), this latching shutdown function will be triggered and the system will remain in FAULT mode until VCC is re-cycled.

The IR2161 also includes over temperature shutdown, which latches the convertor off when the die temperature of the IC exceeds 130-140°C. Experimental measurement reveal that the die temperature will be no more than 20°C above the ambient temperature at all operating frequencies inside the convertor.

Calculating Rcs

The value of the current sense resistor Rcs is critical to achieve correct operation in the IR2161 based Halogen convertor.

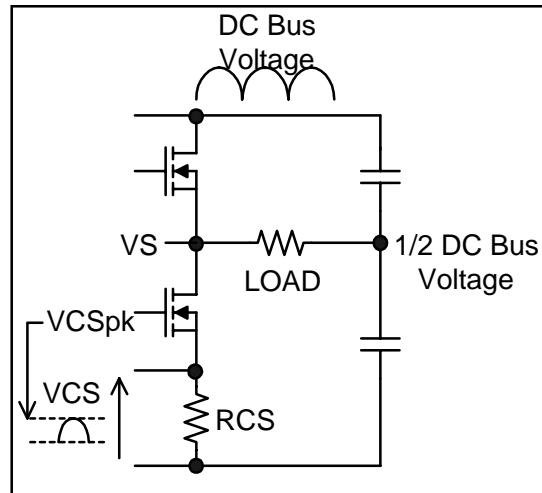


Figure 11, Calculating Rcs

Ignoring the output transformer we can assume for this calculation that the load is connected from the half bridge to the mid point of the two output capacitors and that the voltage at this point will be half the DC bus voltage. The RMS voltage of the DC bus is the same as that of the AC line so we can see that the RMS voltage across the load shown in Figure 8, will be half the RMS voltage of the line. The load is the maximum rated load of the convertor. The current in Rcs will be half the load current given by :

$$I_{CS(RMS)} = \frac{P_{LOAD}}{V_{AC}}$$

Since the load is resistive the current waveform will have a sinusoidal envelope and so the peak can be easily determined taking into account that the current has a high frequency component with an approximate 50% duty cycle:

$$I_{CS(PK)} = 2\sqrt{2} \times I_{CS(RMS)}$$

Therefore:

$$V_{CS(PK)} = I_{CS(PK)} \times R_{CS}$$

For correct operation at maximum load the peak voltage should be 0.4V.

The calculation can be simplified by combining the formulae,

$$R_{CS} = \frac{0.4 \cdot V_{CS}}{2 \cdot \sqrt{2} \cdot P_{LOAD}}$$

Which can be simplified to:

$$R_{CS} = 0.141 \cdot \frac{V_{AC}}{P_{LOAD}}$$

Example

For a 100W convertor working from a 230VAC supply the current sense resistor would need to be :

$$\frac{0.141 \times 230}{100} = 0.324\Omega$$

The nearest preferred value to this would be 0.33 Ohms.

The power dissipation in Rcs should also be considered and is given by :

$$P_{CS} = \left(\frac{P_{LOAD}}{V_{AC}} \right)^2 \times R_{CS}$$

In this case :

$$\left(\frac{100}{230} \right)^2 \times 0.33 = 0.062W$$

It is important to bear in mind that the resistor must be rated to handle this current in a high ambient temperature.

IMPORTANT NOTE

The filter resistor RL should be 1K, which is needed to protect the CS input from negative going transients. CCS should be 1nF and is also necessary to filter out switching transients that can impair the operation of the shutdown circuit.

Adaptive Dead Time

Because of the fact that the DC bus voltage varies during the mains half cycle, the dead time may need to vary in order to achieve soft switching. The IR2161 has an adaptive dead time circuit (ADT) that detects the point at which the voltage at the half bridge slews to 0V (COM) and sets the LO output high at this point. There is an internal sample and hold system that allows approximately the same delay to be used to set HO high after LO has gone low. This reacts on a cycle-by-cycle basis of the oscillator and therefore will adjust the dead time as necessary regardless of external conditions.

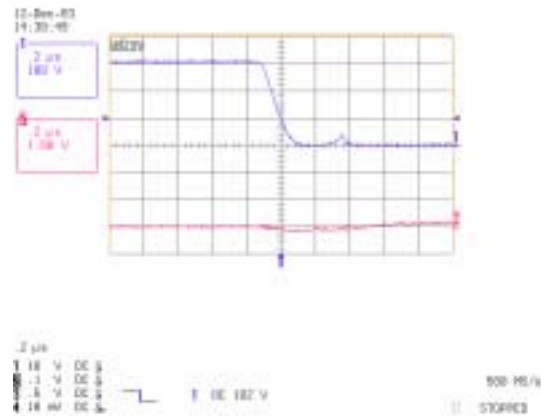


Figure 12, ADT when VS slews from VBUS to COM

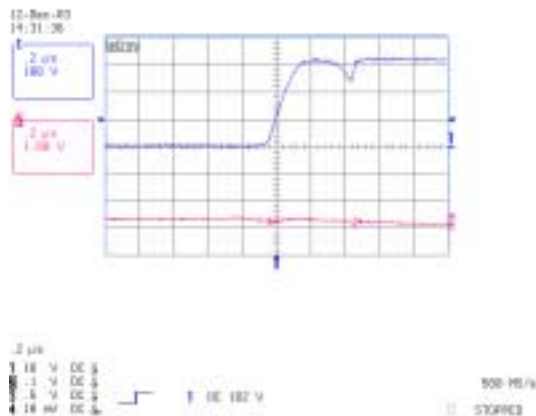


Figure 13, ADT when VS slews from COM to VBUS

The above waveforms are typical, showing the operation of the ADT circuit in either direction. In this case the design could be optimized further by increasing the snubber capacitor to slightly increase the slew time, in order to account for the propagation delays in the system. Alternatively an output transformer with a greater leakage inductance can extend the period before the VS voltage turns around and starts to go back the other way again.

The designer does not need to take into account parasitic capacitances in the MOSFETs or leakage inductance in the output transformer and fix the dead time accordingly.

The system can operate reliably down to dead times in the order of 300nS, which should be low enough to accommodate the output transformer leakage inductance and parasitic MOSFET capacitances of a practical Halogen convertor.

The slew rate can easily be increased, if necessary, by adding a small *snubber* capacitor across the primary of the transformer if necessary. However, should the snubber capacitor be too large, it will prevent the VS voltage from slewing all the way to the opposite rail. Consequently the ADT function will be unable to operate, causing the IR2161 to revert to the default dead time of 1.2 to 1.4µS. Snubber capacitors would normally be in the order of hundreds of pF.

When designing a halogen convertor it is desirable to optimize the system at maximum load, where the conduction losses

of the power MOSFETs in the half-bridge will be at a maximum. At lighter loads there may be hard switching if the VS voltage is unable to slew all the way or it slews so rapidly that the voltage begins to turn around again before the IR2161 is able to switch on the relevant MOSFET in the half bridge.

Such a situation is not desirable but may be acceptable at lighter loads where the conduction losses are small.

With correct optimization of the output transformer and surrounding circuit it is possible to achieve a design that will not hard switch from 20% to 100% of the maximum rated load of the system.

This system avoids the need for an external resistor to program the dead time and contributes to the multi functional nature of the CSD pin to the IR2161 being realized with only 8 external pins

In any design when there is no load at the output, the VS voltage will not slew and obviously the ADT circuit is not able to function in this condition. In this case the dead time will default to approximately 1.2µS, the maximum allowed by the IC and there will be hard switching.

Although this will inevitably lead to some switching losses, there are no conduction losses so the temperature rise of the half bridge MOSFETs should not create a problem in this case.

Dimming

Almost any Halogen convertor available can be dimmed by an external *phase cut* dimmer that operates in *trailing edge* mode. This means that at the beginning of the line voltage half cycle, the switch inside the dimmer is *closed* and mains voltage is supplied to the convertor allowing the convertor to operate normally. At some point during the half cycle, the switch inside the dimmer is *opened* and voltage is no longer applied. The DC bus inside the convertor almost immediately drops to 0V and the output is no longer present. In this way bursts of high frequency output voltage are applied to the lamp. The RMS voltage across the lamp will naturally vary depending on the phase angle at which the dimmer switch switches off. In this way the lamp brightness may easily be varied from zero to maximum output.

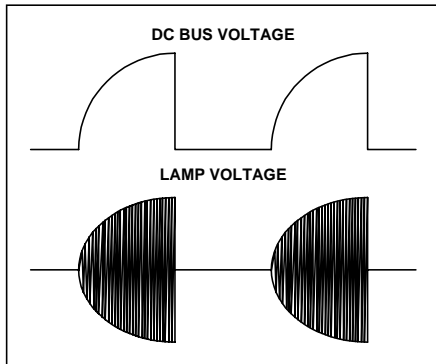


Figure 14, Trailing Edge Dimming

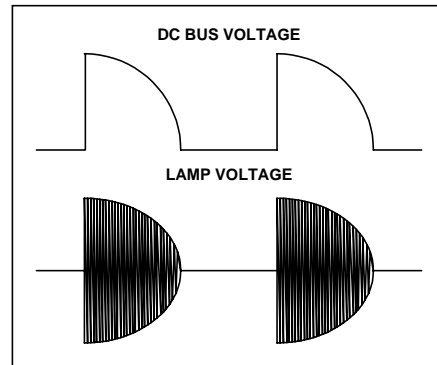


Figure 15, Leading Edge Dimming

Trailing edge dimmers are less common however than leading edge dimmers. This is because they are more expensive to make and need to incorporate a pair of MOSFETs or IGBTs whereas a leading edge dimmer is based around a single triac.

Conversely many Halogen convertors are not able to operate with leading edge dimmers because of the fact that they are based around a triac. It is possible, however, to design a Halogen convertor that will work effectively with a triac based dimmer by designing the input filter components correctly ensuring that at the firing point of the triac the oscillator can start up rapidly. In the IR2161 based system this is easy to achieve through the addition of RD and CD, which conduct a large current to VCC due to the high dv/dt that occurs when the triac fires. At the same time, the bus voltage rises rapidly from zero to the AC line voltage. If the VCC voltage falls below UVLO- during the time when the triac in the dimmer is off, the soft start will not be initiated because the soft start circuit is not reset until VCC drops approximately 2V below UVLO-. This takes some time as the VCC capacitor discharges very slowly during UVLO micro-power operation. The intermediate period is referred to as Standby mode.

During dimming the voltage compensation circuit will cause a frequency shift upward at angles above 90° because the peak voltage at CS will be reduced (see figure 15). This will result in a reduction of voltage at CSD and thus an increase in frequency. However this will not have a noticeable effect on the light output.

The problem associated with operation of Halogen convertors with triac dimmers is due to the fact that after a triac has been fired it will conduct until the current falls below its

holding current. If the load is purely resistive (as in a filament lamp directly connected to the dimmer) this will naturally happen at the end of the line voltage half cycle as the current has to fall to zero. In a Halogen convertor it is necessary to place a capacitor and inductor at the AC input to comply with regulations regarding EMI conducted emissions. This means that when the line voltage falls to zero there could still be some current flowing that is enough to keep the triac switched on and so the next cycle will follow through and not be phase cut as required. This can happen intermittently resulting in flickering of the lamps. The way to avoid the problem is to ensure that the product has the smallest possible filter capacitor CCS and to state a minimum load for the convertor. This would be typically one third of the maximum load to avoid problems of this kind.

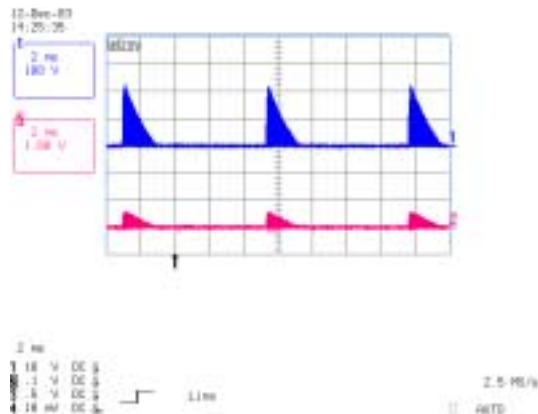
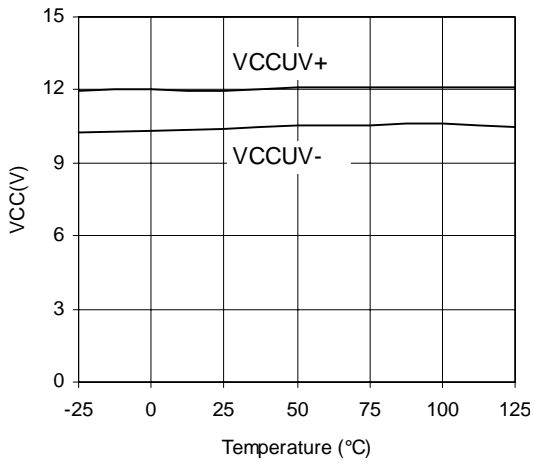
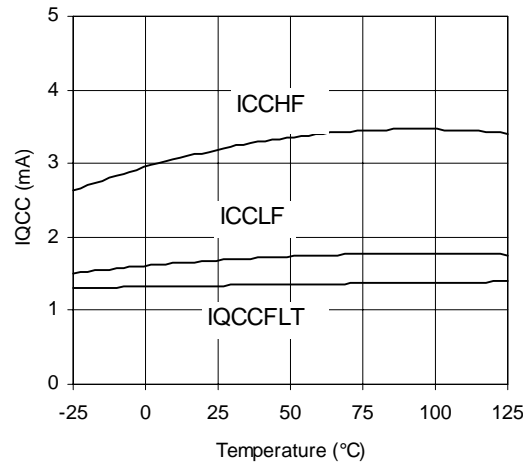


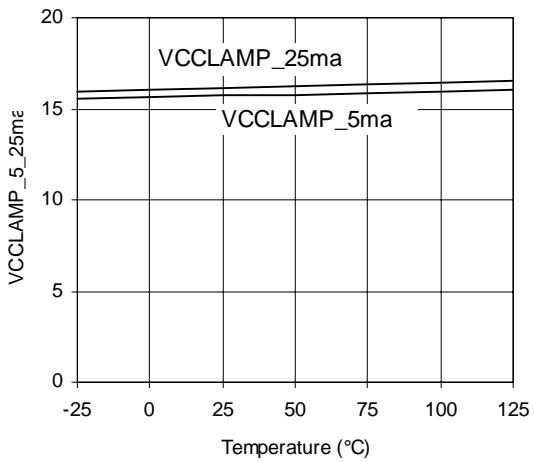
Figure 15, Half Bridge voltage and current during dimming



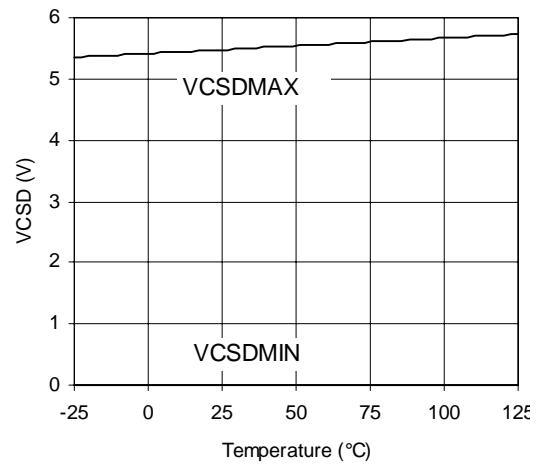
Graph : VCCUV+/- vs TEMP (IR2161)



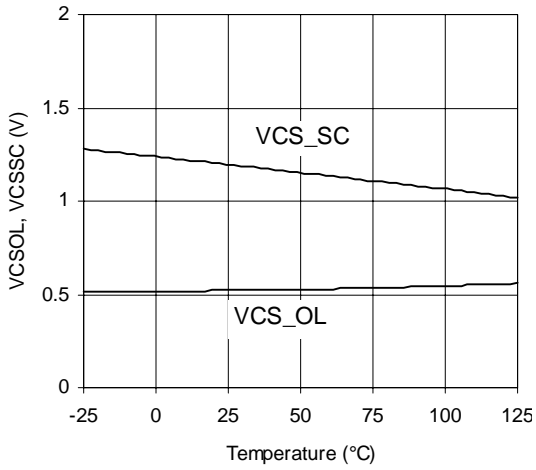
Graph : IQCC vs TEMP (IR2161)



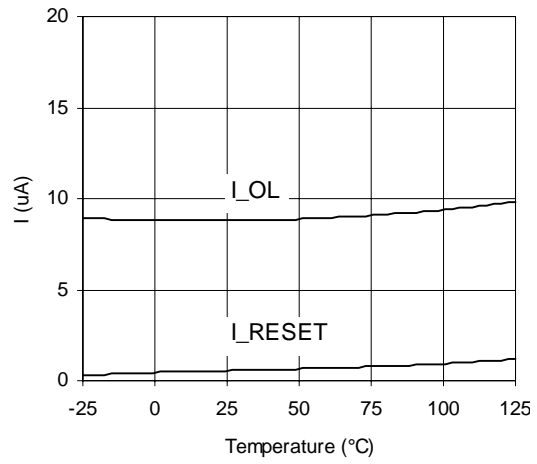
Graph : VCCLAMP_5_25ma vs TEMP (IR2161)



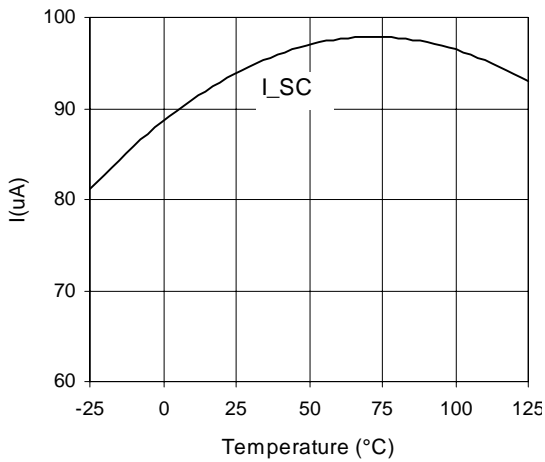
VCSDMIN,MAX vs TEMP (IR2161)



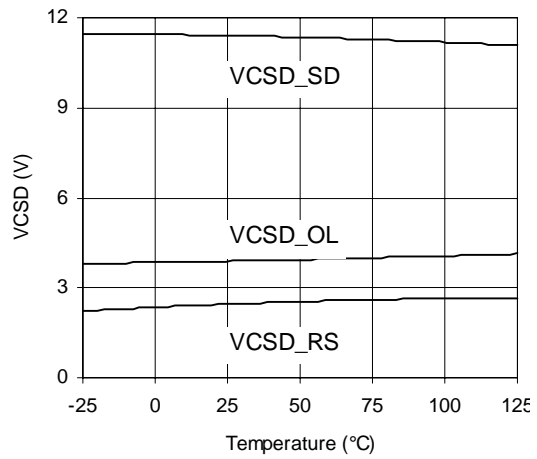
VCS_OL, VCS_SC vs TEMP (IR2161)



I_RESET, I_OL vs TEMP (IR2161)



I_SC vs TEMP (IR2161)

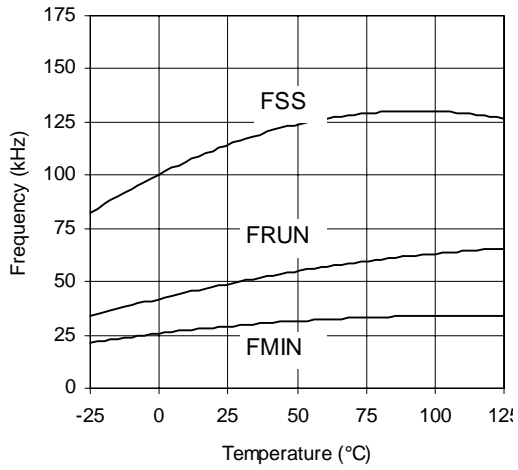


Graph : VCSDSD,OL,RS vs TEMP (IR2161)

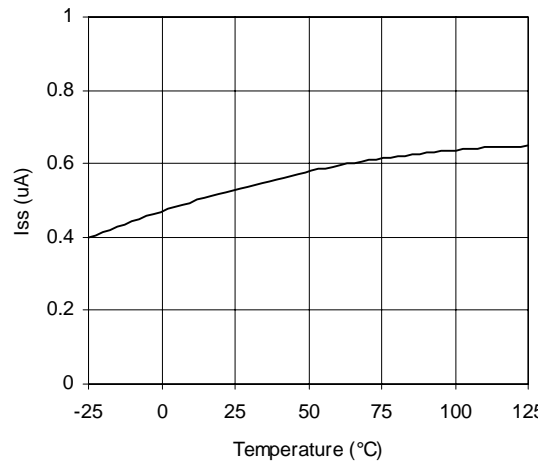
IR2161(S)

ADVANCE DATA

International
IR Rectifier

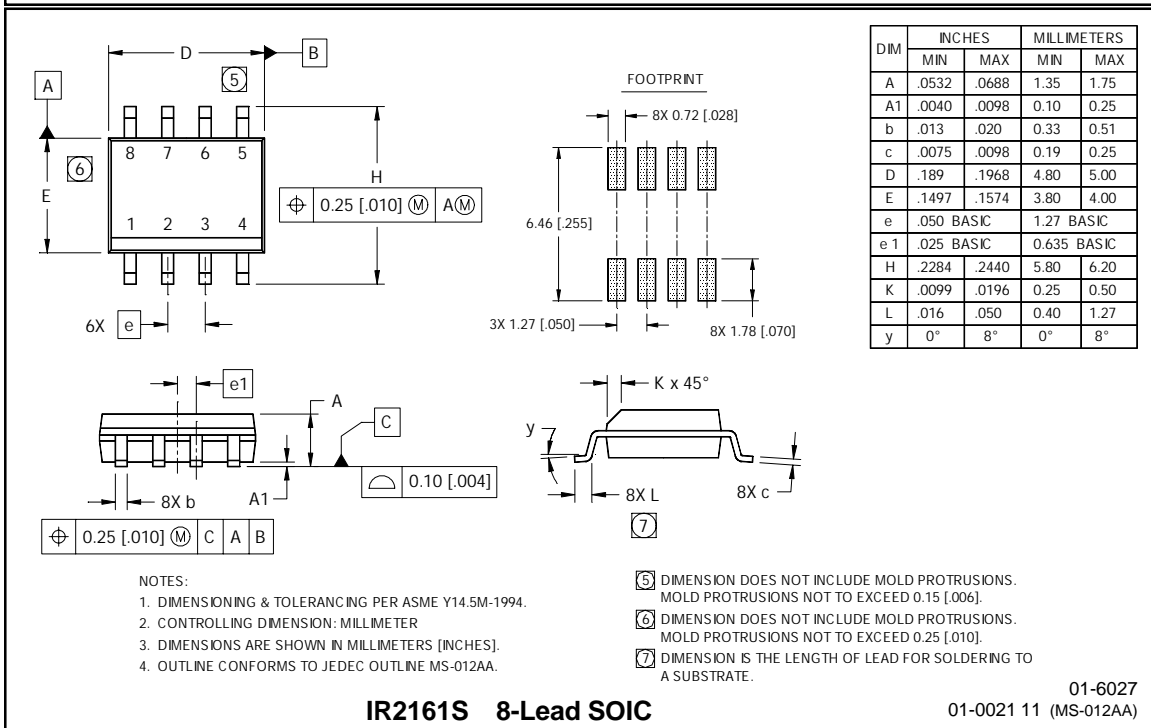
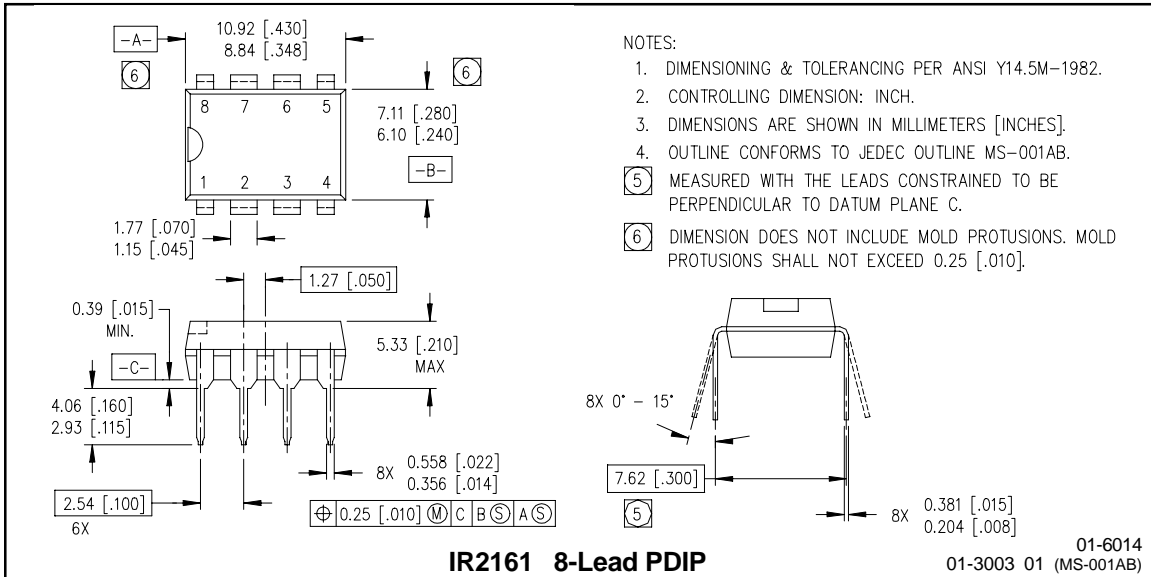


Frequency vs TEMP (IR2161)



Graph : Iss (uA) vs TEMP (IR2161)

Case outlines



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