

IRFB9N65APbF

SMPS MOSFET HEXFET® Power MOSFET

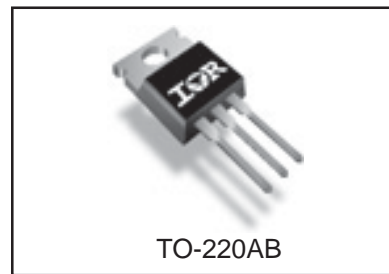
Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Lead-Free

V_{DSS}	$R_{DS(on) \max}$	I_D
650V	0.93Ω	8.5A

Benefits

- Low Gate Charge Q_g results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	8.5	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	5.4	
I_{DM}	Pulsed Drain Current ①②	21	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	167	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③④	2.8	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Typical SMPS Topologies

- Single Transistor Flyback
- Single Transistor Forward

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Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	650	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.67	—	V/°C	Reference to 25°C, I _D = 1mAⓄ
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.93	Ω	V _{GS} = 10V, I _D = 5.1A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 650V, V _{GS} = 0V
		—	—	250		V _{DS} = 520V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g _{fs}	Forward Transconductance	3.9	—	—	S	V _{DS} = 50V, I _D = 3.1AⓄ
Q _g	Total Gate Charge	—	—	48	nC	I _D = 5.2A
Q _{gs}	Gate-to-Source Charge	—	—	12		V _{DS} = 400V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	19		V _{GS} = 10V, See Fig. 6 and 13 ④Ⓞ
t _{d(on)}	Turn-On Delay Time	—	14	—	ns	V _{DD} = 325V
t _r	Rise Time	—	20	—		I _D = 5.2A
t _{d(off)}	Turn-Off Delay Time	—	34	—		R _G = 9.1Ω
t _f	Fall Time	—	18	—		R _D = 62Ω, See Fig. 10 ④Ⓞ
C _{iss}	Input Capacitance	—	1417	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	177	—		V _{DS} = 25V
C _{riss}	Reverse Transfer Capacitance	—	7.0	—		f = 1.0MHz, See Fig. 5Ⓞ
C _{oss}	Output Capacitance	—	1912	—		V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz
C _{oss}	Output Capacitance	—	48	—		V _{GS} = 0V, V _{DS} = 520V, f = 1.0MHz
C _{oss eff.}	Effective Output Capacitance	—	84	—		V _{GS} = 0V, V _{DS} = 0V to 520V ④Ⓞ

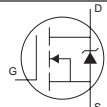
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche EnergyⓄ	—	325	mJ
I _{AR}	Avalanche Current①	—	5.2	A
E _{AR}	Repetitive Avalanche Energy①	—	16	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	0.75	°C/W
R _{θCS}	Case-to-Sink, Flat, Greased Surface	0.50	—	
R _{θJA}	Junction-to-Ambient	—	62	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	5.2	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	21		
V _{SD}	Diode Forward Voltage	—	—	1.5	V	T _J = 25°C, I _S = 5.2A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	493	739	ns	T _J = 25°C, I _F = 5.2A
Q _{rr}	Reverse Recovery Charge	—	2.1	3.2	μC	di/dt = 100A/μs ④Ⓞ
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

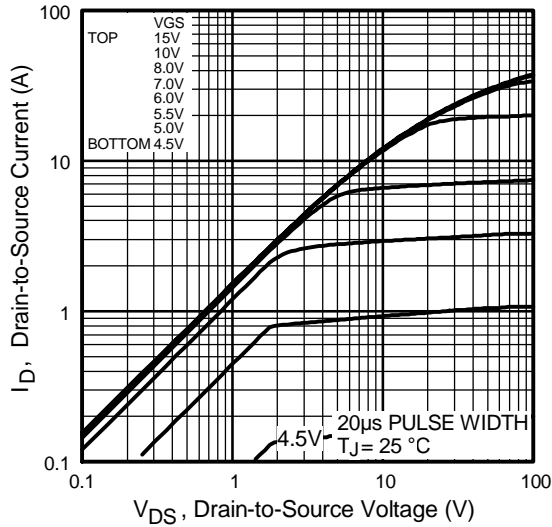


Fig 1. Typical Output Characteristics

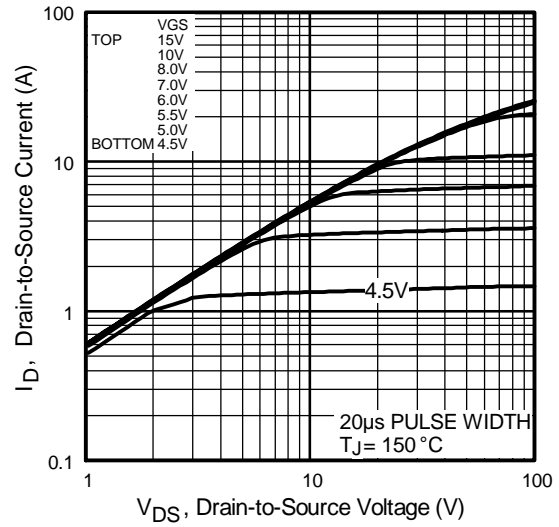


Fig 2. Typical Output Characteristics

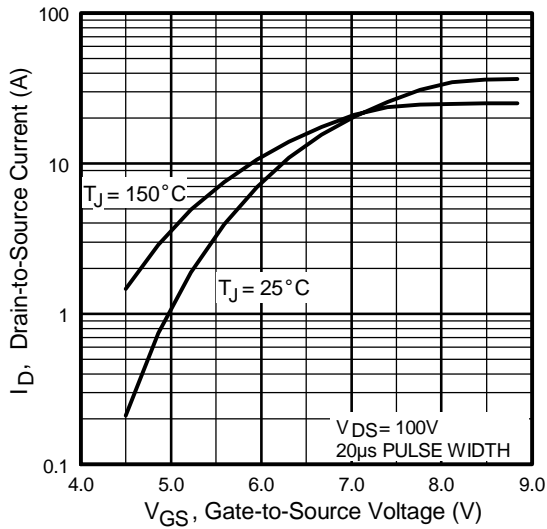


Fig 3. Typical Transfer Characteristics

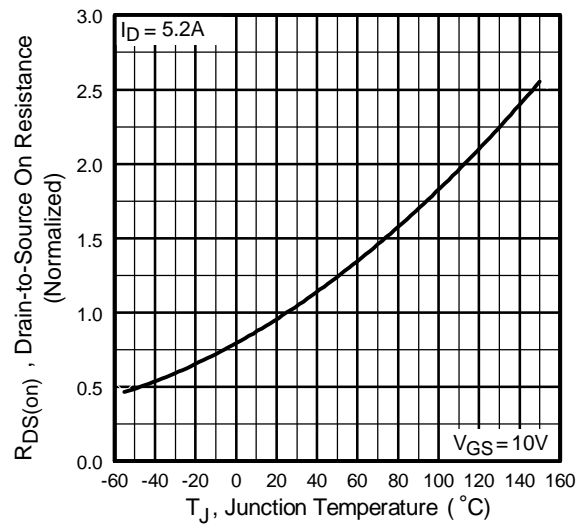


Fig 4. Normalized On-Resistance Vs. Temperature

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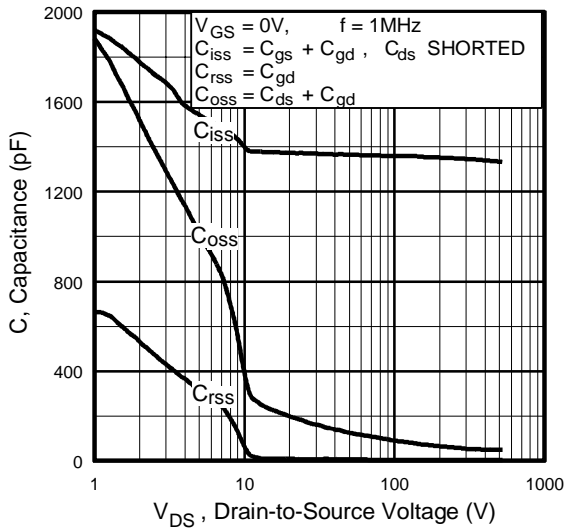


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

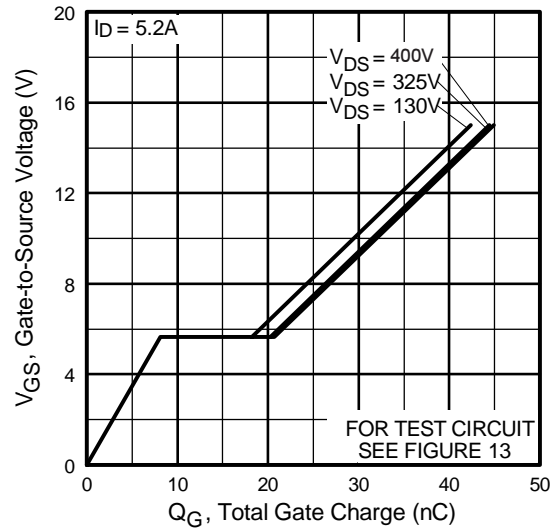


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

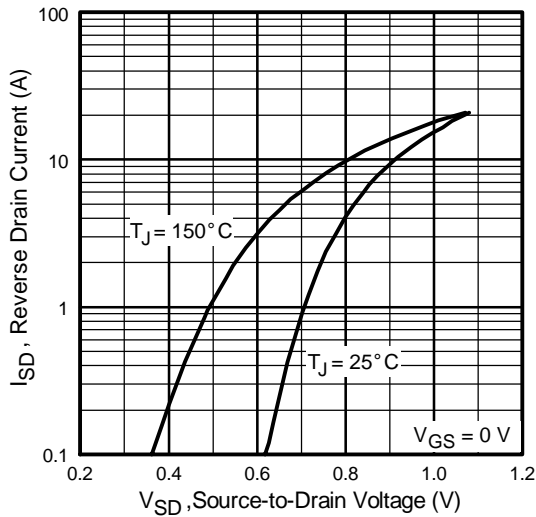


Fig 7. Typical Source-Drain Diode Forward Voltage

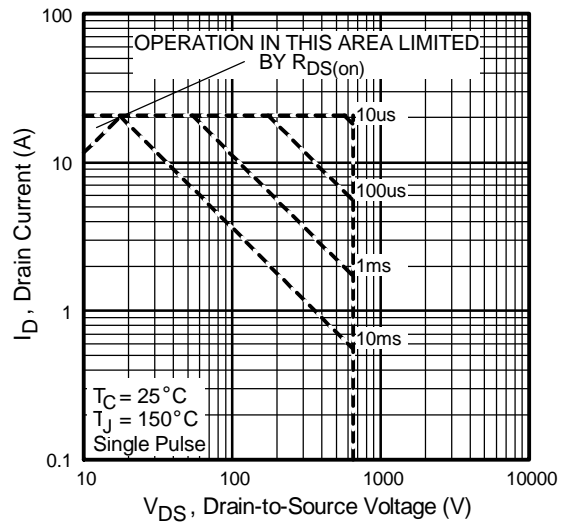


Fig 8. Maximum Safe Operating Area

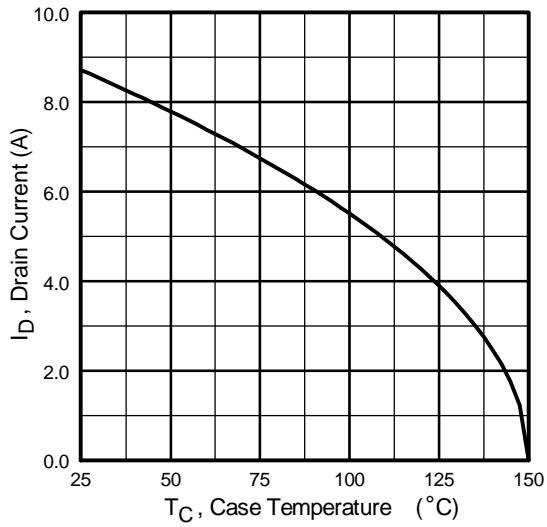


Fig 9. Maximum Drain Current Vs. Case Temperature

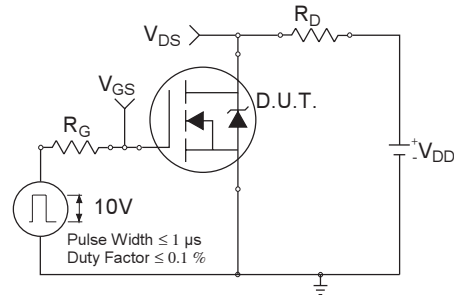


Fig 10a. Switching Time Test Circuit



Fig 10b. Switching Time Waveforms

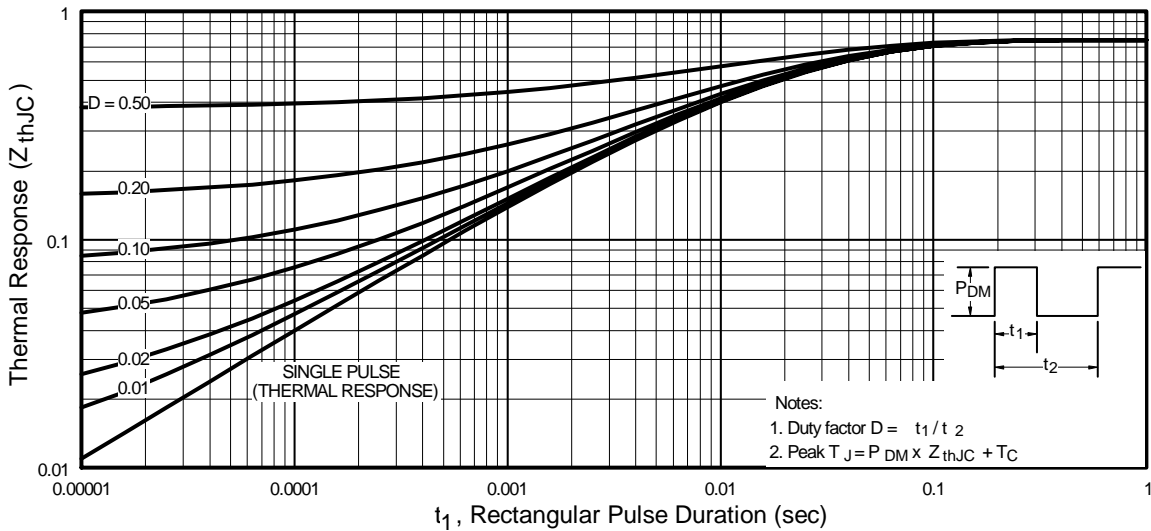


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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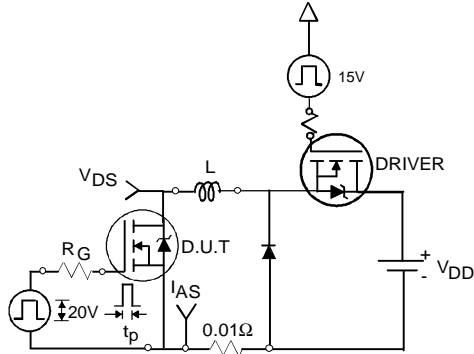


Fig 12a. Unclamped Inductive Test Circuit

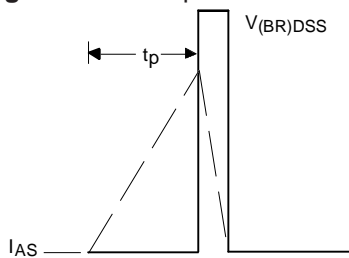


Fig 12b. Unclamped Inductive Waveforms

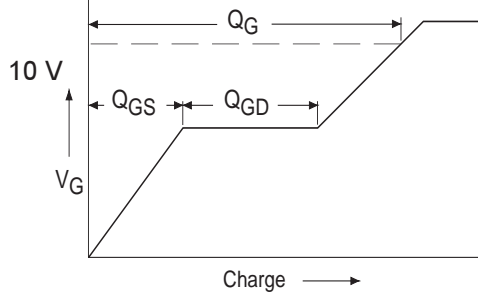


Fig 13a. Basic Gate Charge Waveform

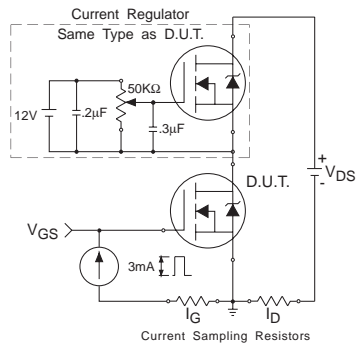


Fig 13b. Gate Charge Test Circuit

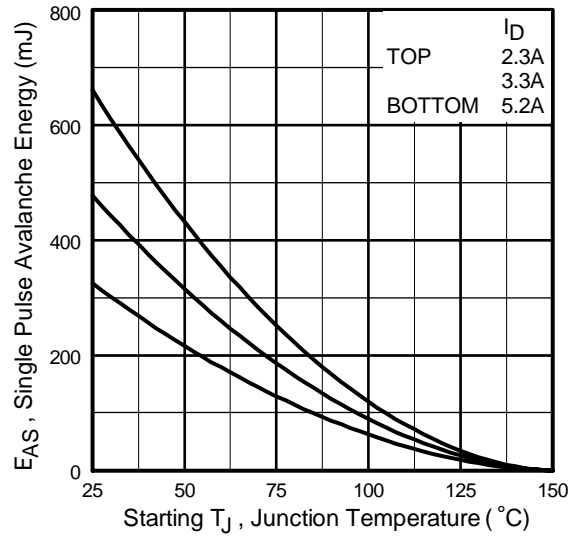


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

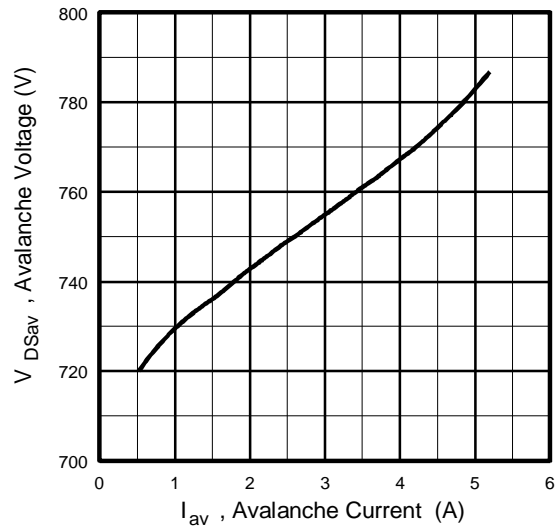


Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

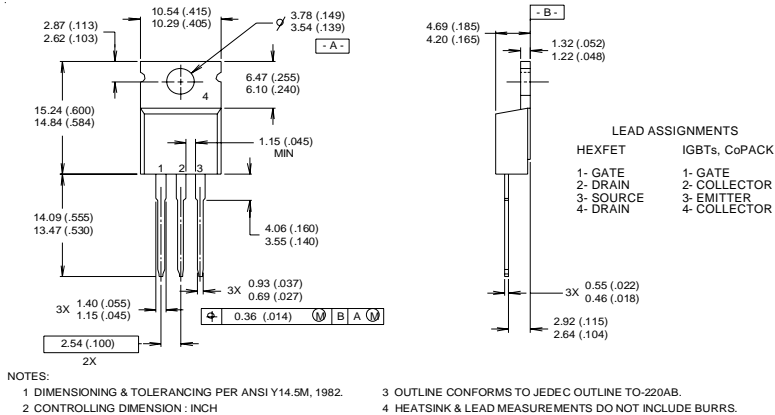
Fig 14. For N-Channel HEXFET® Power MOSFETs

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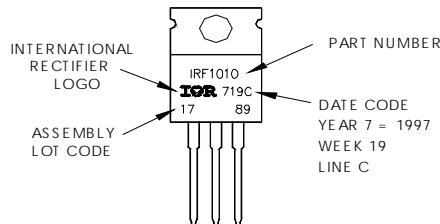
TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"
Note: "P" in assembly line
 position indicates "Lead-Free"



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 24\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 5.2\text{A}$. (See Figure 12)
- ③ $I_{SD} \leq 5.2\text{A}$, $di/dt \leq 90\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}
- ⑥ Uses IRFIB5N65A data and test conditions

Data and specifications subject to change without notice.

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